A 9-72V Input to 1-2.2V Output Single-Inductor Multi-Path Multi-Stage Hybrid DC-DC Converter Achieving 87.8% Peak Efficiency with 110mΩ DCR Inductor

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***Abstract*—This paper presents a single-inductor multi-path multi-stage (MPMS) hybrid DC-DC converter designed for ultra-low voltage conversion ratio (VCR) operation. A design methodology for the inductor-middle hybrid converter architecture is introduced, and an optimized switched-capacitor (SC)-based hybrid converter for both the first and second stages, combined with the proposed multi-path (MP) design, is demonstrated. The MP architecture effectively reduces inductor RMS current and voltage stress on the switches, minimizing losses across a wide V_{IN} range. A start-up control using only internal switches is also employed to pre-charge both the flying and output capacitors appropriately. The proposed MPMS hybrid converter is fabricated in a 0.18µm BCDMOS process and supports a V_{IN} range of 9V-72V and a V_{OUT} range of 1V-2.2V. A peak efficiency of 87.8% is achieved using a compact inductor with a 110mΩ DCR.**

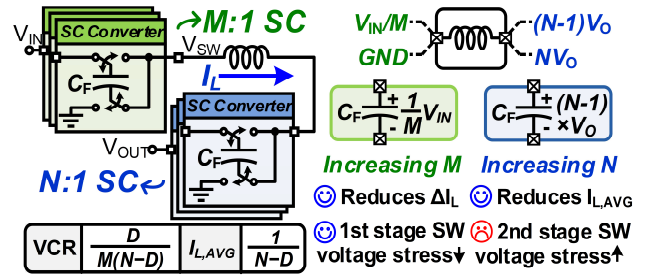
***Keywords*—Hybrid DC-DC converter, multi-path multi-stage, wide input voltage range, ultra-low voltage conversion ratio, inductor-middle DC-DC converter, soft-start.**

I. Introduction

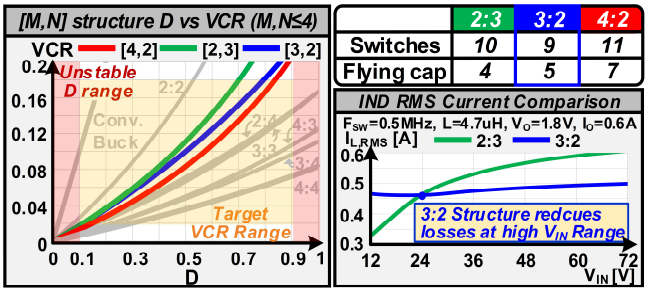
Highly efficient step-down DC-DC converters with ultra-low voltage conversion ratios (VCR), defined as the output voltage (V_{OUT}) over the input voltage (V_{IN}), are increasingly in demand for automotive, data center, and industrial systems. As these applications transition from 12V to 48V inputs and beyond 60V in future technologies, ultra-low VCR converters capable of operating over a wide V_{IN} range have become critical for chipmakers. In addition to the wide V_{IN} requirement, providing flexible V_{OUT} is essential to support diverse system supply voltages.

Inductor-last hybrid converters address ultra-low VCR challenges by reducing inductor ripple (ΔI_L) and voltage stress on switches [1-7], but the inductor still carries the full load current (I_O). In contrast, inductor-first hybrid converters reduce the inductor's average current ($I_{L,AVG}$), but their operable VCR range is limited, especially at low VCR [8-10]. While inductor-middle hybrid converters offer a broad VCR range and effective current reduction [11, 12], [11] requires a large volume inductor to manage ΔI_L and core losses caused by the high V_{SW} swing, and [12] becomes inefficient at ultra-low VCRs due to extremely low duty-cycle (D) operation.

This paper introduces a single-inductor multi-path multi-stage (MPMS) hybrid DC-DC converter for wide-ranging ultra-low VCR operation. To reduce the inductor's RMS current, an optimized hybrid SC-based converter is implemented in both the first and second stages, combined with a multi-path (MP) architecture between these stages. In addition, a start-up control using only internal switches is employed to pre-charge both the flying and output capacitors appropriately.



(a)



(b)

Fig. 1. (a) Inductor-middle hybrid converter. (b) Analysis of different combinations of first and second stage designs.

II. Inductor-Middle Hybrid DC-DC Converter

Fig. 1 shows the architecture of inductor-middle hybrid converter. The inductor is placed between the first and second stage converters, and each stage can be implemented using different step-down converter topologies. To minimize losses and improve the efficiency, it is essential to understand the characteristics of each stage and their impact on architecture's performance is essential.

For optimal design, both the inductor current and the voltage stress on the switches have to be considered. In wide V_{IN} range applications, not only $I_{L,avg}$ but also ΔI_L becomes significant. While $I_{L,AVG}$ dominates $I_{L,RMS}$ at low V_{IN}, ΔI_L increases substantially at high V_{IN} due to the large V_{SW} swing, which can also induce considerable core losses. Therefore, minimizing the RMS current of the inductor ($I_{L,RMS}$) is critical for reducing conduction losses. The voltage stress on the switches also varies depending on the converter configuration.

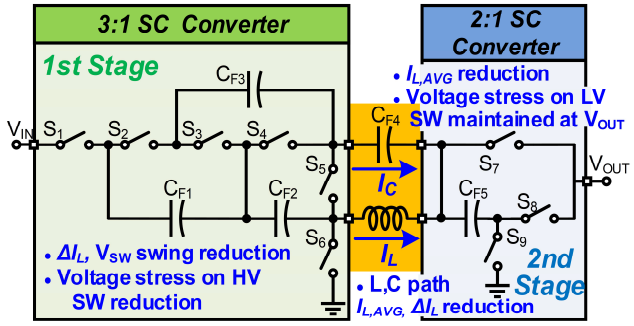


Fig. 2. Proposed single-inductor multi-path multi-stage (MPMS) hybrid converter.

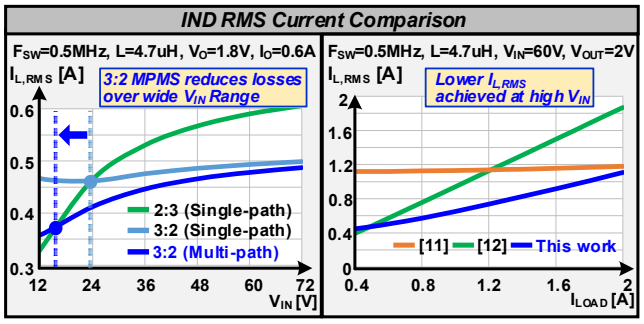


Fig. 3. Inductor RMS current comparison.

In the inductor-middle hybrid converter, ΔI_L is primarily determined by the first stage, whereas $I_{L,AVG}$ is determined by the second stage. In the first stage, using an M:1 SC converter reduces the V_{SW} swing by a factor of 1/M compared to a conventional buck converter, thereby lowering ΔI_L. This also reduces the voltage stress on the switches by the same factor, resulting in significant switching loss reduction, especially at high V_{IN}. Therefore, a higher M is beneficial for mitigating ΔI_L and voltage stress on the switches. In the second stage, using an N:1 SC converter, where the input voltage, corresponding to the inductor's output, switches between (N-1)V_O and N·V_O, reduces $I_{L,AVG}$ to I_O/N. Although it offers the $I_{L,AVG}$ reduction, increasing N results in higher voltage stress on the switches in the second stage, unlike in the first stage design.

The optimal configuration, considering $I_{L,RMS}$ and voltage stress on the switches, depends on the specific V_{IN} and V_{OUT} requirements. As shown in Fig. 1 (b), for a V_{IN} range of 9V to 72V, targeting a VCR range of 0.02 to 0.18, we determined that the optimal values are M = 3 and N = 2. This configuration prioritizes loss reduction by minimizing ΔI_L and inductor core losses at high V_{IN}, while also reducing voltage stress on high-voltage (HV) switches. Although increasing M or N could further reduce $I_{L,RMS}$, it also introduces an excessive number of passive components and switches, leading to higher complexity, additional losses and increased cost.

III. MPMS Hybrid DC-DC Converter

Fig. 2 shows the proposed MPMS hybrid converter which employs 3:1 SC at the first stage and 2:1 SC at the second stage. To further reduce the RMS value of the inductor current, we propose a MP architecture, utilizing a flying capacitor (C_{F4}) to create an additional current path in parallel with the inductor, thereby forming multiple current paths. This architecture not only reduces the inductor's average current through the MP but also decreases its ripple current by further lowering the V_{SW} swing from 1/3V_{IN} to 1/3(V_{IN}–2V_{OUT}).

Fig. 3 depicts the inductor RMS current comparison. The proposed MPMS converter lowers the RMS current over a wide V_{IN} range, and is particularly advantageous at lower V_{IN} levels due to the significant reduction in $I_{L,AVG}$. Compared to prior inductor-middle converters, the proposed converter demonstrates the lowest $I_{L,RMS}$ at V_{IN} of 60V and V_{OUT} of 2V, as both ΔI_L and $I_{L,AVG}$ are effectively mitigated.

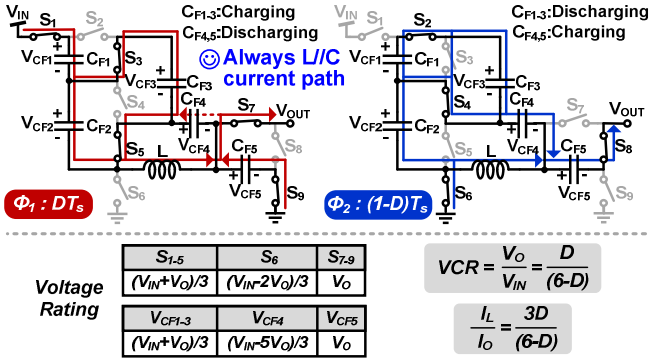


Fig. 4. Operation principle of MPMS hybrid converter.

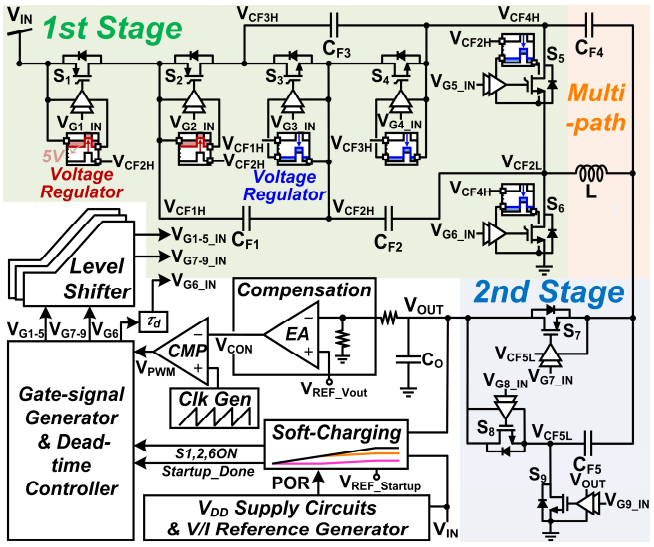


Fig. 5. Overall architecture.

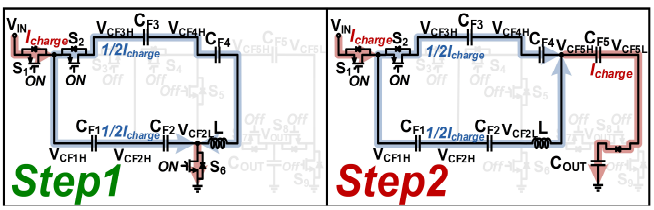
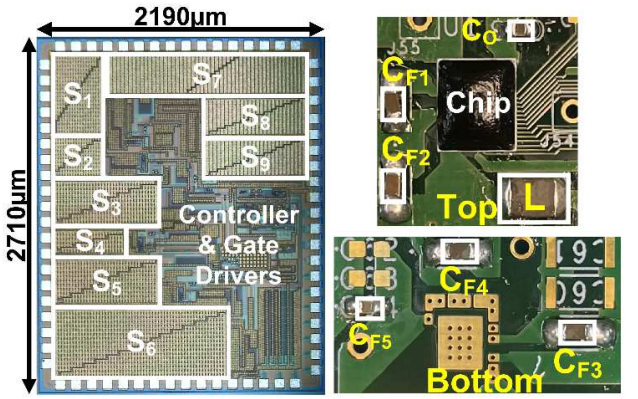


Fig. 6. Start-up control for pre-charging five flying capacitors and an output capacitor.



Component		C_{F1},C_{F2},C_{F3}	C_{F4}	C_{F5},C_O	L
Value		10μF	10μF	10μF	4.7μH (**110mΩ**)
Derated	$72V_{IN}$, $2.2V_{OUT}$	0.17μF	0.89μF	5.53μF	
	$9V_{IN}$, $1V_{OUT}$	6.7μF	9.35μF	8.52μF	
Size		1.6×0.8×0.8 mm³ (**0603**)	1.6×0.8×0.8 mm³ (**0603**)	1.6×0.5×0.55 mm³ (**0402**)	3.2×2.5×2.0 mm³ (**1210**)

Fig. 7. Die micrograph, PCB photo, and summary of passive elements.

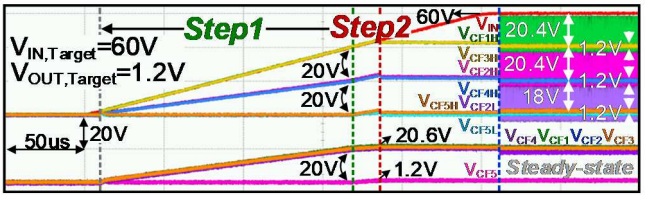


Fig. 8. Measured start-up waveform.

The proposed converter operates in a two-phase mode, as shown in Fig. 4. During phase Φ_1, the output current is supplied by both the inductor and C_{F5}, while during phase Φ_2, it is provided by both the inductor and C_{F4}. Thus, a multi-path current flow is consistently formed, with a flying capacitor always providing current in parallel with the inductor's current path. The VCR of the proposed MPMS converter can be calculated as D/(6-D), ensuring sufficient D for ultra-low VCR. For a D range of 0.1 to 0.9, the VCR spans from 0.017 to 0.176. Furthermore, the voltage stress on the first and second stages is effectively mitigated in the proposed design.

Fig. 5 shows the complete architecture of the proposed MPMS converter. The first stage uses six LDMOS switches, while the second stage employs three low-voltage (LV) CMOS switches. The supply voltage for each gate driver is generated from internal node voltages. Considering the wide V_{IN} range, voltage regulators are used for the gate drivers in the first stage. These regulators generate ~5V when their supply voltage exceeds 5V and track the supply voltage when it is below 5V. The second stage gate drivers use the internal node voltages directly, as these nodes maintain the V_{OUT} swing.

The start-up control for pre-charging five flying capacitors and the output capacitor is implemented using existing switches (Fig. 6). Initially, as V_{IN} begins to rise, S_1, S_2, and S_6 turn on to charge C_{F1}-C_{F4}. When V_{IN} reaches 2/3 of the target level, each capacitor is charged to 1/3 of V_{IN}, and S_6 is turned off. The current then flows through C_{F5}, S_8's body diode, and

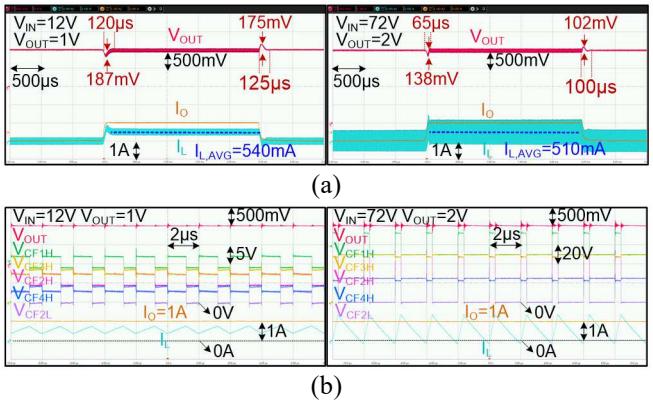


Fig. 9. Measured waveforms. (a) Load transient response. (b) Steady-state.

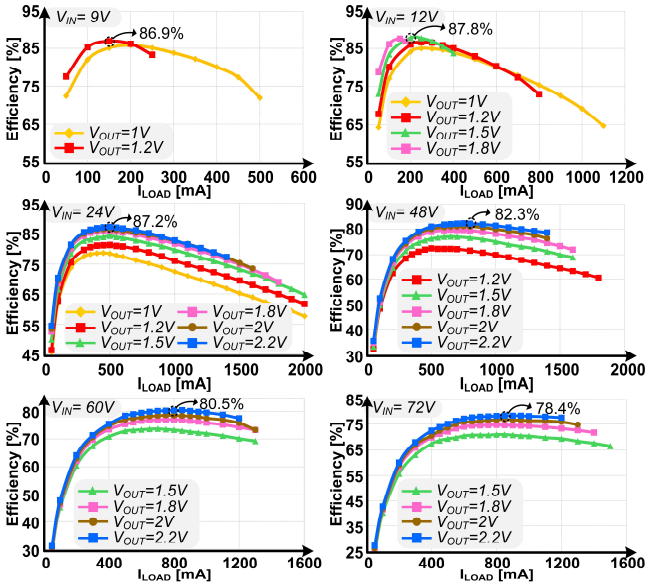


Fig. 10. Measured efficiency.

C_{OUT}, simultaneously charging C_{F5} and C_{OUT}. Once C_{F5} and C_{OUT} reach the target V_{OUT} level. Once C_{F5} and C_{OUT} reach the target V_{OUT} level and C_{F1}-C_{F4} are charged to $1/3V_{IN}$+$1/2V_{OUT}$, all switches turn off. After V_{IN} reaches the target level, the loop begins switching. Any slight charge imbalance in C_{F1}-C_{F4} is resolved within a few switching cycles as the capacitors redistribute their charges to steady-state levels.

IV. Measurement Results

The proposed MPMS converter is fabricated in a 0.18μm BCD process. Fig. 7 shows the chip and board photo with passive components information. It utilizes a 4.7μH inductor with a 110mΩ DCR, occupying a volume of 16mm³ (3.2mm×2.5mm×2.0mm). The flying capacitors C_{F1}-C_{F4} use 10μF with 0603 packaging, while C_{F5} and C_O use a 10μF capacitor with 0402 packaging.

Fig. 8 shows the measured start-up waveform. The flying capacitors and the output capacitor are properly charged through pre-charging sequence, as indicated in Fig. 6, and switching begins when V_{IN} reaches the target level. Fig. 9 shows the measured waveforms of load transient and steady-state. The $I_{L,AVG}$ shows $0.54I_O$ at a V_{IN} of 12V and V_{OUT} of 1.2V, and $0.51I_O$ at a V_{IN} of 72V and V_{OUT} of 2V. Due to the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Parameter	This work	ISSCC24 [11]	JSSC24 [4]	ISSCC23 [12]	JSSC23 [5]	ISSCC22 [6]	ISSCC22 [7]
L location	Middle	Middle	Output	Middle	Output	Output	Output
Process	0.18μm HV	0.18μm HV	0.18μm HV	0.18μm HV	0.18μm HV	0.18μm HV	0.18μm HV
V_{IN} [V]	**9-72 (×8)**	12-60 (×5)	12-48 (×4)	5-24 (×4.8)	48 (×1)	12/24 (×2)	36-55 (×1.5)
V_{OUT} [V]	**1-2.2 (×2.2)**	1.2 (×1)	1 (×1)	2.8-4.2 (×1.5)	0.7-1 (×1.4)	1 (×1)	0.8-2 (×2.5)
Max I_O [A]	2	2	4	5	12	4	3
F_{SW} (MHz)	0.5	0.5	4.5	1.2	0.52-4.4	1	2.5-5
# of SWs	6 LDMOSs & 3 CMOSs	2 LDMOSs & 14 CMOSs	6 LDMOSs	4 LDMOSs & 3 CMOSs	2 GaNs & 9 LDMOSs	2 LDMOSs & 4 CMOSs	7 LDMOSs
$V_{DS,MAX}$ of SWs	$\frac{V_{IN}+V_{OUT}}{3}$	V_{IN}	$\frac{2V_{IN}}{3}$	$\frac{V_{IN}}{2}$	$\frac{V_{IN}}{2}$	V_{IN}	$\frac{2V_{IN}}{5}$
# of L	1	1	3	1	3	2	3
Inductor (DCR)	**4.7μH (110mΩ)**	10μH (N/A)	0.33μH (N/A)×3	2.2μH (35mΩ)	0.62μH (N/A)×3	1.8μH (N/A)×2	0.82μH (N/A)×2
L vol. (mm^3)	3.2×2.5×2	N/A	N/A	3.2×2.5×2	N/A	N/A	N/A
C_{FLY}	10μF×5	22μF×4	1μF×2	10μF, 5.8μF	1μF×5	4.7μF	0.22μF×4
Peak η	87.8%	92.7%	90.7%	**92.4%	90.4%	88.3%	87%
VCR	$\frac{D}{6-D}$	* $\frac{D}{4+4D_1}$	$\frac{D}{3}$	** $\frac{D}{2(1+D)}$	$\frac{D}{10}$	$\frac{D}{2}$	$\frac{D}{5}$
VCR range	**0.014-0.15 (×10.7)**	0.02-0.1 (×5)	0.02-0.08 (×4)	0.12-0.84 (×4)	0.015-0.02 (×1.3)	0.04-0.08 (×2)	0.014-0.055 (×3.9)
Die (mm^2)	5.9	15	3.3	9.4	12	9.6	6.1
Total passive area (mm^2)	19.82	N/A	N/A	24.42	N/A	N/A	N/A
Soft start-up	**O**	X	X	O	X	X	X

***D_1 is a duty cycle used in SPCSC ** LSP mode**

reduced V_{SW} swing, significant reductions in ΔI_L are achieved. Fig. 10 shows the measured efficiency at different V_{IN} and V_{OUT} values. Despite using a compact size inductor with a large DCR (110mΩ), the proposed MPMS converter achieves a peak efficiency of 87.8% at V_{IN} of 12V and V_{OUT} of 1.5V, and 78.4% at V_{IN} of 72V and V_{OUT} of 2.2V. This comparable efficiency, even with a single inductor with a large DCR value, is maintained across a wide V_{IN} range due to lowered $I_{L,RMS}$ and reduced voltage stress on HV switches.

Table I summarizes the performance summary. The proposed converter not only offers the widest V_{IN} range of 9V to 72V but also supports flexible V_{OUT} from 1V to 2.2V. Even with the compact size of a single inductor and capacitors, comparable efficiencies are achieved across a wide V_{IN} and V_{OUT} operation range.

ACKNOWLEDGMENT

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