A 154fs RMS Jitter 4GHz MDLL with Stochastic Sampling Based Spurious Tone Reduction

Dirk Pfaff, *Member, IEEE*, Robert Abbott, Tom Eeckelaert, Ralph Mason, *Member, IEEE*, and Jared Mercier

***Abstract*—This 4GHz multiplying delay-locked loop (MDLL) lowers RMS jitter to 154fs (integrated between 1kHz to 100MHz) while limiting power and area consumption to 6.69mW and 0.0022mm^2 respectively. This is achieved with a digitally controlled ring oscillator (RO-DCO) with moderate phase noise level of -124dBc at 1MHz offset frequency, combined with a resolution of 1MHz and a wide frequency range of 0.67- 5.67GHz. Spurious tones associated with errors in the MDLL clock realignment process are suppressed by timing error measurements based on stochastic sampling and subsequent correction by a digital-to-time converter (DTC).**

***Index Terms*—Multiplying delay-locked loop (MDLL), low-jitter, phase noise, ring-oscillator, reference spur.**

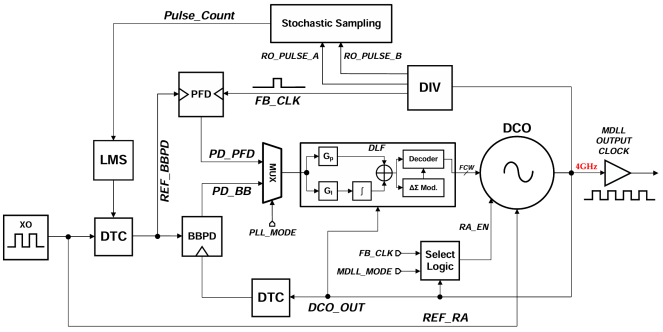


Fig. 1: Proposed system architecture of MDLL.

I. Introduction

Clock synthesizers implemented as Digital Phase-Locked Loops (DPLLs) with Ring Oscillator (RO) Digitally Controlled Oscillators (DCOs) are becoming a popular choice for on-chip frequency synthesis, attributed to low-cost, compact silicon area, and scalability across process nodes. However, the higher jitter level of RO based DPLLs hinders their widespread application and designers often need to resort to resonant LC-tank oscillators to meet jitter objectives, unlocked by their 20dB - 30dB lower oscillator phase noise level [1], [2]. This paper proposes an area efficient, digital process compatible, LC-tank free frequency synthesizer with sub-200fs RMS jitter, thereby extending the application of RO based synthesizers to jitter sensitive applications such as clock generation for high-speed data converters and multi-Gb/s communication transceivers, an area so far reserved to LC-resonator based synthesizers.

The key to lowering the jitter of RO based frequency synthesizers lies in the usage of a high frequency external crystal oscillator (XO) combined with an architecture that leverages the low XO jitter. The traditional digital PLL requires the loop bandwidth to be limited to $1/10$ of the XO clock frequency to maintain stability, which unfortunately restricts RO jitter suppression. On the other hand, Injection-Locked PLLs (IL-PLLs) and Multiplying Delay-Locked Loops (MDLLs) reduce RO jitter accumulation by periodically realigning the noisy RO edge with a clean XO clock edge. The result is that RO phase noise is suppressed in a wider frequency band, thereby relaxing oscillator jitter requirement. In the MDLL case, RO jitter is suppressed up to half the XO frequency, or at least 5 times that of a conventional digital PLL. Nevertheless, recently published IL-PLL and MDLL based synthesizers [5]–[8], [10], [11] exhibit jitter of vastly varying levels. The reasons are numerous, but a relevant root cause for excessive jitter is the added quantization jitter caused by the finite frequency resolution of the DCO, which can be expressed as [4]

$$\mathcal{L}(\Delta f) = \frac{1}{12}\left[\frac{\Delta f_{LSB}}{\Delta f}\right]^2 \frac{1}{f_{inj}}\left[2sin(\frac{\pi \Delta f}{f_{inj}})\right]^{2n}, \qquad (1)$$

where Δf_{LSB} is the frequency resolution, f_{inj} is the injection frequency, and n is the order of the $\Delta\Sigma$ modulator. Eq. (1) stresses the fact a DCO with sufficiently fine frequency resolution is mandatory to meet jitter objectives.

Also, an MDLL based clock synthesizer type is prone to the generation of undesired spurious tones. Without the addition of dedicated correction circuits, the XO edge is likely misaligned against the DCO clock edge that is being realigned. This causes a periodic disturbance of the MDLL output clock, manifesting in reference spurious tones with levels expressed as [7]

$$dBc_{MDLL}(f_{out} \pm f_{XO}) \approx 20log(t_{SPO} \times f_{out}). \qquad (2)$$

Here f_{out} and f_{XO} represent the MDLL output and XO frequency respectively. The timing parameter t_{SPO} represents the static phase offset (SPO) between the XO edge and the DCO edge to be aligned. A digital-to-time converter (DTC) can be introduced to eliminate SPO, which leads to a significant reference spurious tone reduction when configured for optimum delay. However, a background DTC calibration method needs to be introduced to ensure that the SPO remains cancelled as operating temperatures and voltages change. The proposed MDLL utilizes a novel, in-situ, spurious tones detection and correction method. This is paired with a carefully designed DCO optimized for best possible random jitter.

II. MDLL

A. MDLL Architecture

The MDLL architecture, shown in Fig. 1, incorporates a conventional DPLL with the DCO's frequency control word (FCW) set by a digital loop filter (DLF). The filter evaluates the bang-bang phase error by a proportional and integral path to form a second order, type II PLL loop. A second order MASH sigma-delta modulator refines the frequency resolution of the DCO. The feedback loop is closed by the programmable frequency divider and a phase-frequency detector (PFD) which is used to establish initial locking, aided by the unlimited lock range offered by the PFD. After initial phase locking has been established, the DPLL is relocked using a flip-flop based bang-bang phase detector (BBPD) in preparation for MDLL clock realignment operation. The BBPD eliminates the feedback divider from the loop [3], which removes not only a noise source, but more importantly, reduces SPO prior to calibration, which in principle is now exclusively limited to the smaller timing error of the BBPD itself. With the SPO greatly reduced, clock realignment can be activated without inadvertently unlocking the DPLL. MDLL clock realignment is facilitated by a multiplexer, built into the DCO, which selects between the internal ring oscillator clock and the XO injection clock REF_RA. The select logic block periodically asserts the multiplexer control input RA_EN to realign the DCO. The RA_EN signal timing is designed such that the DCO output clock remains glitch free. The remaining circuits shown in Fig. 1 are used for spurious tones suppression and will be explained in Chapter III.

B. Digitally Controlled Oscillator

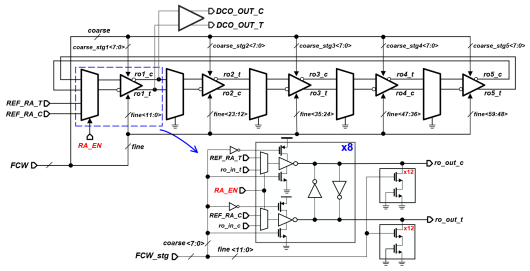


Fig. 2: DCO architecture and stage.

The 5-stage RO-DCO combines coarse and fine frequency tuning for a wide tuning range of 0.67 – 5.67GHz and a fine frequency resolution of 1MHz. The structure of the RO-DCO is shown in Fig. 2. Coarse tuning is realized by programming of the inverter drive strength by means of activation of parallel, tristate inverter segments. A total of 150 coarse settings are available with an average step size of 30MHz. Fine tuning relies on a thermometer coded capacitor bank with 60 capacitors distributed across the 5 DCO stages, providing 60 settings. The DCO delivers true and complementary output buffered phases and is completed by multiplexers for clock realignment with the unused stages select signals connected to a tie-low. Cross-coupled inverters are implemented for pseudo-differential operation.

III. Spurious Tone Suppression

The reference spurious tones are minimized by cancellation of the SPO, or the offset between the injection clock path and the BBPD clock path. This offset can be lowered by matching of the two clock paths, but best possible SPO elimination requires two DTCs in the XO to BBPD and DCO to BBPD clock paths, as shown in Fig. 1. Notice that the XO to DCO injection path is free of any delay circuits to ensure that the realignment clock maintains the lowest possible random jitter. The spurious tone level can be measured with a spectrum analyzer in a test environment and reduced by adjustment of the DTC delay, but an automated, on-silicon and in-situ calibration method needs to be introduced in any practical application. Fortunately, the SPO can be assessed by analyzing DCO clock pulses. The used technique is illustrated in Fig. 3.

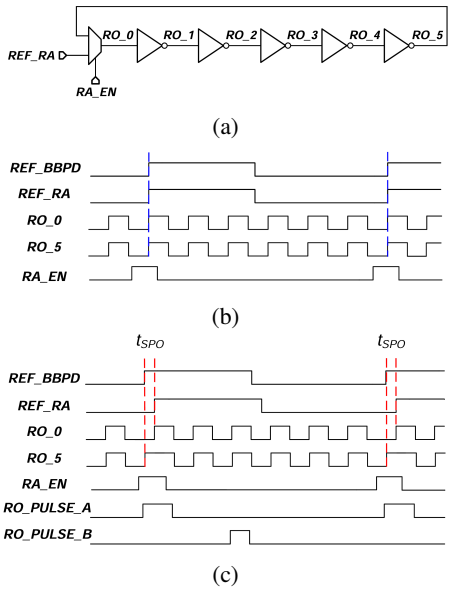


Fig. 3: (a) Ideal 5-stage RO-DCO. (b) Timing diagram of the RO-DCO pulses without SPO. (c) Timing diagram of RO-DCO and derived RO_PULSE_A and RO_PULSE_B pulses when SPO is present.

Fig. 3(a) shows the simplified RO-DCO with internal nodes $RO\_0, \ldots, 5$. Presuming a delay-free MUX, RO_5 and RO_0 are aligned since no SPO is present. Fig. 3(c) shows how the timing is altered when a positive SPO is present. Here, the realignment clock REF_RA is lagging REF_BBPD by t_{SPO}, delaying RO_0 by the same amount. To maintain phase locking, the PLL will speed up the RO-DCO to compensate for the late alignment clock. The positive clock edge of RO_0 and RO_5 are now separated by t_{SPO}, which increases the pulse width at RO_5 during realignment. Additional logic built into the feedback divider is used to extract the widened pulse, RO_PULSE_A, along with a reference pulse

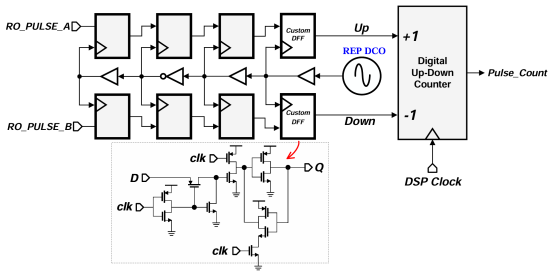


Fig. 4: Stochastic sampling circuitry.

RO_PULSE_B. Note that RO_PULSE_A is shorter than RO_PULSE_B in the case of negative SPO.

A least-mean-square (LMS) algorithm evaluating the pulse duration difference is introduced to minimize the reference spurious tones. Fig. 4 illustrates the circuitry to achieve stochastic sampling. RO_PULSE_A and RO_PULSE_B are sampled by flip-flops to generate pulses (Up, $Down$) if a logic high input was sampled. Otherwise, these signals remain low. It can be shown that the sampling is uniformly distributed as long as the sampling clock is sufficiently noisy and asynchronous to the sampled signal [9]. Both criteria are met using a noisy replica RO-DCO configured with a FCW different from the main DCO. Therefore, the likelihood of a Up and a $Down$ occurrence is a direct measure of the duration of RO_PULSE_A and RO_PULSE_B respectively. Following the sampling process, Up and $Down$ are counted using a large-number, digital counter.

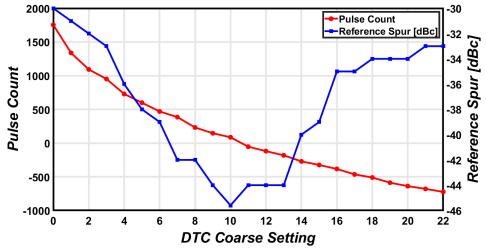


Fig. 5: Pulse count and reference spur vs. DTC coarse setting.

Based on the error signal generated from the digital counter, $Pulse\_Count$, an LMS algorithm controls the DTC settings. Fig. 5 shows the measured $Pulse\_Count$ and reference spur vs. DTC control setting. It can be seen that the DTC setting resulting in the lowest spurious tone level coincides with $Pulse\_Count$ equal zero. Therefore, this measurement confirms that the latter parameter can be used to reliably calibrate the reference spurious tones. The best reference spurious tones suppression achievable with this implementation is -46dBc, which is limited by the DTC coarse tuning step size of 1.5ps. This spurious tone level is predicted by Eq. (2) evaluated for a 4GHz MDLL output clock. Significantly improved calibrated spurious tone level can be expected from the proposed calibration technique when a finer resolution DTC is engaged. This can be readily achieved by utilizing the capacitor bank of Fig. 2.

IV. Measurement Results

The proposed MDLL is fabricated in TSMC's 5-nm FinFET process node. The MDLL operates on a nominal 0.75V supply voltage consuming a total power consumption of 6.69mW. Fig. 6 shows the measured phase noise spectrum using a Keysight E5052B of the proposed MDLL locked to a 491.567MHz off-chip crystal. The phase noise and integrated jitter measurements are shown at optimal loop filter settings and performed at room temperature. The RMS jitter is 154fs integrated between 1kHz-100MHz. The phase noise at 1MHz frequency offset is -124 dBc/Hz.

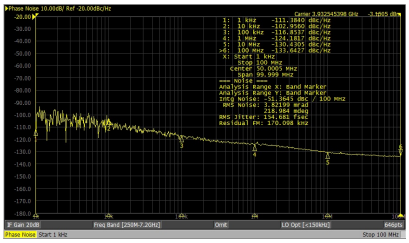


Fig. 6: Measured output phase noise when MDLL mode is enabled from 1KHz to 100MHz offset from 4GHz carrier.

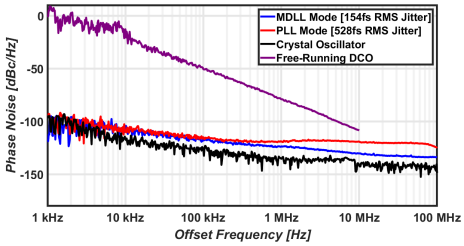


Fig. 7: Measured output phase noise of MDLL, PLL, crystal, and DCO.

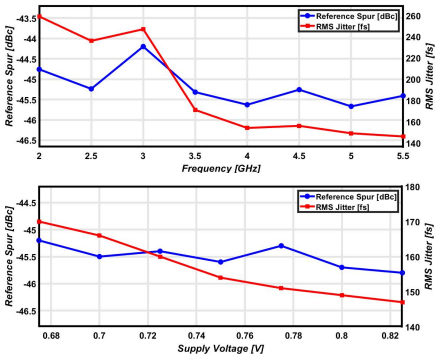


Fig. 8: Measured reference spur and RMS jitter vs. (a) frequency and (b) supply voltage.

Fig. 7 shows the measured phase noise of the MDLL, PLL, crystal oscillator, and free-running DCO. The PLL RMS jitter, integrated from 1kHz to 100MHz, is 528fs, but drops to 154fs when MDLL clock realignment is enabled. This

TABLE I: Performance Comparison of Ring-Based Injection-Locked PLLs.

Parameter	**This Work**	SSCL'2020 B.Liu [5]	CCIC'2019 A.Santi. [6]	ISSCC'2018 S.Yang [7]	SSCL'2019 B.Liu [8]	SSCL'2024 H.Hua. [10]	ISSCC'2015 W.Deng [11]
Tech.	5nm	5nm	65nm	28nm	65nm	65nm	65nm
Arch.	MDLL	IL-PLL	MDLL	MDLL	IL-PLL	MDLL	Soft-IL
Freq. Range [GHz]	0.67-5.67	0.4-1.5	1.6-3.0	1.55-3.35	N/A	0.9-1.2	0.8-1.7
Freq. [GHz]	4	1	1.65	3	1	1.04	1.5
Ref. Freq. [MHz]	492	100	100	200	100	104	400
Ref. Spur [dBc]	-46	-31	-50	-44	-52	-35	-58
RMS Jitter [fs]	**154**	740	397	292	400	4980	3600
Int. BW [MHz]	0.001 - 100	0.01 - 10	0.03 - 30	0.01-40	0.01 - 10	0.01 - 10	0.001 - 100
Power [mW]	6.69	0.52	2.5	1.45	1.2	5.52	3
FoM [dB]	**-248.0**	-245.5	-244	-249.1	-247.2	-242.6	-224.4
Active Area [mm^2]	0.0022	0.0036	0.0275	0.0056	0.035	0.0892	0.048

*FoM = 10log $\left[(\frac{\sigma_{rms}}{1s})^2(\frac{P_{DC}}{1mW})\right]$.

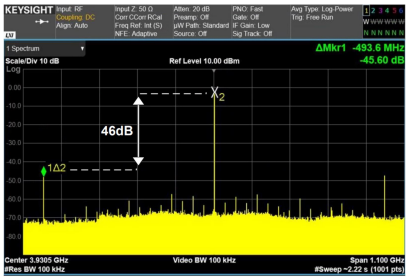
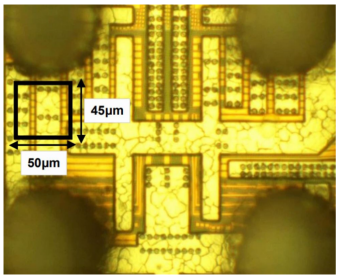


Fig. 9: Measured output spectrum of MDLL after spurious tone calibration.



Power (mW)	
DCOs	3.45
DTCs	1.36
DSP	1.88
Total	6.69

Fig. 10: Die Micrograph and power breakdown.

jitter reduction is attributed to lower MDLL phase noise in the 1MHz to 100MHz band, confirming that the MDLL loop bandwidth significantly exceeds the PLL loop bandwidth. The measured reference spur and RMS jitter vs. frequency and supply voltage are shown in Fig. 8. Fig. 9 shows the frequency spectrum of the MDLL after the spurious tone calibration. The measured reference spur using a Keysight N9030B PXA Signal Analyzer is approximately -46dBc. Fig. 10 shows the die micrograph of the MDLL which occupies an active area of 0.0022mm^2. The performance of the MDLL is compared with state-of-the-art ring-based IL-PLLs as shown in Table I. This design achieves best in class RMS jitter and an excelled jitter-power FoM of -248.0dB.

V. Conclusion

A highly-digital low-jitter MDLL is presented. The MDLL achieves low noise by utilizing a high-frequency reference operating at 492MHz, high DCO frequency resolution using the parasitic capacitance of a minimum sized NFET transistor obtaining a 1MHz/LSB resolution, high-frequency LSB dithering, and a low-noise BBPD. The MDLL is implemented in TSMC 5-nm FinFET process and achieves an RMS jitter of 154fs integrated between 1kHz-100MHz at 6.69mW of power.

VI. Acknowledgement

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