A 9.98-ENOB 8 kHz Bandwidth 100-260 nW DT Level-Crossing ADC for Sparse and Generic Signals

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***Abstract*—This paper presents an event-driven Discrete-Time Level Crossing Analog-to-Digital Converter (DT-LCADC) that is energy-efficient in the conversion of both sparse and generic signals, and exploits signal sparsity to reduce the output data rate. The proposed DT-LCADC uses the comparator delay, to classify each level-crossing event as slow or fast, according to the rate of change of the input signal. The converter can adaptively select the most suitable search scheme, between linear and binary, according to the type of event. The proposed DT-LCADC, manufactured with 65 nm CMOS technology, achieves 9.98 ENOB and a signal bandwidth of 8 kHz, while consuming between 100 and 260 nW from a 0.8 V supply, depending on the input signal. The corresponding Walden FoM$_W$ ranges from 6.2 to 16.1 fJ/c.s, achieving a more than 4X improvement in worst-case power efficiency compared to state-of-the-art DT-LCADCs. To convert time-sparse neural signals, the proposed ADC requires only 110 nW, while reducing the output data rate down to 8.9 kb/s. This leads to a compression ratio of 94.4%, compared to a Nyquist ADC with the same accuracy.**

***Index Terms*—Data Compression, Edge Computing, Event-Based Sensor Interface, Level-Crossing ADC, Time-sparse signal.**

I. Introduction

Edge data processing is becoming increasingly popular in applications, such as tactile electronic skins [1] for robots and wearable biomedical devices [2] for healthcare. By processing data directly at the source, the data rate required to describe signals can be significantly reduced by utilizing the knowledge of the signals being acquired. In this way, the amount of data to be stored or transmitted can be minimized, improving overall resource efficiency and energy consumption. To accomplish this aim, the hardware needs to be highly energy efficient and specifically tailored to the target signals. For example, time-sparsity is a common signal characteristic in the aforementioned applications: event-driven sensing based on continuous-time (CT) level-crossing analogue-to-digital converters (LCADCs) [2]–[4], has been shown to be an efficient approach to convert sparse signals in a train of pulses.

Unlike conventional uniform sampling Nyquist Analog-to-Digital Converters (ADCs), CT-LCADCs perform sampling and conversion only when the input signal crosses predefined thresholds (levels), as shown in Fig. 1 (a-b). Therefore, when the signal amplitude remains within two levels for a certain interval of time (i.e., the signal is "sparse" in time, having long intervals when no change or information is observed), the CT-LCADC will not perform any conversion, saving power. The issue of CT-LCADCs is that the following digital processors need to either be able to operate with asynchronous signals [2] or must operate at a very high clock frequency to re-time the pulses without introducing excessive quantisation noise and prevent signal distortion. As an example, the CT-LCADC in [3] requires a re-timing clock running at a frequency 3600x higher than the bandwidth, resulting in a large power consumption overhead.

To ease the integration of Level Crossing ADCs in digital systems, while maintaining the advantages in terms of data compression, a Discrete-Time LCADC (DT-LCADC) has been proposed in [5]. In a DT-LCADC, the input signal is converted into a digital output at a clock edge, only if the current sample amplitude is one or more levels away from the previous one (Fig. 1 (d)). Being the output bitstream synchronous to a clock, the DT-LCADC integration in digital systems is easier and can be more energy-efficient than the CT-LCADC counterparts. However, these advantages are obtained at the cost of a higher converter power consumption since the comparator is activated at each clock cycle, even in the absence of signal amplitude variations. Attempts to reduce power consumption have been proposed in [6] and [7], leading to DT-LCADC architectures that are competitive with CT-LCADC ones. The efficiency in [7] is still limited by its synchronous delta modulation, which requires a large oversampling. In [6], the ADC conversion is based on a predefined number of linear searches that are triggered when the input amplitude crosses a level. The DT-LCADC in [6] operates at a significantly lower oversampling rate, which, however, remains 13 times higher than the converter bandwidth. This clock speed is needed because of the inefficiency of the linear search algorithm in following the input when this signal has fast variations, and thus is close to the ADC bandwidth. Additionally, the energy efficiency of a

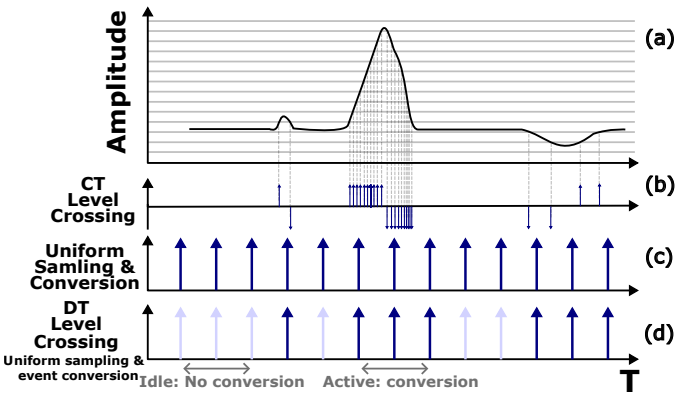

Fig. 1: (a) Time-sparse signal example. (b) CT event-driven sampling and conversion, (c) Conventional uniform sampling and (d) DT sampling and event-driven conversion

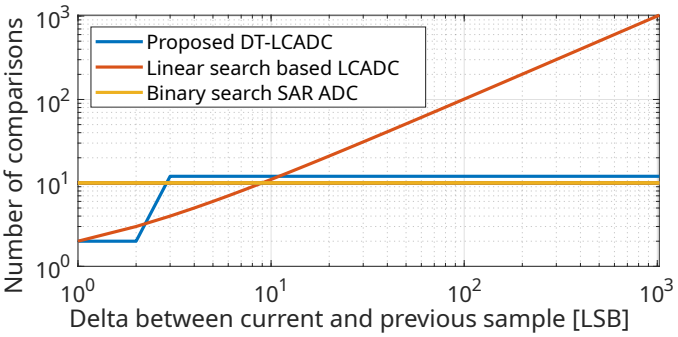

Fig. 2: Number of comparisons required to perform one conversion versus delta amplitude between adjacent samples.

DT-LCADC is signal dependent and significantly degrades if the input signal is not sparse.

To fill this gap, we propose here a new DT-LCADC architecture that maintains energy efficiency for sparse and non-sparse inputs, achieving best in class Walden Figure of Merit (FoM$_W$) and the highest data Compression Ratio (CR) among state-of-the-art LCADCs.

This paper is further structured as follows: Section II describes the main innovation and the proposed LCADC topology. Section III shows the measurement results and a performance comparison with the state-of-the-art. Conclusions are drawn in Section IV.

II. Proposed DT-LCADC

A. Adaptative search concept

State-of-the-art DT-LCADCs [6], [7] use a linear search algorithm starting from the value of the previous sample. If the delta between the new sample and the previous one is small, the search converges to the new sample in few comparisons, maximizing the energy efficiency (Fig. 2). However, if the signal has faster changes, the linear search will need many more comparisons (Fig. 2). In this case, a Successive Approximation Register (SAR) binary search would be way more efficiency in number of comparisons and energy. In a nutshell, the approach used in this work observes the time needed by the comparator to make a decision between the previous and the current sample. If the comparator decision is slow, the delta between samples is small and thus a linear search is used. If the decision is fast, the change is large and thus a complete SAR search is performed.

B. ADC Architecture

Fig. 3 shows in detail the proposed DT-LCADC circuit architecture and timing diagram. The ADC can cope with 8 differential channels. The input channels are time-multiplexed. For simplicity, the timing diagram focus on one channel without multiplexing. The signal is sampled at the rising edge of Clk_{sys}. After sampling, the dynamic comparator is triggered, generating internally oversampled $Ready$ pulses to synchronise subsequent operations [8]. An inverted and delayed version of the $Ready$ signal is fed back to the comparator input Clk_{comp}. The first and second periods of $Ready$ are needed for every sample. The DAC is precharged to the previous sample (stored in a shift register, which keeps the information for each channel). Before the first comparison, the DAC is incremented by 1 LSB, and at the second comparison the DAC is decremented by 1 LSB. In such a way, the ADC checks if the present sample is within $\pm 1V_{LSB}$ from the previous one. If this is not the case, a Level is crossed and thus LC becomes high.

The $Ready$ signal indicates when the comparisons are complete. By introducing a current-starved inverter as a reference delay and propagating the start of the comparison signal Clk_{comp}, through it, the comparator delay can be monitored [9]. If the comparator delay is lower than the reference one, the current sample is far away from the current DAC content. This is here denoted as a 'Fast' event. Conversely, if the current sample is close to the current DAC content, a 'slow' event occurs. The boundary between fast/slow detection can be set to 1 LSB by tuning the reference delay with an external V_{bias}.

The information provided by LC detected and Slow/Fast event is used to control the DAC. If LC and Fast are detected (Sample 3 in Fig. 3), a complete SAR conversion will be performed, self-synchronised by the comparator $Ready$ signal. The conversion result will be written to a 10-b shift register memory for this channel. If LC and Slow are detected (Sample 2 and 4 in Fig. 3), the comparator will be disabled and the SAR logic will not be triggered. To update the LC threshold window, the digital code (stored in the shift register) representing the previous sample will be incremented or decremented by 1 LSB according to the results of the first two comparisons. If no level is crossed, the comparator will

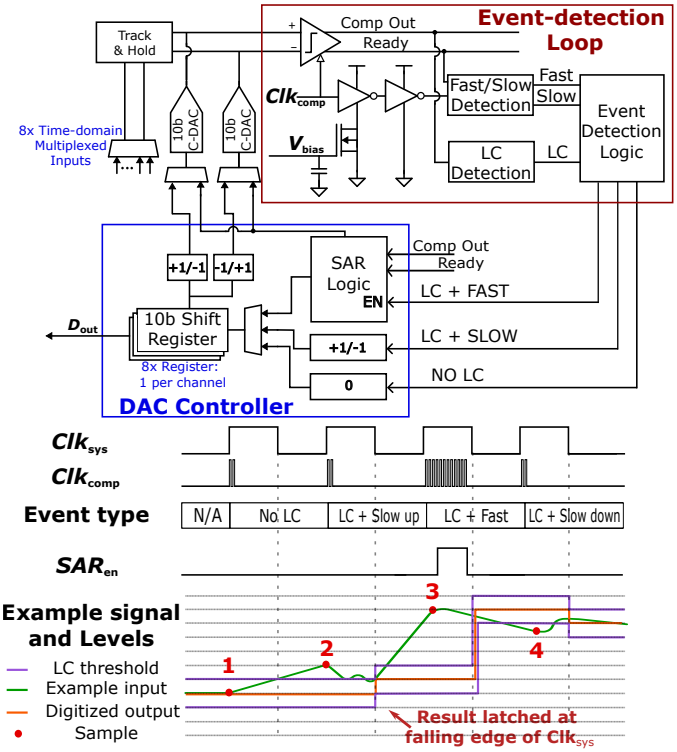

Fig. 3: Proposed LCADC architecture and its timing diagram

also be disabled, and no further actions will be performed until the next sample. It should be noted that the ADC remains perfectly functional for large variations of the reference delay. However, its performance will slightly degrade if the reference delay is different from the delay given by the comparator when 1 V_{LSB} is present at its inputs. For this reason, in future implementations, the reference delay can be e.g., defined by a Delay Locked Loop.

III. Measurement Results

The proposed 10-bit DT-LCADC has been manufactured in 65nm CMOS technology (Fig. 4) and occupies an area of 0.04 mm^2. This DT-LCADC requires a minimum oversampling ratio of 2, to prevent DAC overvoltages when the input switches between two successive samples with relatively large amplitudes and opposite phases. Since this LCADC topology performs both time sampling and amplitude quantization, post-interpolation (based on, e.g., spline) [3] is not necessary to reconstruct the output signal. The 8-channel DT-LCADC is operated at a clock frequency (Clk_{sys}) of 256 kHz, leading to 32 kS/s sampling rate and 8 kHz bandwidth per channel. The recorded DT-LCADC output obtained for a 1 kHz input tone test reveals an SNDR=61.8 dB in 8 kHz bandwidth (Fig. 5) corresponding to 9.98 Equivalent Number of Bits (ENOB).

Fig. 6 shows the trend of the measured SNDR when varying the amplitude and frequency of a sinusoidal input tone, and the corresponding power consumption, further decomposed into its digital and analog components. The digital power includes contributions from the comparator, digital logics, and memory, while the analog one contains only the power consumed by the DAC. At the two extremes of the frequency span, the converter power consumption exhibits different asymptotic trends: for input frequencies smaller than 10 Hz, most of the adjacent samples differ by less than 1 LSB, never triggering a complete search. On the other hand, for input frequencies higher than 300 Hz, most events are classified as "fast", requiring a complete binary search for nearly each conversion.

To further evaluate the performance of the converter, examples of neural signals available in the dataset [12] have been selected as test input. The signals in the data set have been first digitally pre-processed with a first-order 8 kHz bandwidth low-pass filter as discussed in [6]. An example of a digitalized output signal is shown in Fig. 7(a) (blue), together with the input raw data (orange). On average, the proposed LCADC requires 110 nW/channel to convert such neural signals, which is only 10 nW more than for DC inputs, proving its efficiency in dealing with time-sparse signals.

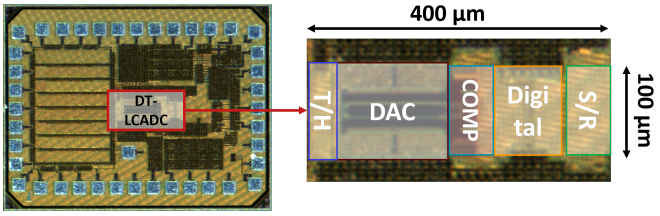

Fig. 4: Micrograph of the proposed DT-LCADC

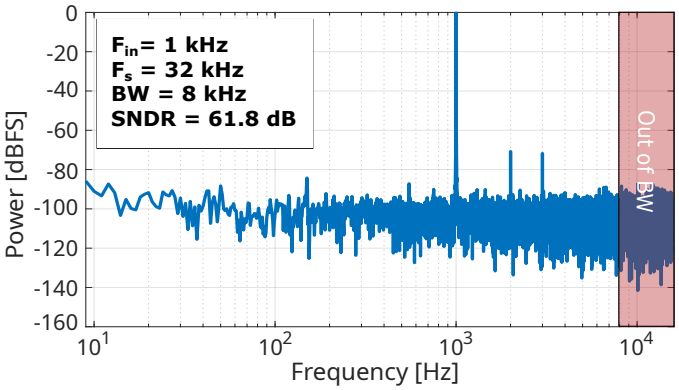

Fig. 5: Measured spectrum of the digitalized output for a 1 kHz single tone test.

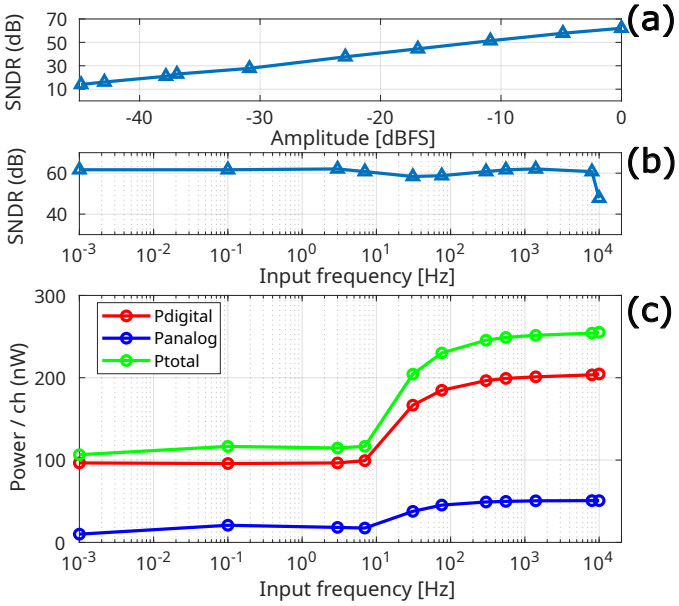

Fig. 6: (a) SNDR versus input amplitude. (b) SNDR versus input frequency. (c) Measured power consumption versus sinewave input frequency.

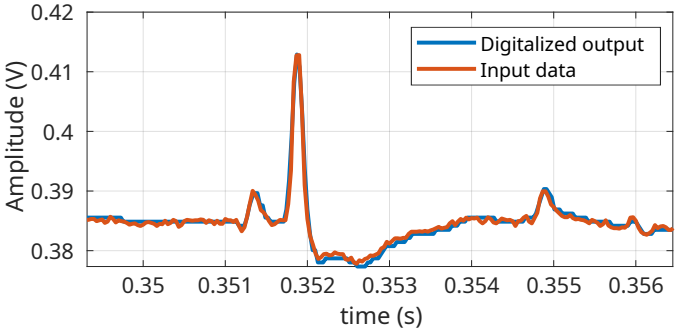

Fig. 7: Original versus digitalized neural signal.

For the conversion of the considered neural signals, the proposed converter achieves an average data rate D_{LC}=8.9 kb/s/channel. Indeed, the compact encoding of each slow event (2 bits) enables a significant data reduction from D_{conv}=160 kb/s/channel otherwise required by a Nyquist ADC. This reduction corresponds to a data compression ratio (CR) [13]

TABLE I: Proposed DT-LCADC performance summary and comparison with the state-of-the-art

	This work	van Assche ESSCIRC22 [7]	van der Ven ASSCC24 [6]	Li ESSCIRC23 [10]	van Assche TCAS-I25 [11]	Timmermans JSSC24 [3]
Topology	DT-LC	DT-LC	DT-LC	CT-LC + SAR	CT-LC + SNN	CT-LC
Number of channels	8	1	16	1	8	1
Technology [nm]	65	40	65	55	40	65
Supply Voltage [V]	0.8	0.5/1	0.7/1.0	1.2	1/0.7	1.2
ADC resolution [bits]	**10**	8	7	4+4	4 - 8	6
Synchronous output	**Y**	Y	Y	N	N	N
Area [mm^2]	0.04	0.012	0.0017 — 0.0029	0.063	0.184 — 0.023	0.0044
Power consumption/channel [μW]	0.1-0.26	0.92-5.38	0.029-0.38	0.44-7	1.27-1.63	0.066-2.8
Bandwidth/channel [kHz]	8	15	8	25	1	20
Peak ENOB (bits)	9.98	10.4	8.2	10	12	9.9
Worst FoM$_W$[a][fJ/conv-step]	**16.1**	131	78.2	171	255	65[e]
Best FoM$_W$[b][fJ/conv-step]	6.2	22	6.1	29.7	199	1.8[e]
Data Compression Ratio (CR)[c]	**94.4%**	70%	90.6%	70%	N/A	92.5%
f_{clksys} / BW[d]	**4x**	1600x	13x	N/A	N/A	N/A

[a] Worst FoM$_W$=$\frac{P_{worst}}{2^{ENOB}\times 2BW}$, where P_{worst} is the power needed to convert a sinusoid input. [b] Best FoM$_W$=$\frac{P_{best}}{2^{ENOB}\times 2BW}$, where P_{best} is the power needed to convert a very sparse input. [c] Based on neural dataset [12], $CR = \frac{D_{conv}-D_{LC}}{D_{conv}}$. [d] This is only applicable to DT-LCADCs, where a system clock is needed for time-synchronization. [e] Re-timing power is not included.

of 94.4% for this dataset. At system level, data rate reduction is very important to achieve ultra low-power application: for example, exploiting to the compression given by the proposed DT-LCADC instead of a Nyquist ADC, up to 57 μW could be saved to transmit the dataset using e.g., a low-energy (3.8 nJ/bit) wireless Bluetooth protocol [14].

The performance of the proposed DT-LCADC is compared in Table I with the relevant state of the art. With an energy per conversion ranging between 6.2 and 16.1 fJ/c.s (depending on the input signals), this work achieves a comparable Walden FoM$_W$ for neural signals and the best overall FoM$_W$ for generic signals, among all reported CT and DT LCADCs. Moreover, the ratio between the maximum and minimum power consumption of this LCADC is the lowest in its class, highlighting its versatility for a wide type of input signals. This feature allows the converter to keep its efficiency in case the signal sparsity would be affected by unwanted interference (e.g., from power lines and motion artefacts) or by intermitting components (like vibrations in tactile sensing). Furthermore, this LCADC attains the highest data Compression Ratio for the analyzed dataset [6] and the lowest needed oversampling compared to other DT-LCADCs. This helps save power and simplifies the clock distribution in large systems.

IV. Conclusion

Unlike SAR converters, DT-LCADCs exploit signal characteristics such as time-sparsity to achieve data compression. However, their power consumption increases significantly with the signal activity, due to need of both, high oversampling and a large number of comparisons to convert fast-changing signals. This in turn limits the advantages and usability of such LCADCs to sparse signals only. To correct this shortcoming, we propose a novel DT-LCADC, fabricated in 65 nm technology, combining the advantages of level-crossing and conventional SAR ADCs. The proposed topology can exploit signal sparsity to achieve data compression while operating at low power, and can accurately convert fast-changing inputs while keeping its energy efficiency. With a Walden FoM$_W$ of 6.2-16.1 fJ/c.s and a compression ratio of 94.4% obtained for a neural signal dataset, the proposed LCADC achieves state-of-the-art performance.

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