A 74-to-100 GHz High-Efficiency Power Amplifier With Interdigitated-Coupled-Four-Line-Based Matching Networks

Xun Bao*, Weiping Wu*†, Zelong Chen*, Yan Wang*, and Lei Zhang*
Email: zhang.lei@tsinghua.edu.cn
*School of Integrated Circuits, Tsinghua University, Beijing, China
†College of Semiconductors, Hunan University, Changsha, China

***Abstract*—This work presents a design methodology for broadband high-efficiency power amplifiers (PA) with interdigitated-coupled-four-line-based (ICFL) matching networks. The coupled line can consider the electrical and magnetic characteristics simultaneously. The proposed ICFL provides a flexible coupling strength to achieve a large bandwidth. Further, the derived synthesizing procedure enables a low design burden. The prototype PA is implemented for 5G backhaul link and radar sensing with a 65nm bulk CMOS technology. Measurement results show that the PA shows a peak power-added efficiency (PAE_{max}) of 21.2% and an operating bandwidth over 74-100GHz with a >14 dBm P_{sat}. It consistently achieves >12dBm P_{1dB} over 74-98 GHz, demonstrating the ability of wideband large-signal operation.**

***Index Terms*—Power amplifier (PA), broadband, efficiency, millimeter-waves (mm-waves).**

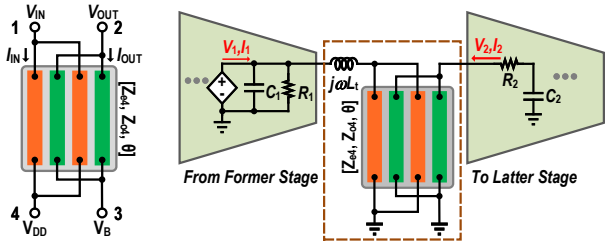
I. Introduction

The increasing demand for high-speed data links and accurate radar sensing has driven the 70/80/90-GHz band to unleash next-generation communication and sensing scenarios [1]–[4]. A power amplifier (PA) is an integral part of these systems, dominating the efficiency and power consumption. With the advantages of low cost and high integration [5], CMOS PAs have become a significant candidate in these applications. However, due to the limited f_T/f_{max}, realizing a wideband yet efficient CMOS PA is still an open challenge.

In order to obtain a broadband PA with decent power gain, a canonical solution is multi-stage architectures. The interstage matching network (IMN), serving for low-loss power transfer and proper DC biasing, plays an essential role in PAs' efficiency and bandwidth. Therefore, an in-depth research on low-loss and broadband IMNs is meaningful. Transformers (XFMR) [6]–[8] and magnetically-coupled resonators (MCR) [9], [10] are typical broadband IMNs. However, for XFMR, adopting simplified lumped models can hardly capture distributed parasitics, limiting the effect of bandwidth extension; for MCR, failing to extract electronic and magnetic parameters simultaneously leads to a strong trade-off between bandwidth, matching loss, and ripple. To remedy these issues, coupled lines have been explored to provide a wideband and low-loss matching [11]–[13]. Nonetheless, under a specific process, the achievable even- and odd-mode characteristic impedances are strongly confined by design rules, limiting the practicability of optimal matching solutions.

This work was supported by the National Key Research and Development Program of China 2024YFF1400200.

Xun Bao and Weiping Wu contributed equally to this work.



(a) (b)

Fig. 1. (a) Matching network model based on interdigitated-coupled-four-line. (b) ICFL used as broadband matching network.

This work presents one solution to these challenges: an interdigitated-coupled-four-line (ICFL) structure used as IMN for a wideband and efficient PA. Advantages are twofold. First, the ICFL allows for a precise consideration of electric and magnetic couplings with three parameters. Secondly, under a given process, the ICFL allows for a greater difference between even- and odd-mode characteristic impedances, enabling a low-loss bandwidth extension. Based on the proposed ICFL, matching equations and the closed-form solution set are derived to guide the synthesis procedure, leading to an optimized PA in bandwidth and efficiency at 70/80/90-GHz bands.

II. ICFL-based Inter-Stage Matching Network Design

To address the design rule restrictions regarding the coupling strength of coupled lines, this work introduces an interdigitated structure. Compared to vertical-coupled lines, the metal thickness and resulting quality factor of horizontal-coupled lines exhibit greater consistency, making the latter more suitable for IMN design [11]. Given the symmetry requirements of interdigitated coupling, a four-line configuration is chosen to demonstrate the proposed interdigitated structure.

A. On-Chip Model of ICFL Structures

Fig. 1(a) shows a four-port model of an ICFL, which can be used for scalable impedance transformation. Its electric and

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} (-\dfrac{j\cot\theta}{Z_p+\cot\theta\cdot\omega L_t}+\dfrac{1}{R_1}+j\omega C_1)^{-1} & \dfrac{Z_m R_1}{(R_1\cdot j\omega C_1+1)\cdot(Z_p+\cot\theta\cdot\omega L_t)-R_1\cdot j\cot\theta} \\ \dfrac{Z_m R_1}{(R_1\cdot j\omega C_1+1)\cdot(Z_p+\cot\theta\cdot\omega L_t)-R_1\cdot j\cot\theta} & \dfrac{(R_1\cdot j\omega C_1+1)\cdot\left[j\tan\theta\left(Z_p^2-Z_m^2\right)+Z_p\cdot j\omega L_t\right]+Z_p R_1}{(R_1\cdot j\omega C_1+1)\cdot(Z_p+\cot\theta\cdot\omega L_t)-R_1\cdot j\cot\theta} \end{bmatrix}\cdot\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (3)$$

magnetic characteristics can be fully expressed by the **Z** matrix (1), which is specified by three parameters: electric length θ, even- and odd-mode characteristic impedance Z_{e4}, Z_{o4}.

$$[\mathbf{Z}] = \begin{bmatrix} -2jZ_p\cot\theta & 2jZ_m\cot\theta & 2jZ_m\csc\theta & -2jZ_p\csc\theta \\ 2jZ_m\cot\theta & -2jZ_p\cot\theta & -2jZ_p\csc\theta & 2jZ_m\csc\theta \\ 2jZ_m\csc\theta & -2jZ_p\csc\theta & -2jZ_p\cot\theta & 2jZ_m\cot\theta \\ -2jZ_p\csc\theta & 2jZ_m\csc\theta & 2jZ_m\cot\theta & -2jZ_p\cot\theta \end{bmatrix} \quad (1)$$

where $Z_p = (Z_{e4}+Z_{o4})/2, Z_m = (Z_{e4}-Z_{o4})/2$. Since the characteristic impedance of the coupled line is decided by both the grounded capacitance and the inter-line coupling, by applying the interdigitated structure, the even- and odd-mode characteristic impedance is tunable to a more significant extent under the specified technology. Ports 1 and 2 work together to receive the signal from the output of the former stage and feed the impedance-transformed one forward to the input of the following stage. Ports 3 and 4 are responsible for power and bias supply, respectively, and virtual ground for the AC case. The two-port matching model can be expressed in the **Z** matrix, as shown in Equation (2).

$$[\mathbf{Z}]_2 = \begin{bmatrix} jZ_p\tan\theta & jZ_m\tan\theta \\ jZ_m\tan\theta & jZ_p\tan\theta \end{bmatrix} \quad (2)$$

B. Optimization Boundary for Broadband PA Stages

To seek for the optimization boundary for broadband PA stages, Fig. 1(b) shows an equivalent half circuit of the ICFL-based IMN, where $(R_1\|C_1)$ represents the output impedance of the former stage, while $(R_2{+}C_2)$ represents the input impedance of the latter stage. A tuning inductor L_t is added to slightly adjust the insertion loss and matching bandwidth.

With $(R_1\|C_1)$ terminating Port 1 and $(R_2{+}C_2)$ terminating Port 2, Fig. 1(b) emerges a two-port circuit of which the **Z**-matrix is shown in Equation (3) at the top of this page. Correspondingly, we define $Z_G = V_2/I_1$ to express the matching performance of the IMN.

$$Z_G \equiv \frac{V_2}{I_1} = \frac{Z_{21}\cdot(R_2+1/j\omega C_2)}{Z_{22}+(R_2+1/j\omega C_2)} \quad (4)$$

where Z_{21} and Z_{22} represents elements in the impedance matrix shown in Equation 3. Since Z_G is a function of Z_{e4}, Z_{o4}, θ, R_1, C_1, R_2, C_2, and L_t, under a given transistor size, the transfer properties of the IMN can be fully expressed by the characteristic of ICFL and the tuning inductor.

C. Design Space Solution of Practical ICFL-based IMNs

Typically, the transistor width of the latter stage is twice that of the former stage for linearity and output power consideration. Therefore, the case with a 48μm/60nm and a 96μm/60nm transistor is chosen as a example for analysis

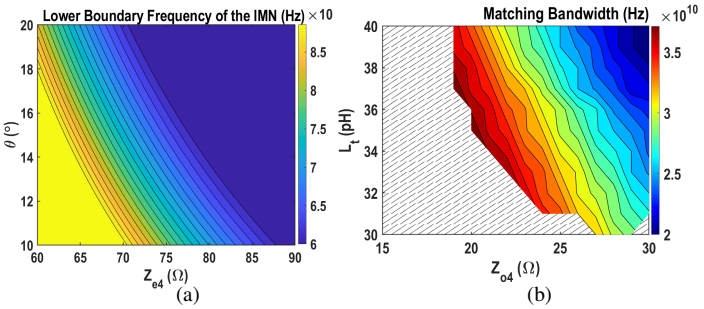


Fig. 2. Co-optimization of (a) the lower boundary frequency as a function of Z_{e4} and θ and (b) the matching bandwidth as a function of Z_{o4} and L_t.

and calculation hereafter. Under this condition, $(R_1\|C_1)$ and $(R_2{+}C_2)$ are (93.5Ω‖58.4fF) and (1.95Ω+164fF), respectively.

It is worth mentioning that the following relationships should be satisfied to obtain a physically meaningful solution:

$$Z_{e4} > Z_{o4} > 0 \Leftrightarrow Z_p > Z_m > 0 \quad (5)$$

For a specified purpose of frequency band, L_t is ignored at the beginning of the design phase for simplicity. This is reasonable since L_t has little effect on the lower boundary frequency of IMN. Hence, Z_G is simplified to Equation (6).

By analyzing the frequency response of Z_G shown in Equation (6), the lower boundary frequency of the IMN is approximately a function of Z_{e4} and θ, as shown in Fig. 2(a). Based on the contour in Fig. 2(a), a Z_{e4} of 75Ω and a θ of 15° gives valuable insight for further optimization.

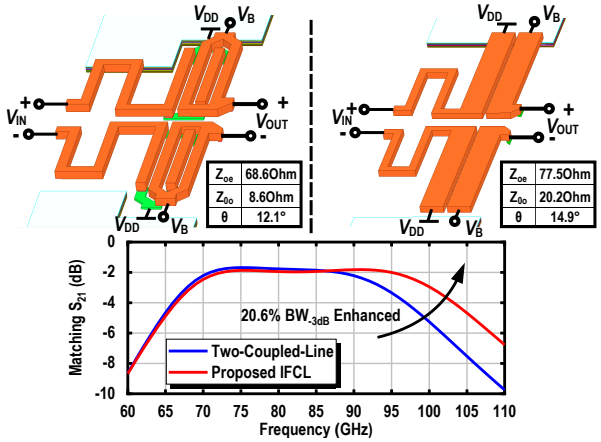


Fig. 3. Matching performances of two-coupled-line and the proposed ICFL.

$$Z_{G0} = \frac{\dfrac{Z_m R_1\,(R_2+1/j\omega C_2)}{(j\omega C_1R_1+1)\cdot Z_p - R_1\cdot j\cot\theta}}{\dfrac{(j\omega C_1R_1+1)\cdot\left[j\tan\theta\left(Z_p^2-Z_m^2\right)\right]+Z_pR_1}{(j\omega C_1R_1+1)\cdot Z_p - R_1\cdot j\cot\theta}} + R_2 + \frac{1}{j\omega C_2} \quad (6)$$

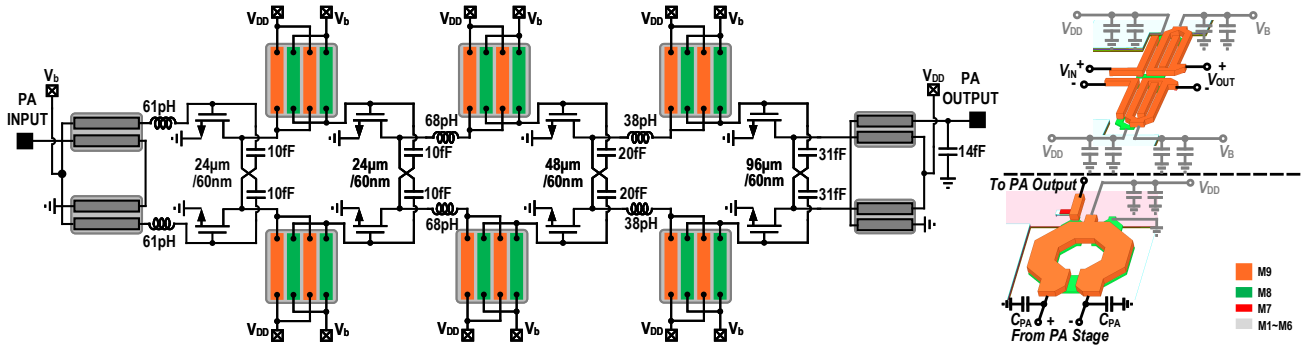


Fig. 4. Schematic of the designed PA, and 3D EM models of key passive components.

Then the matching bandwidth as a function of Z_{o4} and L_t is derived based on Equation (4). When imposing the boundary condition on matching losses, a contour map of the -1dB matching bandwidth is plotted in Fig. 2(b), where the slash-filled portion represents the range where the boundary condition is not satisfied. It can be shown that a smaller Z_{o4} and an appropriate L_t help broaden the matching bandwidth. Therefore, the ICFL-based IMN, with a larger tuning range of the difference between even- and odd-mode characteristic impedances, can help get closer to the optimal solution set and thus realize better matching performances. Meanwhile, the trade-off between bandwidth, matching efficiency, and ripple, should be judiciously considered.

III. Broadband Efficient PA with the Proposed Technique

An IMN between stages of 48μm/60nm and 96μm/60nm, is designed with the proposed ICFL-based matching technique, shown in the upper right part in Fig. 3. The active transistors are biased and powered from the ends of ICFLs. With the proposed ICFL and the synthesizing procedure, the matching bandwidth can be enhanced by 20.6% compared to its two-coupled-line counterpart, as shown in Fig. 3.

A prototype four-stage differential PA is designed under 65-nm bulk CMOS technology, whose schematic and part of the implementations of passive structures are depicted in Fig. 4. The capacitive neutralization technique is applied in each stage to absorb C_{GD} of transistors, improving the reverse isolation. Further, transistor sizes are approximately twice as the previous stages for optimal linearity and output power.

The output network is achieved by a distributed balun shown in the lower right part in Fig. 4, which has been proven effective in broadband operation [12]. Both input and output baluns serve as a single-ended/differential conversion.

IV. Measurement Results

The chip micrograph is shown in Fig. 5, which has a core area of 0.4×0.21mm^2. The measured small-signal performance is shown in Fig. 6, where the peak gain is 24.6dB, with a -3dB-bandwidth from 74.9-93.8GHz. The S_{11} and S_{22} are below -8dB over the whole band, and the S_{12} is below -40dB.

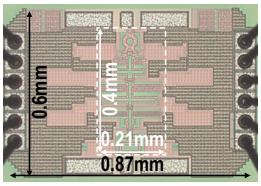


Fig. 5. Chip micrograph.

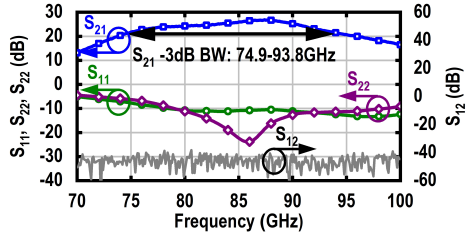


Fig. 6. Measured small-signal S-parameters.

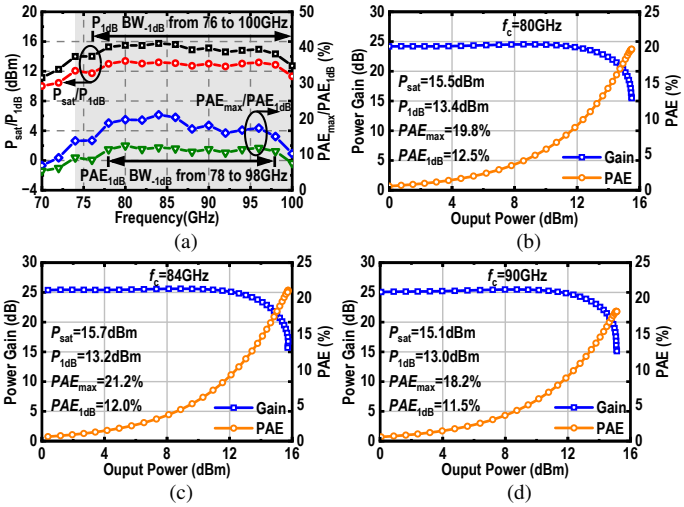


Fig. 7. (a) Measured large-signal performances versus frequency, and large-signal performances vs output power at (b)80GHz, (C)84GHz, (d)90GHz.

As shown in Fig. 7, the PA is further characterized by large-signal continuous-wave (CW) measurement. The PA continuously achieves >14-dBm saturated output power (P_{sat}) over 74–98 GHz, with a 3-dB P_{out} fluctuation from 74-100GHz. Further, the PA shows a flat 1-dB compression point (P_{1dB}) over 74-98 GHz, and a -1-dB bandwidth of PAE at P1dB (PAE_{1dB}) of over 74–100GHz, demonstrating wideband large-signal operation. At 84GHz, the PA achieves 15.7-dBm P_{sat}

TABLE I

PERFORMANCE COMPARISON WITH STATE-OF-THE-ARTS

	This work	[2]TCASII'23	[3]IMS'20	[16]IMS'20	[4]TMTT'21	[6]JSSC'22	[17]JSSC'18	[8]MWTL'23
Technology	65nm CMOS	28nm CMOS	55nm CMOS	22nm FinFET	28nm FD-SOI CMOS	65nm CMOS	0.13μm SiGe BiCMOS	65nm CMOS
Architecture	4-stage CS 1 way	3-stage CS 2-ways	2-stage CA 2 ways	1-stage CS 1 way	2-stage CS 1-stage CA 1 way	4-stage CS 4 ways	2-stage CE 1 way (S.E.)	3-stage CS 1 way
Supply (V)	1.2	0.9	2.5	2.1	1.0	1.2	1.4	1.2
Gain (dB)	24.6	23.6	16.1	11.7	26.5	29.3	7.5	20.0
GBW(GHz)	333	244	102	104	68	117	14	60
S_{21} BW_{-3dB} (GHz)	74.9-93.8 (22.6%)	72.9-89 (19.9%)	73-89 (19.8%)	72-99 (31.6%)	75.4-78.6 (4.2%)	82.7-86.7 (4.8%)	92-98 (6.3%)	92.5-98.5 (6.3%)
P_{1dB} BW_{-1dB} (GHz)	76-100 (28.6%)	NA	NA	70-75 (6.8%)	NA	83.4-88.8 (6.3%)$^{\$}$	NA	NA
Frequency (GHz)	84	81	80	73	77	86.4	95	95
P_{sat} (dBm)	15.7	12.15	18	14.6	13.5	19.1	7.5$^{\$}$	13.0
P_{sat} /Way (dBm)	15.7	12.15	15	14.6	13.5	13.1	7.5	13.0
P_{1dB} (dBm)	13.4	NA	12.9	12.1	10$^{\$}$	16.2	3$^{\$}$	12.8
PAE_{max} (%)	21.2	12	12.6	18.6	14.5	8.6	18.5$^{\$}$	21.1
PAE_{1dB} (%)	12.0	NA	5$^{\$}$	13.6	7$^{\$}$	4.6$^{\$}$	11.5$^{\$}$	20$^{\$}$
Core Area (mm^2)	0.10	0.18	0.21	0.01	0.14	0.17	0.16	0.11
FoM†	92.05	84.71	83.27	77.63	89.34	96.23	67.23	85.8

†FoM=P_{sat}(dBm)+Gain(dB)+20logf_0(GHz)+10logPAE_{max}(%)

CS: Common source. CA: Cascode. CE: Common emitter. S.E: Single-ended.

$^{\$}$ Graphically estimated.

$^{\#}$ Simulated Results.

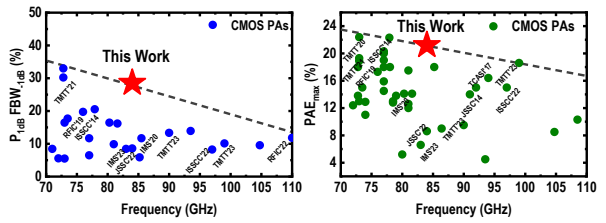


Fig. 8. Performance comparison of P_{1dB} FBW_{-1dB} and PAE with state-of-the-arts.

and 13.2-dBm P_{1dB} with a 21.2% PAE_{max} and 12.0% PAE_{1dB}.

Table I summarizes and compares the PA's performance with the state-of-the-art using International Technology Roadmap for Semiconductors (ITRS) figure of merit (FOM) [14] [15]. With the discussed technique, the proposed PA achieves a high output power and PAE, with the widest P_{1dB} fractional bandwidth (FBW) of 28.6%, which supports wideband large-signal operation.

V. CONCLUSION

This work presents an ICFL-based IMN for broadband PAs at 70/80/90-GHz bands. The proposed structure's larger achievable difference between even and odd-mode characteristic impedances contributes to a low-loss and broadband matching network solution, thus enabling high-efficiency PA with the ability of broadband large-signal operation. Closed-form design equations and procedures are analyzed thoroughly.

As a proof of concept, a prototype PA covering the bandwidth over 74-100GHz is designed and implemented. The prototype PA achieves superior broadband operation, high efficiency, and competitive FoM, demonstrating the effectiveness of the proposed ICFL-based design technique. In Fig. 8, the competitive performance of the FBW_{-1dB} of P_{1dB} and PAE versus CMOS PAs at comparable frequency bands is demonstrated visually. The prototype PA achieves superior broadband operation, high efficiency, and competitive FoM, demonstrating the effectiveness of the proposed ICFL-based design technique.

REFERENCES

[1] "Modernizing and Expanding Access to the 70/80/90 GHz Bands," 2020-05-19. [Online]. Available: https://docs.fcc.gov/public/attachments/DOC-364458A1.pdf

[2] D. Pan, Z. Duan, Y. Wang, C. Wang, Y. Li, L. Sun, and L. Cheng, "A 77-GHz Power Amplifier With Digital Power Control for Multi-Mode Automotive Radar in 28-nm Bulk CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 875–879, 2023.

[3] Y. Xue, C. Shi, G. Chen, J. Chen, and R. Zhang, "Two W-Band Wideband CMOS mmW PAs for Automotive Radar Transceivers," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 1109–1112.

[4] C. Nocera, G. Papotto, A. Cavarra, E. Ragonese, and G. Palmisano, "A 13.5-dBm 1-V Power Amplifier for W-Band Automotive Radar Applications in 28-nm FD-SOI CMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 3, pp. 1654–1660, 2021.

[5] Y.-H. Hsiao, *et al*, "A 77-GHz 2T6R Transceiver With Injection-Lock Frequency Sextupler Using 65-nm CMOS for Automotive Radar System Application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 10, pp. 3031–3048, 2016.

[6] V.-S. Trinh and J.-D. Park, "An 85-GHz Power Amplifier Utilizing a Transformer-Based Power Combiner Operating Beyond the Self-Resonance Frequency," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 3, pp. 882–891, 2022.

[7] G. Park, S. Park, and S. Jeon, "A High-Efficiency E-Band Power Amplifier With Optimized Output Matching Network in a 28-nm Bulk CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 3, pp. 1032–1036, 2024.

[8] W. Wu, R. Chen, S. Chen, J. Wang, L. Chen, L. Zhang, and Y. Wang, "A Compact W-Band Power Amplifier With a Peak PAE of 21.1% in 65-nm CMOS Technology," *IEEE Microwave and Wireless Technology Letters*, vol. 33, no. 6, pp. 703–706, 2023.

[9] M. Vigilante and P. Reynaert, "On the Design of Wideband Transformer-Based Fourth Order Matching Networks for *E* -Band Receivers in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, 2017.

[10] H. Jia, C. C. Prawoto, B. Chi, Z. Wang, and C. P. Yue, "A Full Ka-Band Power Amplifier With 32.9% PAE and 15.3-dBm Power in 65-nm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2657–2668, 2018.

[11] X. Huang, H. Jia, W. Deng, Z. Wang, and B. Chi, "A Compact E-Band Load-Modulation Balanced Power Amplifier in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 10, pp. 3172–3182, 2024.

[12] F. Wang and H. Wang, "A Broadband Linear Ultra-Compact mm-Wave Power Amplifier With Distributed-Balun Output Network: Analysis and Design," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2308–2323, Aug 2021.

[13] W. Wu, X. Bao, S. Chen, Y. Wang, and L. Zhang, "32.4 A 67.8-to-108.2GHz Power Amplifier with a Three-Coupled-Line-Based Complementary-Gain-Boosting Technique Achieving 442GHz GBW and 23.1% peak PAE," in *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, vol. 67, 2024, pp. 526–528.

[14] "International Technology Roadmap for Semiconductors," 2001-01-31. [Online]. Available: https://semiconductors.org/wp-content/uploads/2018/08/2001SysDrivers.pdf

[15] Z. Zong, X. Tang, K. Khalaf, D. Yan, G. Mangraviti, J. Nguyen, Y. Liu, and P. Wambacq, "A 28-GHz SOI-CMOS Doherty Power Amplifier With a Compact Transformer-Based Output Combiner," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 6, pp. 2795–2808, 2021.

[16] Q. Yu, Y.-S. Yeh, J. Garret, J. Koo, S. Morarka, S. Rami, G. Liu, and H.-J. Lee, "An E-Band Power Amplifier Using High Power RF Device with Hybrid Work Function and Oxide Thickness in 22nm Low-Power FinFET," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 999–1002.

[17] S. Afroz, H. Kim, and K.-J. Koh, "Power-Efficient *W* -Band (92–98 GHz) Phased-Array Transmit and Receive Elements With Quadrature-Hybrid-Based Passive Phase Interpolator," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1678–1693, 2018.