

A Type-I Reference Sampling PLL with Locking Region Tracking Achieving -261.8 dB FoM_{jitter, N} and 7% Jitter Variation over PVT

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Abstract—This work presents a type-I differential double-edge reference-sampling ring-oscillator based phase-locked loop (DDE-RSPLL) utilizing locking region tracking (LRT) to achieve low jitter over process, voltage and temperature (PVT) variations. The differential double-edge sampling technique is used to widen loop bandwidth (BW_{Loop}) and suppress the phase noise of the ring oscillator. The LRT is introduced to maintain the sampling points in the high-gain region to eliminate phase detection gain (K_{PD}) variation and maintain high K_{PD} and wide BW_{Loop} over PVT variations. The prototype PLL implemented in 65-nm CMOS achieves 426 fs jitter_{RMS} and consumes only 1.42 mW, corresponding to a -245.8 dB FoM_{jitter} and a -261.8 dB FoM_{jitter, N}. Over a temperature span of -45 °C to 105 °C and supply voltage variations of $\pm 15\%$ (i.e., 0.85 V to 1.15 V), the measured jitter_{RMS} deviation remains within 7%.

Keywords—Type-I Phase-Locked Loop, Reference Sampling, Loop Bandwidth, Phase Detection Gain, PVT Robustness.

I. INTRODUCTION

Ring oscillator (RO) based phase-locked loops (PLLs) have been widely adopted for both wireless and wireline communications due to their process mobility, compact area and wide frequency tuning range (FTR). However, suppressing the inherent RO phase noise (PN) necessitates a wide loop bandwidth (BW_{Loop}). Multiplying Delay-Locked Loops (MDLLs) can effectively realize a wide BW_{Loop} by periodical phase realignment, but they suffer from the reference spur arising from imperfect phase alignment [1]. Sub-sampling PLLs, despite their wide BW_{Loop} potential, suffer from high-power reference buffers and limited lock-in range [2]. Alternatively, as depicted in Fig. 1, reference sampling PLLs (RSPLLs) show better lock-in robustness and eliminate the reference buffer to save power. However, they can induce high power consumption and large area due to the required G_m and capacitors for the type-II configurations [3]. The type-I RSPLL achieves wider BW_{Loop} with compact size. However, its phase detection gain (K_{PD}) is related to the locking points location, which varies with process, voltage, and temperature (PVT) fluctuation. The K_{PD} variation results in corresponding variation in BW_{Loop} , which causes the PLL jitter degradation and necessitates off-chip calibrations [4]. To address these limitations, this work proposes a type-I differential double-edge reference sampling phase-locked loop (DDE-RSPLL) to further increase the BW_{Loop} to approximately $0.5 F_{REF}$. The locking region tracking (LRT)

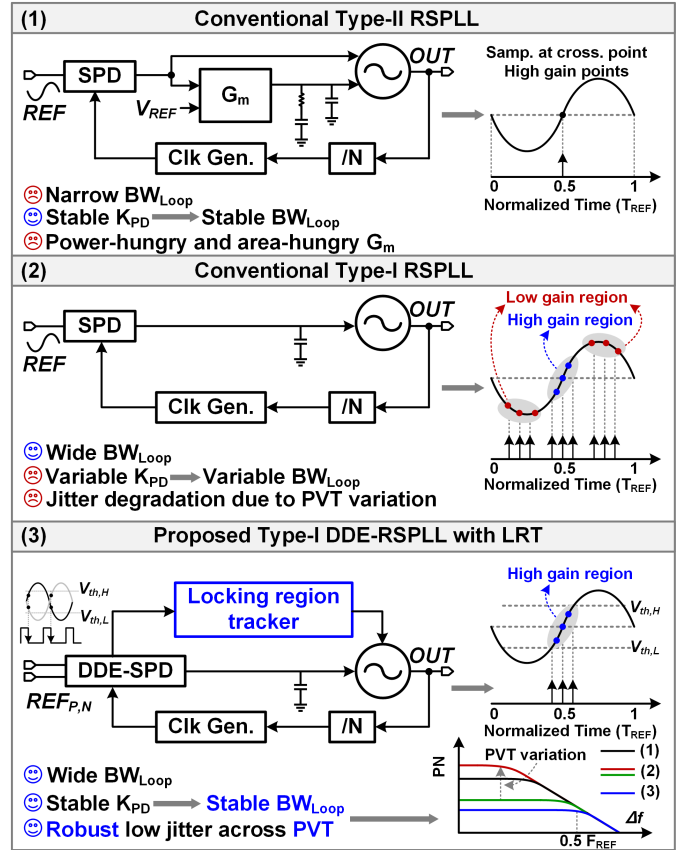


Fig. 1. Comparison with the conventional type-I and type-II RSPLL.

is implemented to dynamically calibrate the sampling points within the high-gain region, thereby maintaining high K_{PD} , wide BW_{Loop} , robust locking, and low jitter over PVT variations.

II. PROPOSED DDE-RSPLL WITH LRT

A. Architecture of the proposed DDE-RSPLL

Fig. 2 shows the architecture of the proposed differential type-I RSPLL. The differential double-edge sampling phase detector (DDE-SPD) samples the sinusoidal reference (REF) REF_P and REF_N at both rising and falling edges, generating the controlling voltage pair $V_{C,P}$ and $V_{C,N}$, which directly

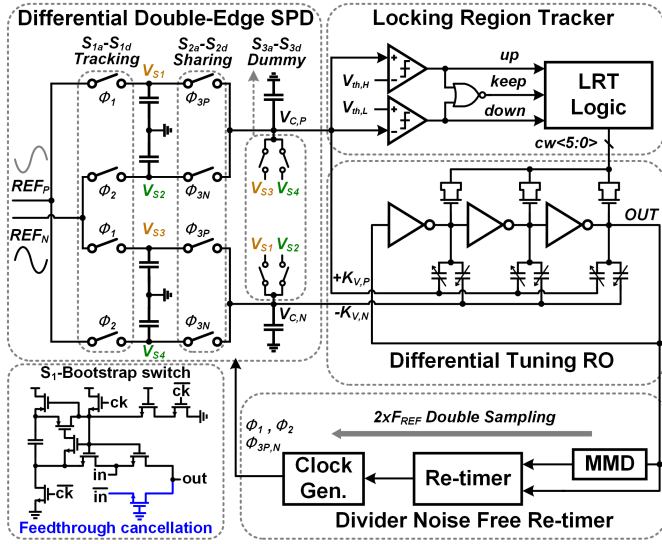


Fig. 2. The architecture of the proposed DDE-RSPLL with LRT.

adjust the RO frequency. Unlike the conventional single-ended approach that uses G_m to realize sampled voltage summation by differential-to-single-ended (D2S) conversion [5], the proposed differential operation avoids power and noise penalty from the active voltage-domain D2S. This configuration obtains $2x$ enhancement in both K_{PD} and RO frequency tuning gain $K_V = K_{V,P} + K_{V,N}$. Furthermore, the double-edge operation enables an equivalent $2x$ increase in the sampling rate, which suppresses the RO PN significantly. The first sampling switches (S_{1a} - S_{1d}) are equipped with bootstrap switches, and the dummy switch is added to cancel the REF feedthrough. The sampling clocks Φ_1 , Φ_2 and Φ_{3p}/Φ_{3n} are sourced from a multi-mode divider (MMD), where a re-timer is added after the last stage to remove the accumulated delay. The locking point is monitored and adjusted by the proposed LRT. When $V_{C,P}$ settles outside the region constrained by $V_{th,H}$ and $V_{th,L}$, the LRT logic adjusts $V_{C,P}$ by shifting discrete-controlled capacitor bank in the RO via the control word $CW \langle 5:0 \rangle$.

B. Principle of DDE-SPD

Fig. 3 illustrates the principle of proposed DDE-SPD. In a conventional type-I Ping-Pong SPD, the sampled voltage V_S modulates the RO frequency directly. The sinusoidal reference signal can directly couple through the parasitic capacitance of switches (C_{para1} and C_{para2}) to the RO, thereby degrading the spur performance. In the proposed DDE-SPD, the REF feedthrough is cancelled by dummy switches, which provides effective spur suppression. During the $0 - \pi$ phase interval, the voltages V_{S1} and V_{S3} are respectively tracked to the REF_P and REF_N by the switches S_{1a} and S_{1c} , and the voltages V_{S2} and V_{S4} are respectively shared to the $V_{C,P}$ and $V_{C,N}$ by the switches S_{2b} and S_{2d} . The REF_P and REF_N will couple to $V_{C,P}$ and $V_{C,N}$ through the parasitic capacitance of S_{2a} and S_{2c} ($C_{para,S2}$), separately. To mitigate this issue, the V_{S1} and V_{S3} are connected to $V_{C,N}$ and $V_{C,P}$ via the perpetually open dummy switches S_{3b} and S_{3a} (identical in size to S_{2a} - S_{2d}). The feedthrough from REF_P and REF_N will

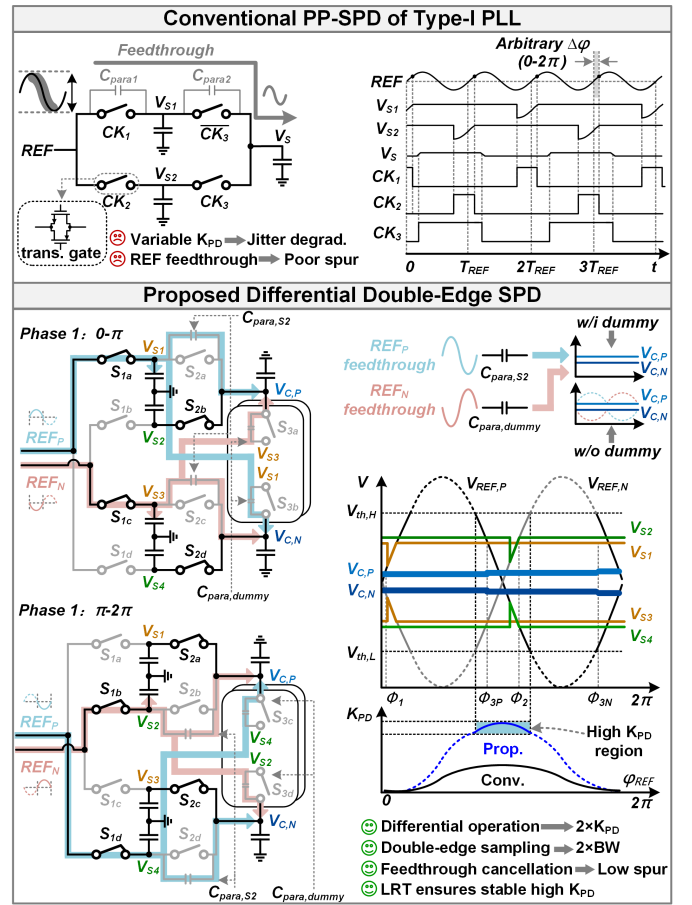


Fig. 3. Principle of conventional SPD and proposed differential double-edge SPD.

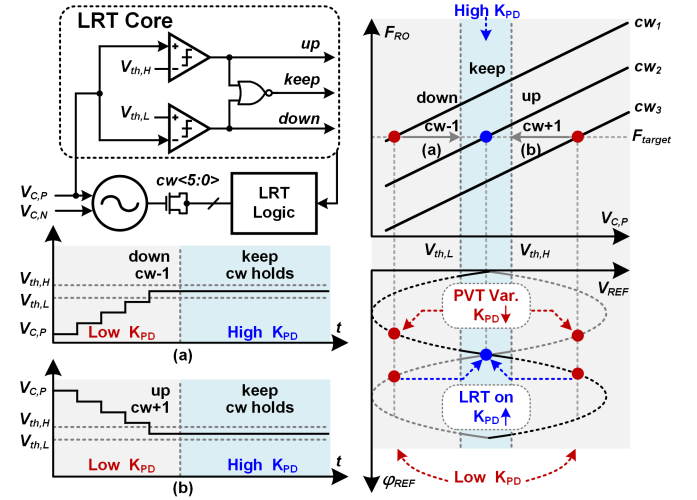


Fig. 4. Operation details of the proposed LRT.

be cancelled through the same parasitic capacitance ($C_{para,S2}$ and $C_{para,dummy}$), providing effective REF spur mitigation. The same mechanism applies to the $\pi - 2\pi$ phase interval. The implementation of dummy switches enables spur mitigation with negligible area penalty and uncomplicated configuration.

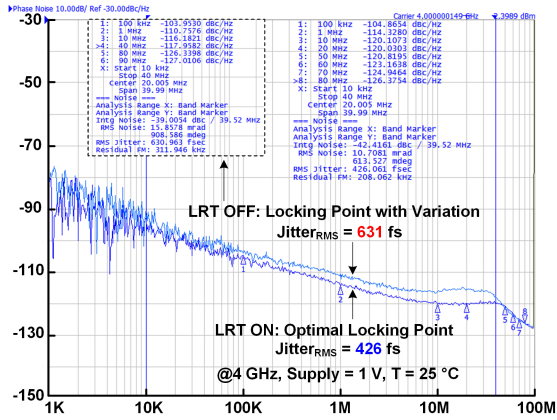


Fig. 5. Measured PLL phase noise at 4 GHz with the LRT off (locking point with variation, light blue trace) and on (optimal locking point, dark blue trace).

TABLE I
JITTER VARIATION WITH LRT OVER PVT

	Process (corners)*	Supply voltage	Temperature
Jitter variation	<±5%	<±7%	<±6%

*Post-layout simulation results

C. Details of LRT

In a conventional type-I RSPLL, the RO controlling voltage can fall at any position within the reference amplitude range due to PVT variations, leading to fluctuations in both K_{PD} and BW_{Loop} . Yet even then, significant variations may still occur across different output frequencies. To address these challenges, this work incorporates the LRT that ensures a stable and high K_{PD} by monitoring the sampled voltage $V_{C,P}$ and maintaining it within $V_{th,H}$ and $V_{th,L}$. Fig. 4 depicts the operation details of the proposed LRT that adjust CW according to three signals *up*, *down* and *keep*, output from two low-frequency comparators. When $V_{C,P}$ surpasses $V_{th,H}$, it signifies that the center frequency corresponding to the current CW is too low. In response, the LRT increments CW by 1, causing $V_{C,P}$ to settle to a lower voltage, and vice versa. After a series of LRT iterations, the loop stabilizes with $V_{C,P}$ residing within the high-gain region then signal *keep* grows up to hold CW without disrupting the type-I loop. In this way, the DDE-RSPLL benefits from a consistently high K_{PD} , attributed to the steep slope of the reference waveform, and the proposed LRT ensures the robustness against PVT variations.

III. MEASUREMENT RESULTS

The proposed DDE-RSPLL, fabricated in a 65-nm CMOS process, occupies an active area of 0.033 mm^2 as shown in Fig. 8(c). As shown in Fig. 5, when the LRT is off, the $jitter_{RMS}$ measures 631 fs at 4 GHz, indicating a non-ideal locking point that PVT variations could cause. With the LRT enabled, it drops significantly to 426 fs. Three chips are measured to illustrate the robustness. As depicted in Fig. 6(a) and (b), over the temperature range of $-45 \text{ }^\circ\text{C}$ to $105 \text{ }^\circ\text{C}$ and the supply voltage range of 0.85 V to 1.15 V, the maximum $jitter_{RMS}$

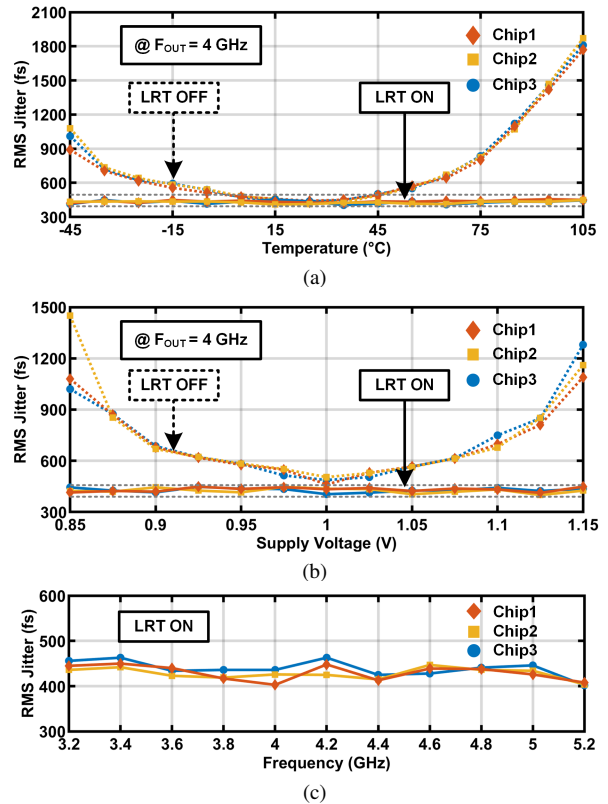


Fig. 6. Measured jitter variation with LRT on/off across (a) temperature, (b) supply voltage and (c) frequency.

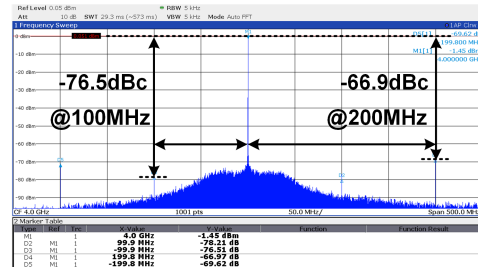


Fig. 7. Measured PLL spectrum at 4 GHz.

exceeds 1.4 ps without the LRT, while the $jitter_{RMS}$ variation keeps under 50 fs with the LRT. The $jitter_{RMS}$ variation is kept below 7% over PVT fluctuations with the LRT. As depicted in Fig. 6(c), the $jitter_{RMS}$ variation from 3.2 GHz to 5.2 GHz remains under 60 fs with the LRT. At 4 GHz, the power consumption is 1.42 mW, equating to a $-245.8 \text{ dB FoM}_{jitter}$ and a power efficiency of 0.355 mW/GHz . With a 100 MHz reference, the $FoM_{jitter,N}$ reaches -261.8 dB . Fig. 7 shows that measured reference spurs are -76.5 dBc and -66.9 dBc at 100 MHz and 200 MHz, respectively. Table-II and Fig. 8(a), (b) summarize and compare the performance of the proposed RSPLL with the state-of-the-art PLLs. The extended BW_{Loop} enables the proposed RO-based DDE-RSPLL achieves comparable FoM_{jitter} to LC-based PLLs, while maintaining better power efficiency, compact area and PVT robustness.

TABLE II
COMPARISON OF STATE-OF-THE-ART PLLS

	This work	ISSCC'24 Y. Huang [6]	TCAS-I'21 Z. Yang [4]	VLSI'24 D. Park [1]	CICC'24 J. Yang [7]	JSSC'21 J. Du [8]
Architecture	Type-I RSPLL	Type-II RSPLL	Type-I RSPLL	MDLL	Type-II RSPLL	Type-II RSPLL
Oscillator Type	Ring	Ring	Ring	Ring	LC	LC
F _{REF} (MHz)	100	100	103	250	100	48
Frequency Tuning Range (GHz)	3.2-5.2	5.6-7.8	2.6-4.2	4.0-5.0	6.0-6.9	1.8-2.3
RMS Jitter (fs)	426	220	440	94	99	414
Power (mW)	1.42	16.47	3.3	13.3	4.6	1.15
REF Spur (dBc)	-76.5@1x _{FREF} , -66.9@2x _{FREF}	-74.2	-63.9	-54	-71.6	-72
Power Efficiency (mW/GHz)	0.355	2.495	1.001	3.325	0.708	0.500
*FoM _{Jitter} (dB)	-245.8	-241.0	-241.9	-249.3	-253.5	-247.0
**FoM _{Jitter, N} (dB)	-261.8	-259.2	-257.0	-261.3	-271.6	-263.8
Active Area (mm ²)	0.033	0.027	0.003	0.045	0.150	0.240
Measurement over (P ^{***})VT?	Yes (-45 °C to 105 °C, ±15% V _{DD})	No	No	No	No	No

*FoM_{Jitter}=10log₁₀(Jitter_{RMS}² · Power), **FoM_{Jitter, N}=10log₁₀(Jitter_{RMS}² · Power/N), ***Verified by post-layout simulation.

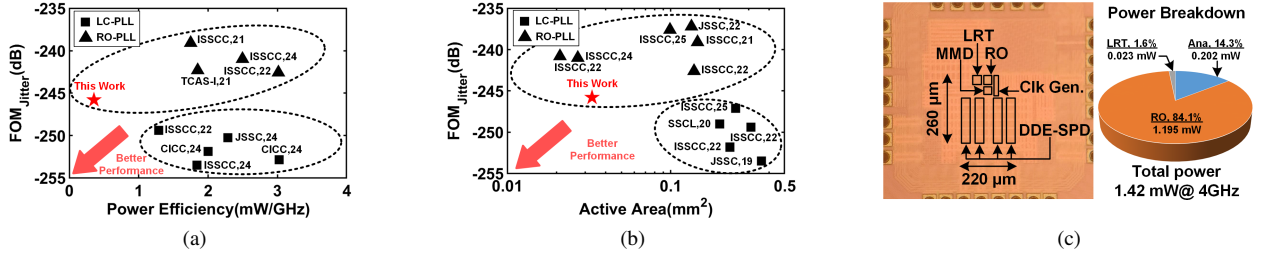


Fig. 8. (a), (b) Performance comparison with the state-of-the-art PLLs. (c) Die micrograph and power breakdown.

IV. CONCLUSION

This work proposes a type-I DDE-RSPLL featuring a stable high K_{PD} over PVT variations. The stable high K_{PD} maintained by the proposed LRT, together with differential and double-edge reference sampling, widens the BW_{Loop} and effectively suppresses the PN of RO. The prototyped 65-nm type-I DDE-RSPLL is measured to deliver competitive performance: 1.42 mW power consumption, 426 fs jitter_{RMS}, -76.5 dBc REF spur, -245.8 dB FoM_{Jitter} and -261.8 dB FoM_{Jitter, N}. The jitter_{RMS} variation is kept below 7% over PVT variations, showing robust locking and noise suppression.

ACKNOWLEDGMENT

This work was supported by the STI2030-Major Projects (2021ZD0202202 and 2021ZD0202202), the Science and Technology Commission of Shanghai Municipality (2021ZD0202202). Corresponding author: Liangjian Lyu.

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