A 20 GS/s 46 dB SNDR 16x Time-Interleaved Pipelined-SAR ADC Using Bulk Calibration for Comparator Offset and Bandwidth Mismatch

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***Abstract*—This paper presents a high-speed 16× time-interleaved (TI) ADC in 22 nm FDSOI CMOS, featuring a 4× TI front-end (FE) sampler with on-chip time-skew and bandwidth mismatch calibration. The FE track-and-hold is isolated by a highly linear push-pull source follower, achieving 16.3 GHz bandwidth and sampling rates up to 28 GS/s. TI time-skew and first-order bandwidth mismatches are estimated off-chip and corrected via capacitive DAC and DAC-based bulk-node tuning, improving SFDR & SNDR by up to 21 dB & 11 dB, respectively. Each of the 16 Pipelined-SAR lanes uses a 3-stage 4/3/4-bit architecture, achieving 47.5 to 44 dB SNDR at 0.94 to 1.75 GS/s. A multi-comparator SAR design enables 0.5 mV-accurate offset calibration by tuning the bulk-node, improving SNR/SNDR by up to 13 dB to 48.5 / 46 dB (1.25 GS/s lane speed) across multiple dies. The TI-ADC maintains 42.4 / 38.8 dB SNDR at Nyquist for $f_s = 20 / 28$ GS/s while consuming 281 / 385 mW from triple supplies (1.2 V/0.9 V/–0.6 V), including input FE and reference blocks. Schreier & Walden FoMs at Nyquist reach 147.9 / 144.4 dB and 130 / 193 fJ/c-s at $f_s = 20 / 28$ GS/s, respectively.**

***Index Terms*—Time-Interleaving, ADC, Pipelined-SAR, mismatch calibration, 22nm FDSOI**

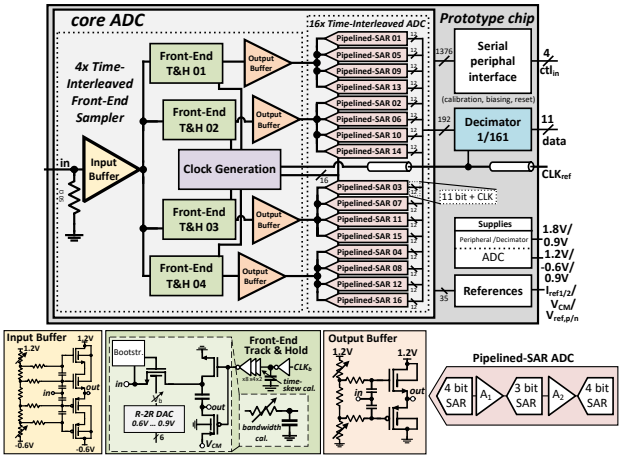

Fig. 1. 16xTI ADC chip architecture with 4x FE T&H

I. Introduction

Multi-gigasample analog-to-digital converters (ADCs) are critical components and bottlenecks in systems requiring high accuracy, speed, and bandwidth, such as optical communications, sensing, instrumentation, and future wireless technologies like 6G. To support e.g. >256-QAM and bandwidths ≥10 GHz in the D-band for 100 Gb/s links, ADCs with >7 ENOB at ≥ 20 GS/s are required. For such demanding metrics, time-interleaved (TI) Successive Approximation Register (SAR) or Pipelined-SAR (PI-SAR) architectures offer the best performance-to-efficiency trade-off. While SAR ADCs are efficient beyond 8-bit resolution up to ≈1 GS/s, higher speeds require pipelining and multi-comparator (loop-unrolled) designs. High interleaving factors (e.g., ≥ 32) ease single-lane speed but increase system complexity, limiting analog front-end (FE) bandwidth due to capacitive loading, shorter sampling windows, and complex clocking. A 16-lane PI-SAR topology provides a good trade-off at ≥ 20 GS/s. High TI performance also demands a linear analog FE sampler with mismatch calibration. Time-skew between lanes limits dynamic range at GS/s rates [1], while bandwidth mismatch degrades performance near the input bandwidth point. The proposed ADC employs a buffered 4× TI FE with mixed-signal calibration for sampling phase and first-order bandwidth mismatch via transistor-bulk modulation, followed by 4×4 2nd-level buffered Sub-ADCs (as shown in Fig. 1). Each Sub-ADC uses a three-stage PI-SAR topology with open-loop amplifiers and multi-comparator conversion, achieving 11-bit resolution at up to 1.75 GS/s. Comparator offsets are mitigated via bulk-node control, enabling >7 ENOB up to 1.75 GS/s per Sub-ADC and resulting in 28 GS/s for the TI-ADC.

II. Design

A. Front-End T&H and Clock Generation

The schematic of the 4× TI FE sampler is shown in Fig. 1. A stacked push-pull class-AB source follower (SF) with extended supplies (1.2 V / –0.6 V) isolates the 4 × track-and-hold (T&H) circuits [1]. This enables a measured dynamic range of <–53 dBc HD3 at $V_{\mathrm{in}} = 1\ V_{\mathrm{pp,diff}}$ up to 16 GHz, while suppressing kickback between T&Hs and supporting 100 Ω differential input termination. Each T&H uses bottom-plate sampling, while the bootstrapped top-plate switch includes a 6-bit bulk-modulated DAC (0.6 – 0.9 V) to tune its on-resistance and thereby the 3 dB bandwidth, effectively allowing first-order bandwidth mismatch calibration. This is enabled by the forward body-biasing capability of the 22 nm FDSOI technology. A multi-phase clock generator buffers a reference sine (≤ 28 GHz), generating 4 sampling phases, each tunable via a 7-bit capacitive DAC (CDAC) for time-skew calibration

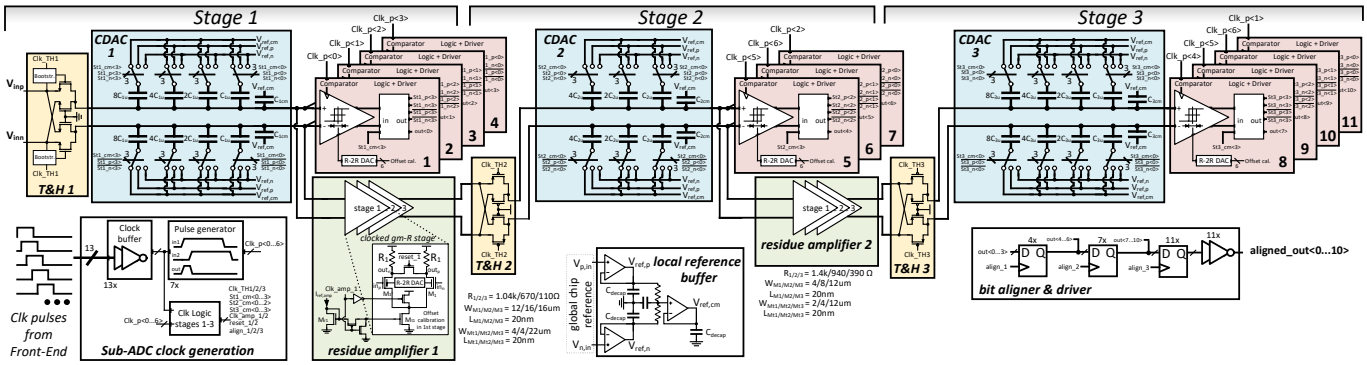

Fig. 2. Schematic Diagram of the proposed 3 stage Pipelined-SAR ADC

with <25 fs resolution, improving dynamic range by up to 16 dB. A second, simplified SF buffer (without stacked devices or negative supply) follows each T&H, driving 4 PI-SAR ADCs and mitigating kickback. As shown in [1], this FE achieves a SNDR of +44 dB SNDR at 22 GS/s up to Nyquist.

B. Pipelined-SAR Design

To balance resolution, speed, and power, the proposed PI-SAR ADC employs 3 SAR stages and 2 residue amplifiers (RA). The 1st and 3rd stages resolve 4 b, while the 2nd resolves 3 b due to two amplification phases within one clock cycle. For the residue amplification, various amplifier topologies have been proposed [2]; here, a 3-stage open-loop design with cascaded common-source (CS) stages and resistor loads is chosen for fast settling, improved linearity, and common-mode stability. This, however, increases area, power, and PVT sensitivity. The latter is mitigated by digital background detection adjusting an off-chip reference current. Power is saved by enabling the amplifiers only during their operation. To maximize conversion speed, a parallel comparator scheme, similar to loop-unrolled SAR ADCs, is used, assigning one comparator per bit decision. This removes reset and MUX delays, enabling up to 1.75 GS/s lane speed without additional power. To maintain consistent RA gain, amplification occurs in a fixed time window ($\approx 30\,\%$ of T_s), requiring synchronous comparator clocking. A single ADC lane is shown in Fig. 2.

1) T&H and CDAC: The 1st stage T&H uses bootstrapped top-plate switches, while the 2nd and 3rd stages use directly clocked PMOS switches, benefiting from relaxed linearity and capacitor mismatch constraints due to interstage gain. The CDAC uses a V_cm-based switching scheme, maintaining constant common-mode voltage. The 1st to 3rd stage CDACs have total capacitances of 180 fF, 92 fF and 42 fF, respectively.

2) Sub-ADC Clocking: Within the FE sampler, a single reference sine at f_s ($\leq$28 GS/s) is connected via transmission lines to a global clock generator, which produces 4 sampling clocks and 16 clock phases, each shifted by $T_\mathrm{s} = 1/f_\mathrm{s}$ [1]. These phases are routed to all 16 Sub-ADCs through a dedicated network optimized to minimize crosstalk between rising edges. Each Sub-ADC uses 13 of the 16 reference pulses to generate 29 internal clock signals for its three stages.

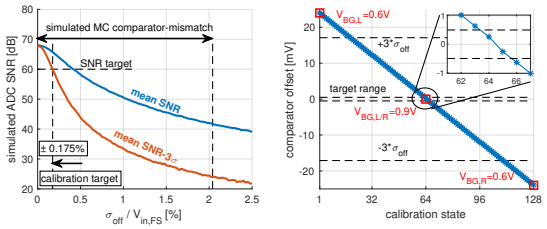

Fig. 3. Simulated offset requirements and calibration range

As all control signals are derived from the reference via frequency division, the TI-ADC sampling rate scales with f_s, enabling flexible operation from below 5 GS/s up to 28 GS/s and supporting power-efficient dynamic scaling.

3) Comparator: The comparator uses a StrongARM latch for fast dynamic operation (Fig. 4). To minimize power, no preamplifier is used, demanding individual input offset calibration. A statistical model is used to evaluate the impact of comparator and amplifier offsets on the SNR of an ideal 3-stage PI-SAR ADC. The average SNR, including a -3σ deviation, is shown in Fig. 3 as a function of normalized offset $\sigma_\mathrm{off}/V_\mathrm{in,FS}$. Excluding spurs, total SNR is limited by thermal noise, offset mismatch, and quantization noise. Achieving the 48 dB thermal-noise-limited SNR target requires offset suppression below –60 dBFS, i.e., normalized offsets $< \pm 0.18\%$. Given a Monte Carlo simulated offset variation σ_off= 5.7 mV and amplitude $V_\mathrm{in,FS}$= 280 mV, the residual offset must be below ± 0.5 mV. This is achieved by tuning the input transistors' bulk nodes, adjusting V_th and thereby g_m to cancel the offset during the comparators amplification phase. Unlike other methods, bulk tuning avoids parasitics at sensitive latch nodes. In Fig. 3, the bulk voltages of $\mathrm{M1_{L/R}}$ are swept (0.6–0.9 V), enabling offset correction over $\pm$ 24 mV in $<$ 0.4 mV steps (7-bit DAC), covering $\pm 3\,\sigma_\mathrm{off}$. The calibrated latch is followed by a high-speed SR latch and output driver. Metastability is mitigated by dynamically activating cross-coupled switches after the decision phase, reducing worst-case response time by up to 30 ps (Fig. 4). The output feeds a logic driver that generates 4 low-latency CDAC control signals.

4) Residue Amplifier: The two RA between the 3 SAR stages require fast settling within limited windows ($<$180 ps

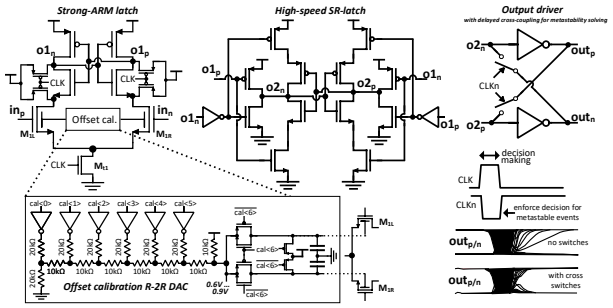

Fig. 4. Comparator schematic

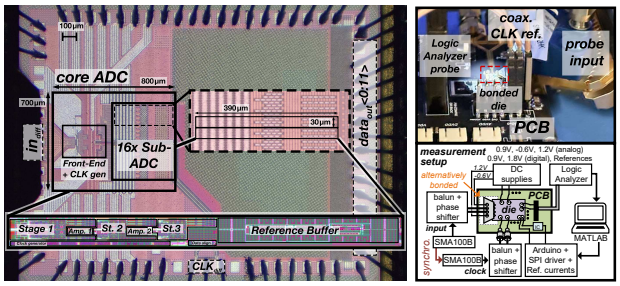

Fig. 5. Measurement setup, die photo with detailed description

at 1.75 GS/s). Open-loop architectures offer high speed but suffer from gain variation due to PVT and mismatch, requiring digital background calibration during post-processing. Each RA consists of three cascaded gm–R stages, as shown in Fig. 2, along with the design parameters. The first two stages provide gain, while the final stage uses a reduced load resistance to improve settling. To save power, the amplifiers are dynamically biased only during the amplification phase. A reset switch at the outputs compensates for turn-on delay and defines a precise time window for a fixed gain. All 16×2 amplifiers are biased by mirrored reference currents from a single off-chip I_{ref}, enabling global analog gain tuning. The ideal RA gains $A_1 = 2^4 = 16$ and $A_2 = 2^3 = 8$ are relaxed to ~ 10 and ~ 6, while nonidealities in the 2nd and 3rd stages remain sufficiently suppressed. The 2nd & 3rd CDACs are adjusted to match the reduced gain, while a redundancy margin is added. At $f_{\mathrm{s}} = 20$ GS/s, the amplifiers consume 4.4 mW per Sub-ADC, accounting for $\sim 42\,\%$ of the total 10.4 mW PI-SAR power. The 2nd-stage amplifier is a scaled-down version of the first, with relaxed requirement and no offset calibration.

5) Reference Buffer: The reference voltages are set to $V_{\mathrm{ref,p}} = 0.8$ V, $V_{\mathrm{ref,n}} = 0.38$ V, and $V_{\mathrm{cm}} = (V_{\mathrm{ref,p}} - V_{\mathrm{ref,n}})/2 + V_{\mathrm{ref,n}} = 0.59$ V. A "slow reference" buffer with a large on-chip capacitor ensures stable voltages at low power, though at the cost of increased area compared to "fast reference" buffers using high-bandwidth amplifiers. To reduce crosstalk, each Sub-ADC includes local reference buffers rather than sharing a global one. While $V_{\mathrm{ref,p/n}}$ variation due to process mismatch is tolerable, V_{cm} must stay centered to prevent residue amplifier railing from DC offset. This requires sufficient gain, therefore the buffers use 3-stage opamp's. Each buffer occupies $\sim 40\%$ of the Sub-ADC area but only $\sim 9\,\%$ of its power.

6) Data Alignment and Decimation: As each bit is generated by a dedicated comparator across three pipelined clock phases, all bits are phase aligned. For prototype characterization, a logic analyzer captures a decimated output stream. Due to equipment constraints, a decimation factor of 161 is used. Clocked by the same reference f_{s}, the decimator serializes the TI-ADC output to $f_{\mathrm{s}}/161$.

III. Measurement Results

A photograph of the prototype die with layout details and measurement setup is shown in Fig. 5. The core TI-ADC, including the FE and clock generator, occupies $0.56\,\mathrm{mm}^2$, while a single PI-SAR lane requires $0.012\,\mathrm{mm}^2$. The measurement supports input connection via wafer probe or bond wires to a PCB. The differential full-scale input is $V_{\mathrm{FS,diff}} = 1.1$ V, with measurements taken at $V_{\mathrm{in,diff}} = 0.93$ V (–1.5 dBFS). The ADC core operates with V_{DD}=0.9 V, while the FE sampler uses additional 1.2 V/–0.6 V. Comparator offset and RA gain are calibrated via iterative foreground routines using decision probability and noise tracking. Fig. 6 shows thermal SNR across 16 lanes and 4 dies, improving from 44.1 dB to 48.5 dB on average, with peak improvement up to 14 dB, following the trend of the model in Fig. 3. With frozen calibration, SNDR degrades by < 1.7 dB for ± 40 mV ΔV_{DD}, and by <0.5 dB after adaptive RA gain tuning for ± 80 mV ΔV_{DD}, demonstrating the robustness of bulk-controlled offset calibration. After lane merging, offset and gain mismatches are digitally corrected at low frequency via mean and RMS normalization. Due to slight gain drift (not phase) over f_{in} among the 4 FE T&H paths, an off-chip 16-tap FIR filter is applied to each interleaved lane. Time-skew errors are foreground calibrated using on-chip CAL-DACs while background detection via cross-correlation algorithms [3] is possible. Near the 3 dB frequency, tuning the T&H bulk nodes suppresses the dominant mismatch spur. Fig. 6 shows TI spectra before and after calibration at $f_{\mathrm{s}} = 20$ GS/s and $f_{\mathrm{in}} = 2.0\,/\,9.9$ GHz. Fig. 7 shows SNDR over f_{in} at $f_{\mathrm{s}} = 20$ GS/s with frozen calibration settings, ranging from 46 dB at 2 GHz to 42.4 dB at Nyquist. Comparator offset calibration improves SNDR by 4.1 dB, time-skew correction boosts SFDR by up to 15 dB and SNDR by 10 dB, and bandwidth mismatch correction adds $\sim$0.9 dB to SNDR and $\sim$5 dB to SFDR around 11 GHz. Fig. 7 also summarizes performance across f_{s}, showing low frequency / Nyquist SNDR of 47.5 / 44.5 dB at 15 GS/s, 45 / 40.9 dB at 25 GS/s, and 44 / 38.8 dB at 28 GS/s. At 20 GS/s, the ADC consumes 281 mW, scaling with f_{s} as shown in Fig. 8, which also details sub-block power distribution. Two low-power undersampling modes at 5 GS/s reduce power to 110 / 150 mW via buffer bias control, achieving 47 / 39 dB (low freq.) and 36 / 30 dB (16 GHz) SNDR, enabling sleep mode. Fig. 8 also compares Schreier FoM and aperture with state-of-the-art (SoA) ADCs [4]. Fig. 7 shows relative signal amplitude over f_{in}, with a wafer-probed bandwidth of 16.3 GHz, reduced to 13.8 GHz using bond wires ($L \sim$300 pH). Due to the AC coupled input buffer, the ADC has a high-pass corner at 1.1 MHz.

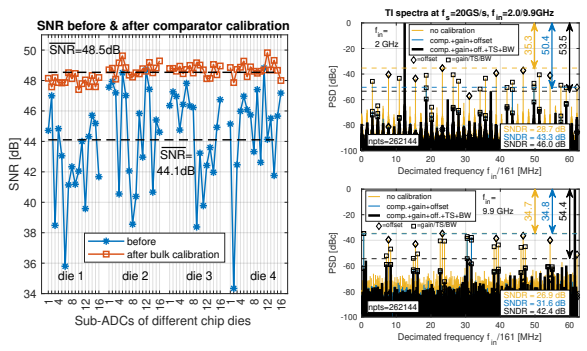

Fig. 6. SNR comparator calibration & TI-spectrum $f_s = 20$ GS/s

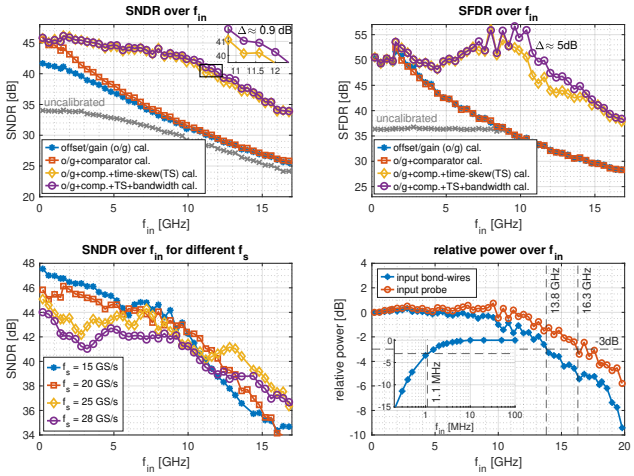

Fig. 7. Measured performance over f_{in}

IV. Summary

All key performance metrics, including Walden and Schreier FoMs, are summarized in Tab. I, demonstrating competitive results compared to SoA ADCs at similar resolution and sampling rates. The proposed ADC features on-chip bulk- and CDAC-based calibration engines to address comparator offsets, sample phase, and bandwidth mismatch. Offset-mismatch calibration across the 16× 3-stage multi-comparator PI-SAR lanes (operating up to 1.75 GS/s) improves SNDR by up to 10 dB, reaching a TI SNDR of 46 dB at low frequency (f_s=20 GS/s) across multiple dies. The buffered 4× TI front-end achieves high linearity with SFDR up to 56 dB while staying above 48 dB up to 12 GHz, enabling a 3 dB bandwidth of 16.3 GHz. Notably, the proposed ADC achieves the highest SNDR of 42.4 dB at 10 GHz (f_s=20 GS/s), considering the necessity of an input buffer which is required to drive the ADC while isolating sampling kickback and crosstalk from subsequent components such as a mixer or baseband amplifier. A differential reference sine drives an on-chip clock generator with σ_{jit}= 45 fs, producing FE sampling clocks and distributing 16 phases to all 16× Sub-ADCs. This enables high-speed synchronous clocking and adaptive sample rates. Time-skew and bulk-based bandwidth mismatch calibration in the FE contribute up to 11 dB SNDR improvement, enabling a Nyquist

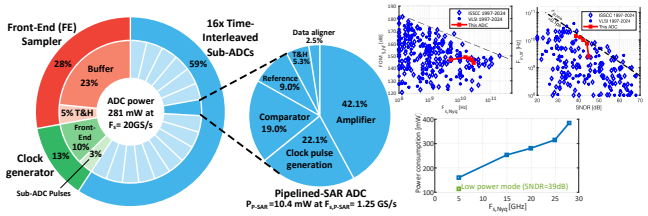

Fig. 8. Power consumption & Performance comparison

TABLE I
State-of-the-art ADCs with ≥10b, f_s ≥15GS/s

	This Work			[5] '23 ISSCC	[6] '23 ESSCIRC	[7] '18 VLSI	[8] '20 JSSC
Tech. [nm]	22			7	7	14	16
Supplies [V]	1.2/0.9/-0.6			N/A	0.75	0.8	1.8/1
f_s [GS/s]	**20**	**25**	**28**	24	16	32	18
BW [GHz]	16.3			7.2	5.8	26	18
SNR LF [dB]	**48.5**	**48**	**47.3**	47.5*	49*	N/A	53.5
SNDR LF [dB]	**46**	**45**	**44**	47.5*	48*	47.3	53.3*
SNDR Nyq [dB]	**42.4**	**40.9**	**38.8**	46.5△	41	42.7	48
Power [mW]	**281**	**315**	**385**	750	334	199	1300 □
FOM_{W} at LF/Nyq [fJ/c-s]	**86/ 130**	**87/ 139**	**106/ 193**	161*/ 181*△	102*/ 228*	33/ 56	191 */ 352*
FOM_{S} at LF/Nyq [dB]	**151.5/ 147.9**	**151/ 146.9**	**149.6/ 144.4**	149.5*/ 148.5△	151.8*/ 144.8	156.3*/ 151.8*	151.7*/ 146.4
Isolating Input-buffer	✓			✓	✓	-	✓

LF=(≤ 2 GHz) *extracted from published data △at f_{in} = 7.2 GHz □includes digital core

SNDR of 42.4 / 40.9 / 38.8 dB SNDR for f_s=20 / 25 / 28 GS/s. Hereby power consumption is 281 / 315 / 385 mW, achieving Schreier FoMs of 147.9 / 146.9 / 144 dB and Walden FoMs of 130 / 139 / 193 fJ/c-s, respectively.

Acknowledgment

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