A 7.7-to-9.8GHz SAR TDC FMCW ADPLL with −131dBFS linearity for 111MHz/25.6us chirp

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***Abstract*— This paper presents a 7.7-to-9.8GHz SAR TDC FMCW ADPLL with DCO PWL foreground calibration and DCO mapping dither technique. The PWL calibration "walks" in a statistical way over the DCO frequency characteristic, and measures DCO INL in the normalized frequency domain. The mapping dither technique lowers frequency error spur level due to timing errors over the radar frame. The ADPLL implemented in 28nm CMOS achieves -131dBFS linearity for 111MHz/25.6us chirp at 8.44GHz.**

Keywords—ADPLL, FMCW, SAR TDC, calibration

I. Introduction

The performance of FMCW automotive radars depends on chirp linearity. The residual frequency error spurs show in the range profile as ghost targets when a strong target (like a bumper) is present. Next, the SNR improvement during the Doppler processing is limited when each chirp, in the radar frame, has the same error. The PLLs with two-point modulation (TPM) [1,2] enable fast chirps, but gain calibration between two modulation paths is required. The multi-bank DCO tuning curve linearization [1] partially calibrates the coarse bank integral nonlinearity (INL) and LC interpolates the INL for other coarse bank codes. The scaling factor to "glue" the transfer function of the mid bank to the coarse bank is also calibrated, but the INL of mid/fine banks are not. Thus, the residual frequency error shows a strong DCO code dependency. Next, the background calibration accuracy is limited by intersymbol interference between different error sources. The dynamic-element-matching (DEM) DCO control is used in [2] to linearize the DCO transfer function. Due to a partial calibration (interpolation) the residual frequency error still shows large level of frequency error spurs for the frequency offset above the PLL bandwidth even though a low FM RMS value is achieved.

This work presents the full DCO piecewise-linear (PWL) foreground calibration, DCO mapping randomization and FMCW ADPLL that achieves -131dBFS linearity for 111MHz/25.6us chirp at 8.44GHz with 2us settling time with 150kHz PLL BW. FM RMS linearity is two times better than [2] for less area and power consumption. SFDR for the large chirp amplitude is 25dB better than [1]. This performance enables deployment of chirp ADPLL in radar application.

II. ADPLL Architecture

Fig. 1 shows the architecture of a SAR TDC based ADPLL. The ADPLL supports two-point modulation through the chirp generator, DCO PWL control and DCO PWL calibration blocks. The LC DCO has the PLL locking path composed of three switched capacitor tuning banks: PVT, coarse (ACQ) and fine (TRK). Due to the dynamic range/resolution trade off the modulation path (MOD) is

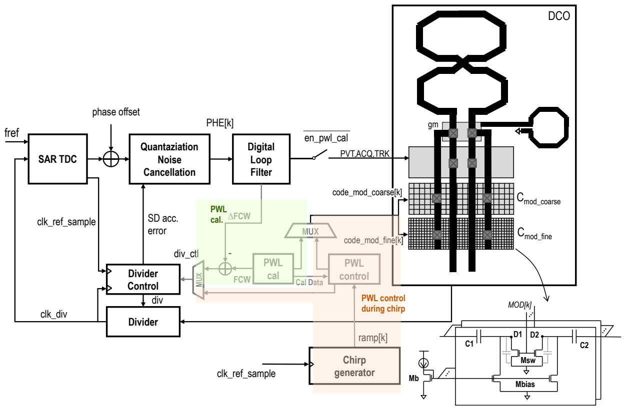

Fig. 1. SAR TDC based ADPLL configuration during the PWL foreground calibration.

constructed from coarse (8b, code_mod_coarse control) and fine (7b, code_mod_fine control) capacitor banks. The star connection is used between PLL/modulation banks so the PLL path state does not invalidate the modulation calibration data through the common inductance during the temperature tracking. The dynamic settling error due to the nonlinear capacitance in the drain of switch (Msw) during ON-OFF transition is improved by adding the controlled finite impedance (Mbias). The fine bank frequency resolution is 43kHz at 8.44GHz. The modulation bank capacitors are switched off starting from the base calibration frequency locked by the PLL path. The DCO is implemented as the top-biased differential LC oscillator [3]. The negative gm cross-coupled pair is realized with GO2 NMOS devices in order to get a phase noise of -122dBc/Hz at 1MHz offset at 8.44GHz. The feedback path is realized through a multi modulus divider that selects one edge of the DCO based on the input from the divider control. The divider control block comprises a ΔΣ modulator for the fractional-N frequency control and it is tracking the accumulated quantization noise of divider. The SAR TDC block measures the time difference between the selected edge of the DCO and the reference signal. The accumulated divider quantization noise is removed in the quantization noise cancellation block. The loop is closed through the digital loop filter.

A. DCO control

Fig. 2 shows the modulation path DCO control. The PWL calibration stores, in the normalized frequency domain (FCW), the DCO INL data in memory (LUT MEM) for each DCO input code of modulation banks. The chirp generator creates a chirp signal ramp[k], in the FCW domain, at each timestamp point of the clk_ref_sample clock. For each chirp frequency point, quantization process starts by a direct binary search to find the coarse code (code_coarse[k]) that produces

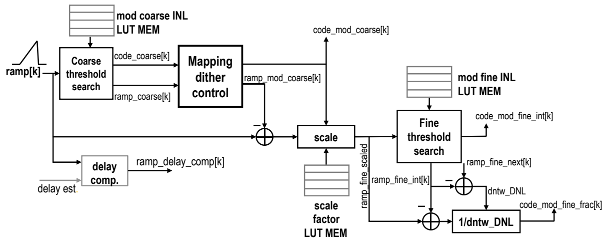

Fig. 2. DCO PWL control: DCO quantization calculation.

the closest frequency point ramp_coarse[k] that is below the required chirp frequency point ramp[k]. When the dither control is inactive, ramp_mod_coarse[k], which is the same as ramp_coarse[k], is used for the residual error calculation. The residual error is scaled and the quantization process is repeated to find the fine bank code code_mod_fine_int[k]. The fine bank is operated as a high speed re-quantizer. The fractional part code_mod_fine_frac[k] of the DCO control is calculated from the residual frequency error and the next code DNL dntw_DNL. The scaling allows for re-use of the fine modulation bank INL at each frequency bin of the coarse bank. The fine bank has an overrange of two coarse steps. When active, the mapping dither control randomly decides whether to use the current or the previous coarse code/quantization level in the residual frequency error calculation for the fine bank quantization. For the same input frequency the mapping dither will generate different sets of DCO codes during the radar frame as shown in Fig. 3. The size of coarse, scale, and fine LUTs are 225x28b, 225x24b and 129x20b respectively.

B. DCO PWL calibration

The DCO foreground calibration is executed at the beginning of each radar cycle. The ADPLL configuration during the DCO INL measurement is shown in Fig. 1. The PWL calibration starts from the current locked channel FCW. The DCO is disconnected from the PLL loop and the DCO input code is controlled by the PWL calibration block. The divider input is connected in the PLL loop. This technique is similar to that proposed in [4], but applied to calibration. The div_ctl input of the divider control will change until it matches (in normalized domain) the frequency at the output of the DCO. To calibrate the DCO step, the PWL calibration toggles the DCO input between the current code and the next code as shown in Fig. 3 for the coarse bank INL calibration. The DCO frequency step (DNL) is calculated from the difference of the divider input for two toggle states. To remove the DCO noise, the average DNL is calculated from multiple toggling measurements. To calibrate the next DCO code, the divider input (FCW) is incremented by the DNL of the current DCO code and the next modulation code is applied. The divider input is saved as the threshold to the INL LUT at the address of the next code. Before the next code is toggled, the DCO is temporarily connected to the PLL loop to remove any DCO drift during calibration. The toggle procedure is then repeated for the next code. In this way PWL calibration “walks” in a statistical way over the DCO frequency characteristic. The scaling LUT calibration can be interleaved with the coarse bank calibration if the coarse code is fixed, and the toggling of the fine bank is done to measure the fine bank step at given frequency. The ratio of the fine bank step for the first code and the fine bank step for

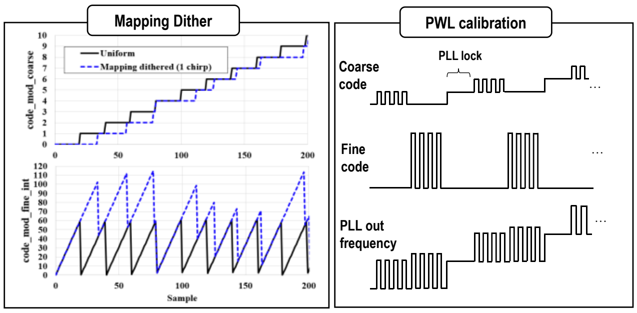

Fig. 3. Code redundancy during the mapping dither, PWL calibration procedure.

the current coarse code gives the scaling factor for the current coarse bin.

The DCO control path delay, if not compensated, produces the phase error step during the coarse bank switching. The DCO path delay is calculated as ratio of the measured phase error step and the PWL calibrated frequency step of the coarse bank for a given input code. The delay compensated ramp_delay_comp[k] chirp signal is added to div_ctl input to cancel the highpass modulation signal.

The full DCO calibration, done only once during startup, takes 760ms. The tracking calibration measures a subset of calibration points and scales the rest, and it takes 58ms.

III. SAR TDC

Fig. 4 shows SAR TDC. The TDC is composed of a synchronization block (Sync.), a charge pump (CP), an active integrator, and a successive approximation analog to digital converter (SAR ADC). Similarly to [5], the frequency of the divider output is multiple times higher than the reference clock. The divider output is used to synchronize the reference clock in the sync block so only one pulse per reference cycle is generated at the sync output. This way the required TDC dynamic range is reduced to the divider output sampling grid. Under control of the sync out pulse, the CP deposits the charge on the integrator capacitor. The charge is digitized by the switched capacitor SAR ADC to produce digital TDC output code tdc[k]. The TDC dynamic range can be set by controlling the CP current i1, i2. During the locking phase low value of i1, i2 is used in order not to saturate the integrator. During the tracking phase the synchronization is replaced with a PFD detector, and the TDC input dynamic range is reduced by increasing the CP level to lower the SAR TDC quantization noise. Fig. 4 also shows the differential CP circuit diagram. The common-mode feedback (CMFB) circuit sets the PMOS current source to be matched with the NMOS current source at the middle of the supply voltage Vcm. The CMFB loop is active only when both UP/DOWN signals are zero. Without the CMFB the mismatch between PMOS and NMOS current sources would result in the second order distortion. The CMFB frequency compensation is achieved by adding a compensating zero as in [6]. The SAR TDC dynamic range is programmable from +/-8.7ns to +/-1.1ns. For the low input dynamic range the TDC resolution is 2.1ps. The measured jitter is 420fs rms, integrated from 1kHz to 100MHz for 150kHz PLL BW. The in-band fractional spur level is -57dBc. The low spur level contributes to the chirp linearity for the frequency points close to the multiples of the reference frequency.

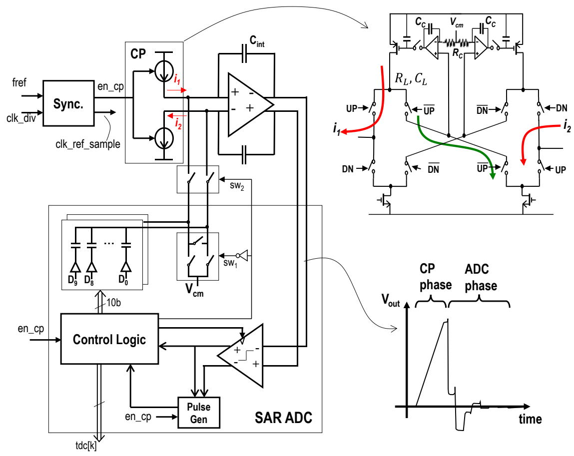

Fig. 4. SAR ADC based TDC.

IV. Measurement Results

Fig. 5 shows measured linearity of 111MHz/25.6us chirp. To separate the phase noise and the nonlinearity contributions to the FM RMS error, a single shot chirp and a radar frame measurement were done. The radar frame nonlinearity is estimated by coherently averaging 100 chirps (equivalent to the zero Doppler hypothesis in radar processing). The LC interpolation of partial calibration data, like [1], increases the low frequency offset clutter level and high frequency spurs. The chirp linearity improves by using the full calibration data, and it is dominated by timing errors. When the full calibration is combined with the mapping dither the linearity improves to -131dBFS level. Similar gain was observed in other Doppler cuts. For high frequency offsets there is no clear distinction between noise and spurs which is a must for a radar.

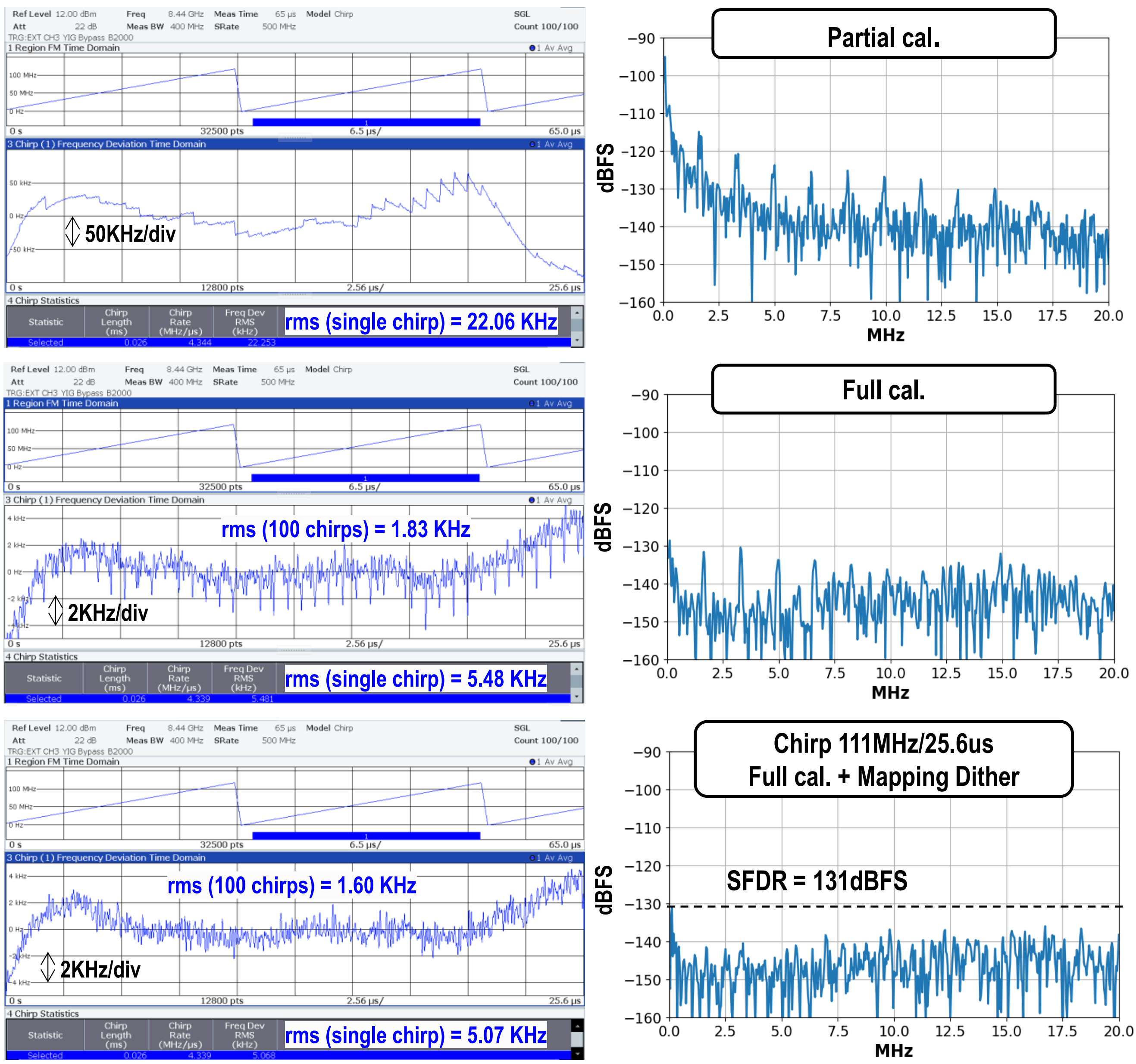

Fig. 5. Measured FM error for 111MHz/25.6us chirp with 2us settling time, FM video BW of 20MHz with 150kHz PLL BW: Partial calibration with interpolation (top), full calibration (middle), full calibration with the mapping dither (bottom).

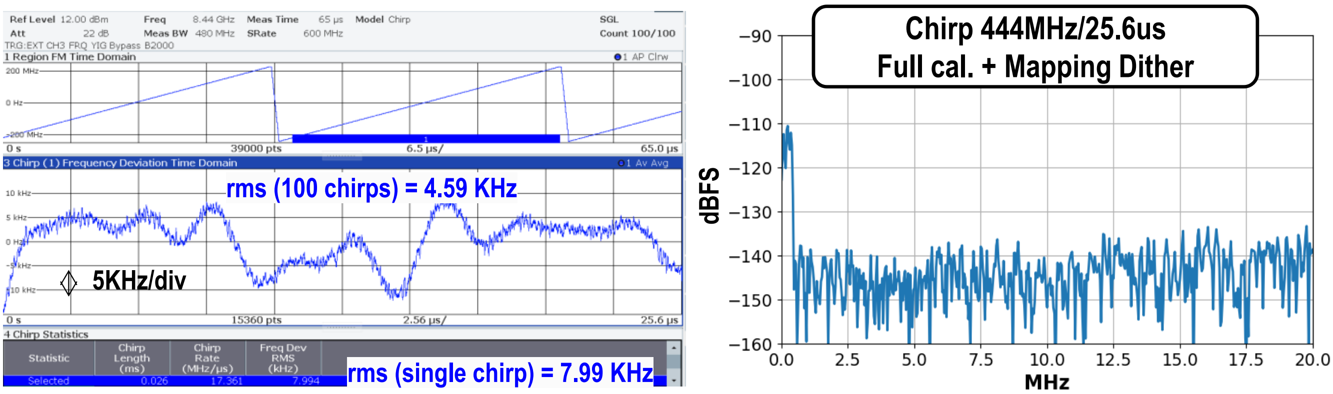

Fig. 6. Measured FM error for 444MHz/25.6us chirp with 2us settling time, FM video BW of 20MHz with 150kHz PLL BW.

Fig. 6 shows 444MHz/25.6us chirp linearity. The low frequency nonlinearity increase is due to limited bandwidth of the measurement buffer. Table I shows performance comparison with prior works. Fig. 7 shows the ADPLL die micrograph fabricated in a 28nm CMOS process, occupying 1mm2.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

		This work	ISSCC 2024 [1]	ISSCC 2022 [2]
Technology		28nm CMOS	28nm CMOS	28nm CMOS
Architecture		SAR TDC ADPLL	TPM DPLL	RTWO-based ADPLL
Chirp linearization technique		Full calibration, Mapping dither	Non-Uniform PWP DPD	Interpolation, RDEM, TDEN, FCO
Frequency range [GHz]		7.7 to 9.8	9.25 to 10.5	8.8 to 12
Reference frequency [MHz]		40	250	80 to 200
Max Chirp BW [MHz]		620 (@8.44GHz)	680 (@10GHz)	650 (@9.5GHz)
RMS FM error @fDCO[KHz]	1 chirp	5.07 (111MHz/25.6us) 7.99 (444MHz/25.6us)	67 (540MHz/32us)	12 (23MHz/20us) 37 (500MHz/10us)
	100 chirp avg	1.60 (111MHz/25.6us) 4.59 (444MHz/25.6us)	NA	NA
RMS FM error @76GHz [KHz]	Multiplication ratio	×9	×8	×8
	1 chirp	45.6 (39MHz/us) 71.9 (156MHz/us)	536 (135MHz/us)	96 (9.2MHz/us) 296 (400MHz/us)
	100 chirp avg	14.4 (39MHz/us) 41.3 (156MHz/us)	NA	NA
SFDR [dBFS]		131 (111MHz/25.6us) 110 (444MHz/25.6us)	85 (540MHz/32us) [1]	NA
DCO PN @ 1MHz offset [2] [dBc/Hz]		-122	-117.5	-122
Power consumption [mW]		91	21	187
Fractional Spur [dBc]		-55.6	-53.7	NA
Area [mm^2]		1	0.34	2

[1] estimated based on Figure 10.6.4 in [1]

[2] Normalized to 8.44GHz

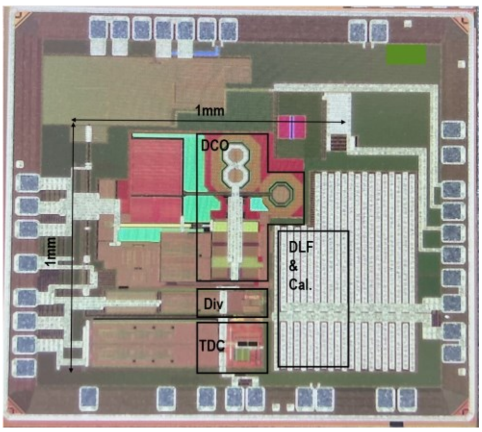

Fig. 7. Die micrograph.

V. CONCLUSIONS

In this paper, we presented ADPLL based FMCW chirp generator that achieves -131dBFS linearity (100 chirp average) by combining the full DCO INL calibration to linearize the DCO frequency transfer function and the mapping dither techniques to reduce the timing errors over the radar frame. The full DCO calibration enables any chirp profile (up/down, stepped-frequency etc.) over the whole frequency band with a single DCO calibration.

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REFERENCES

[1] F. Tesolin et al., "A 10GHz FMCW Modulator Achieving 680MHz/µs Chirp Slope and 150kHz rms Frequency Error Based on a Digital-PLL with a Non-Uniform Piecewise-Parabolic Digital Predistortion", ISSCC, pp. 198-199, 2024.

[2] H. Shanan et al., "A 9-to-12GHz Coupled-RTWO FMCW ADPLL with 97fs RMS Jitter, -120dBc/Hz PN at 1MHz Offset, and with Retrace Time of 12.5ns and 2µs Chirp Settling Time," ISSCC, pp. 146-147, Feb. 2022.

[3] E. Hagazi, H. Sjoland, and A. Abidi, "A filtering technique to lower LC oscillator phase noise," IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[4] M. Ferriss at al., "A 14mw fractional-n pll modulator with an enhanced digital phase detector and frequency switching scheme," ISSCC, pp. 352-353, Feb. 2007.

[5] C.-M. Hsu et al., "A Low-Noise Wide-BW 3.6-GHz Digital SD Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2776 –2786, Dec. 2008.

[6] Lah, J. Choma, and J. Draper, "A continuous-time common-mode feedback circuit (CMFB) for high-impedance current-mode applications," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 4, pp . 363-369, April 2000.