New Perspective on Chiplet ESD and Dielectric Breakdown for Optimizing Protection Circuit in 2.5D/3D bonding technology

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***Abstract*— Chiplet Electrostatic Discharge (ESD) presents a critical reliability challenge for 2.5D/3D integration. This paper introduces a methodology to optimize ESD protection for chiplet internal interfaces. The approach integrates measured chiplet ESD characterization with device robustness evaluations that utilize Very Fast Transmission Line Pulsing (VF-TLP) and full-chip testing. A systematic correlation between measured chiplet ESD characteristics and circuit ESD vulnerabilities guides the design of optimized ESD protection. Demonstrated using a Universal Chiplet Interconnect Express (UCIe) transceiver, this methodology offers a framework for developing area-efficient, custom ESD protection for chiplet internal I/Os.**

Keywords—2.5D/3D, ESD Protection, Chiplet, Internal IO

I. Introduction

Memory latency remains a significant bottleneck in high-performance computing [1], driving advancements in 2.5D/3D die-stacking to achieve closer logic-memory integration. This integration, however, introduces a critical and underexplored vulnerability: Electrostatic Discharge (ESD) within chiplets that affects internal I/Os. Unlike well-characterized ESD events at external I/Os (such as CDM), these internal events often involve significantly lower voltages—potentially as low as 3V, posing unique protection challenges [2, 4]. This vulnerability is exacerbated by industry trends towards lower intrinsic device withstand voltages and shrinking interconnect pitches in 2.5D/3D stacking, which severely constrain the area for protection circuits. To address this specific low-voltage internal ESD threat, this paper presents a methodology that combines chiplet-level ESD waveform characterization, Very Fast Transmission Line Pulsing (VF-TLP) testing, and Dielectric Breakdown Testing. Our study discusses the framework for developing optimized, area-efficient ESD protection circuits, which are essential for robust 2.5D/3D internal I/O interfaces.

II. Chiplet ESD Characterization

To address the Chiplet ESD models, we developed a testing setup (Fig. 1) mimicking the ESD event in 2.5D/3D bonding. Our setup uses diced silicon chiplets with aluminum metallization, mirroring real scenarios. Unlike standard FICDM tests [3], our chiplets (25-225mm²) were positioned on an 85um-thick dielectric layer on top of a grounded plane. The chiplets are charged by an SMU to emulate triboelectric charge accumulation. Discharge occurred through a 1Ω current-sensing probe (from [2]), replicating low impedance die-to-die interconnects. Current waveforms were captured using a 23GHz and 100GS/s oscilloscope. Automated tests with ≥100 measurements per condition ensure statistical significance. Analysis of the captured transient waveforms, illustrated in Fig. 2, indicates a consistent pulse shape irrespective of the applied charging voltage. It is important to clarify that the measurements presented in Fig. 2 specifically capture the Chiplet ESD waveform by a positive induced voltage; the waveform by a negative induced voltage was not measured in this study. For negative charging, we assume the waveform to be opposite in polarity to the positive case. This assumption forms the basis for our later analysis of protection requirements under negative charging scenarios in Section IV. The measurement reveals a notable asymmetry in peak currents (I_{peak}), with the magnitude of the second (negative) I_{peak} frequently exceeding that of the first (positive) I_{peak}, as shown in Fig. 3. As depicted in Fig. 4 for a 75 mm² chiplet, the peak discharge current (I_{peak}) demonstrates a clear linear dependence on chiplet charging voltage.

This linear relationship is statistically confirmed by the high R-squared value (>0.99) and low Root Mean Squared Error (RMSE) from the linear fit shown. This characteristic linear scaling was also consistently observed for larger chiplet sizes, such as 225 mm². Furthermore, the analysis revealed a consistent asymmetry: median second (negative) I_{peak} exceeded the first (positive) I_{peak} by ~15% across most voltages. Analysis of three statistical metrics presented in Fig. 5—Normalized Interquartile Range (nIQR), Coefficient of Variation (CV), and Normalized Median Absolute Deviation (nMAD)—confirms the repeatability of the experimental measurements. Although potential surface oxidation of the aluminium metallization could theoretically introduce additional variability, the consistency observed in our data implies that such effects might only have a limited effect. Also, a clear linear relationship between I_{peak} and chiplet area was identified (Fig. 6). This finding suggests a predictable scaling for Chiplet ESD voltage based on chiplet size, directly correlating larger areas with increased peak discharge currents and potentially higher ESD risk. Frequency spectrum analysis of the measured Chiplet ESD events (Fig. 7) reveals dominant spectrum content concentrated within the 3-4 GHz range, accounting for approximately 80% of the observed cases. A secondary, less frequent peak occurs in the 10-13 GHz range (approximately 20% of cases). These characteristic frequencies are higher than the typical ~1 GHz spectrum from standard CDM waveforms defined by [3].

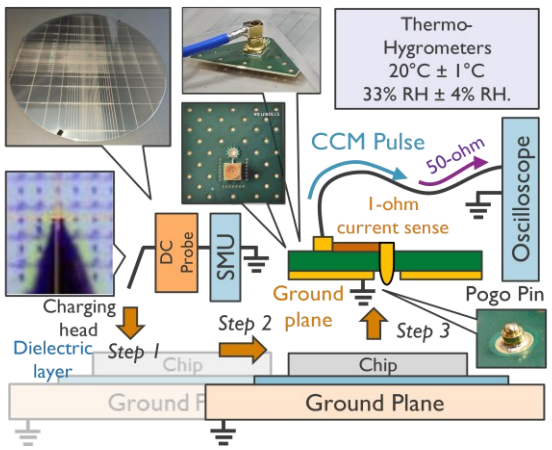


Figure 1. Schematic diagram of the experimental setup designed for Chiplet ESD characterization. The setup

emulates the 2.5D/3D bonding process by directly charging with SMU and discharging metallized silicon chiplets with 1 Ω current sensing probe.

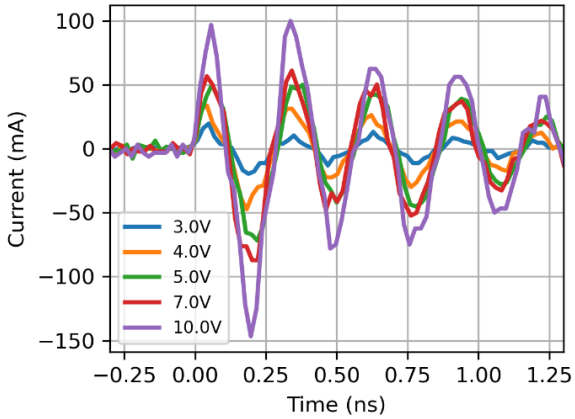


Figure 2. Representative discharge current waveforms for a 75mm² chiplet at various charging voltages. The consistent pulse shape at various charging voltages indicates a uniform discharge mechanism. This strong oscillation is also distinct from the typical waveform outlined in the CDM standard [3].

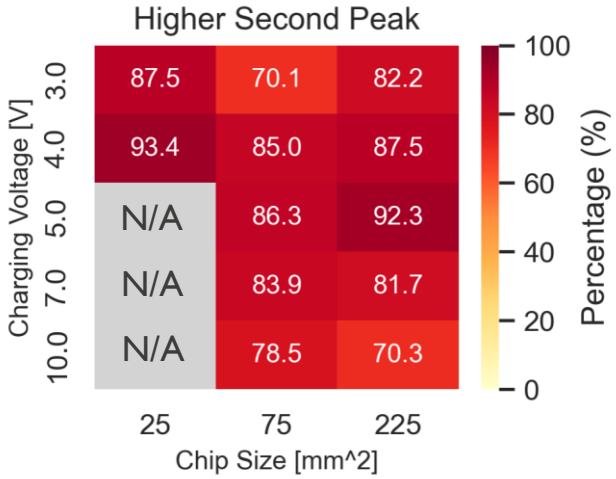


Figure 3. The high occurrence of larger second peak currents is confirmed statistically by more than 1200 measured discharge events.

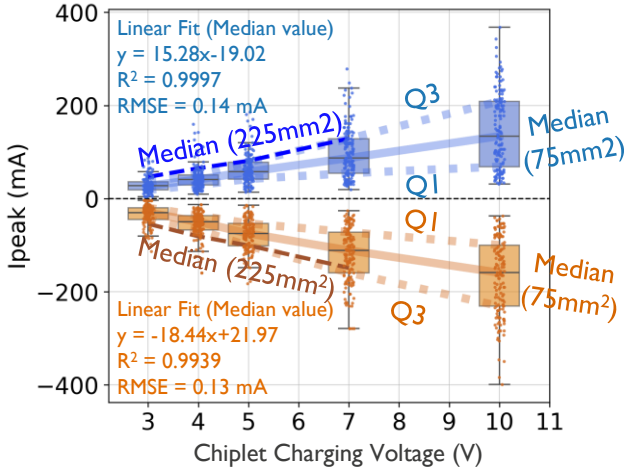


Figure 4. Measured peak discharge current I_{peak} as a function of charging voltage for 75mm² and 225mm² chiplets. The results demonstrate a linear scaling of I_{peak} value with voltage for both chip sizes. Notably, negative polarity I_{peak} is consistently larger than positive I_{peak} across all voltages.

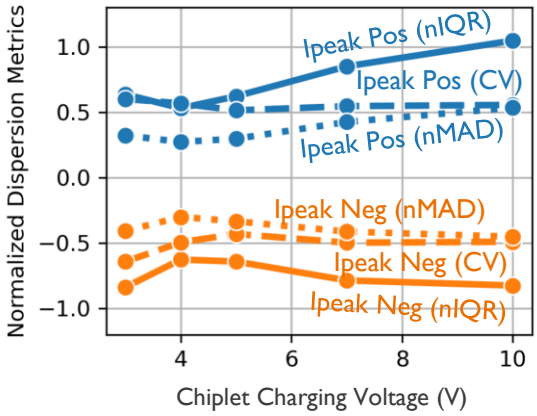


Figure 5. Low and constant normalized metrics for peak discharge current across charging voltages and polarities indicate consistent variability, independent of pre-charge voltage, and therefore confirm a robust Chiplet ESD measurement methodology.

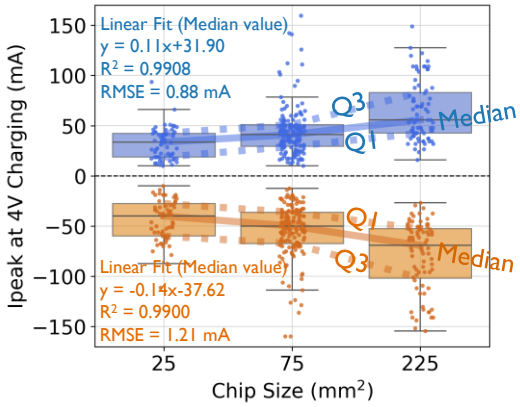


Figure 6. Peak discharge current (I_{peak}) at 4V scales linearly with chip area (25-225mm²), confirming that larger chip area will require higher ESD protection.

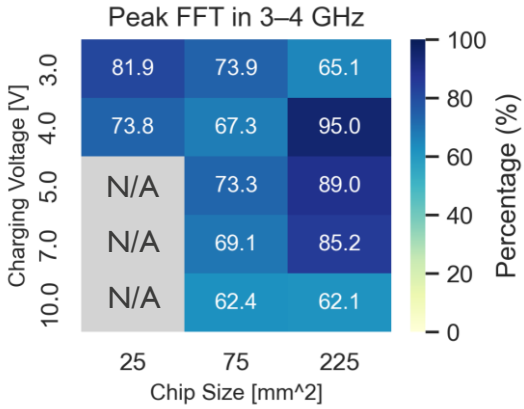


Figure 7. Frequency spectrum reveals high occurrence for I_{peak} at 3-4 GHz (~80% of cases), and low occurrence at 10-13 GHz (~20% of cases), frequencies exceeding the ~1 GHz typical for JS-002 CDM.

III. Dielectric Breakdown Testing

To evaluate the transistor dielectric robustness under realistic Chiplet-ESD conditions, we must move beyond the standard device-level (two-pin) VF-TLP tests. Such conventional tests typically isolate the stressed component (e.g., focusing on

gate oxide integrity) and may consequently underestimate the overall system robustness. Real-world ESD events engage the entire chip structure, a floating substrate, and a grounded or floating wafer chuck in the 2.5D/3D integration tool. To address this, we employed dielectric breakdown testing using representative full-chip (single-pin) configurations with grounding at the back of the wafer (Fig. 8); and a variation with an interposed dielectric representing conductive vs. insulating bonding chuck. Iterative VF-TLP pulses (pulse width 1 ns and rise time 200 ps) were applied to PMOS/NMOS devices on a 9mm² 12nm FinFET chip until the gate oxide broke (10% leakage increase). The results underscore the importance of realistic test configurations. Full-chip setups consistently yielded higher breakdown voltages (V_{BD}) than device-level tests (Fig. 9). The dielectric layer provided further V_{BD} enhancement, especially for PMOS devices, suggesting series capacitance from both PMOS n-well junction and dielectric mitigates gate oxide stress. Area-dependent effect was also observed, with larger 10X PMOS devices benefiting more than 1X devices (Fig. 9), likely due to increased junction capacitance. Measurement repeatability was verified using control charts (Fig. 10). Future work is required to explore negative polarity stress, the possible overshoot of ultra-fast ESD (mimicking actual Chiplet ESD).

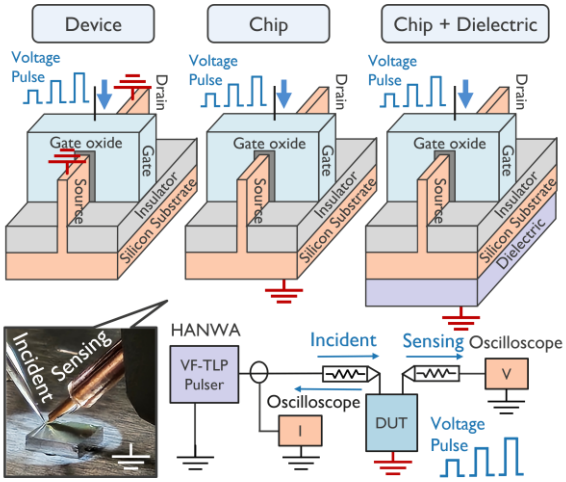


Figure 8. Schematic illustration of the Dielectric Breakdown Testing setups used to evaluate device ESD robustness. Three VF-TLP-TDT configurations were tested: (1) device-level, (2) full-chip with grounded backside, and (3) full-chip with dielectric and grounded wafer chuck.

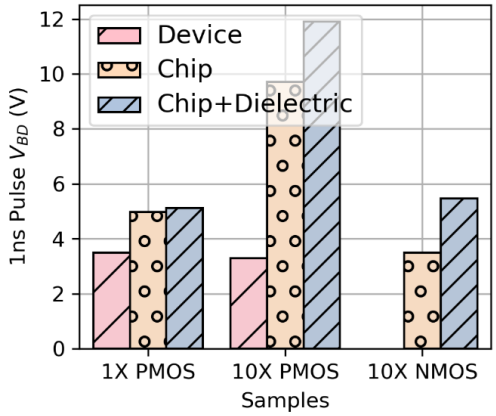


Figure 9. Gate oxide breakdown voltage of PMOS and NMOS devices measured using VF-TLP in device-level and full-chip configurations (grounded and insulated with dielectric). The results show an increase in V_{BD} for full-chip configurations, particularly with the dielectric layer.

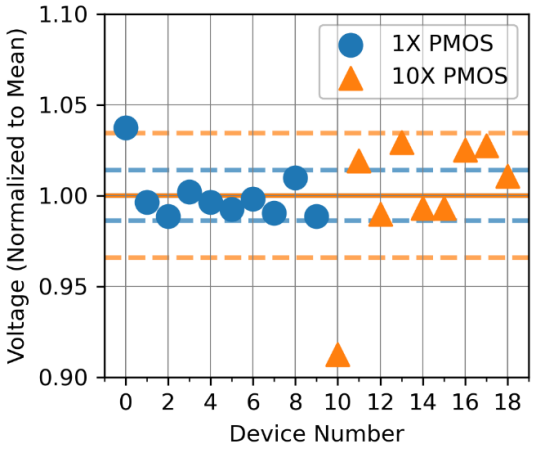


Figure 10. Control charts show consistent V_{BD} measurements for 1X area and 10X area PMOS devices (with dielectric config), validating the testing methodology's reliability.

IV. Optimizing ESD Protection Circuit for UCIe I/Os

Using the discussed chiplet ESD insights, we evaluate the ESD robustness of the transceiver design for Universal Chiplet Interconnect Express (UCIe) [5], as a case study applying waveform characteristics to protection. We use VF-TLP (1 ns pulse, 200ps rise) to characterize the dual-diode ESD protection for transceiver. Despite waveform differences between VF-TLP and Chiplet ESD event (Fig. 2), it's a practical method for assessing ESD failure current thresholds (I_{t2}). Characterization involved PD, PS, ND, NS stress for Rx, and PD/NS for Tx (Fig. 11). The Rx incorporates an RC-triggered power clamp with a 1040 µm² area BigFET.

VF-TLP testing on Rx circuits revealed a lower positive-pulse breakdown voltage than negative (Fig. 12). Despite this ESD robustness asymmetry, positive chiplet charging (Fig. 13a) indicates optimal symmetric Rx protection. This correlates lower positive I_{peak} stress (Fig. 4) with weaker device positive polarity robustness. Conversely, with negative chiplet charging (Fig. 13b), an asymmetric Rx design (differently sized upper/lower dual-diodes) is optimal. This asymmetric approach better aligns protection with the higher negative I_{peak} stress and the device's stronger negative robustness. These contrasting outcomes (Fig. 13a vs. 13b) underscore that the optimal ESD strategy requires correlating potentially asymmetric source characteristics (Fig. 4) with inherent device robustness asymmetries. Thus, the design topologies depend critically on specific stress polarity and magnitude, recognizing that a final design must ultimately address the overall worst-case from unpredictable event polarity. Other findings include weaker PD/PS performance (additional RC clamp bypass) in Rx. For Tx, inherent diodes provide ~13V self-protection within in a ~ 13 um² layout area, needing less additional ESD protection than Rx.

The core contribution of this work is the presented methodology for tailoring chiplet ESD protection strategies by integrating chiplet ESD characteristics. The analysis of the UCIe transceiver [5] serves as an example of using this approach. Specific design suggestions (e.g., symmetric Rx,

and asymmetric Tx) are secondary outcomes, dependent on the ESD control, ESD protection circuit, and the specific technology. The generally applicable principle, however, is the systematic framework: (1) Estimate chiplet ESD waveforms depending on its size and target stress voltage to identify the stress parameters like I_{peak}. (2) Correlate these parameters with ESD robustness data (e.g., by VF-TLP testing). (3) Utilize this integrated understanding to optimize ESD protection circuit (e.g., dual-diode protection) for area and capacitance penalty. This methodology provides a robust framework for designing effective chiplet interface with ESD protection.

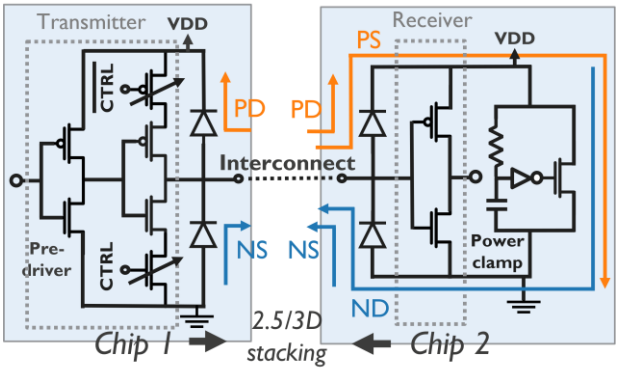


Figure 11. This schematic illustrates gated diode ESD protection in a simplified UCIe transceiver with 12nm FinFET technology [6]. Its ESD robustness for the high-speed internal I/O was characterized using VF-TLP stress (1 ns pulse, 200ps rise).

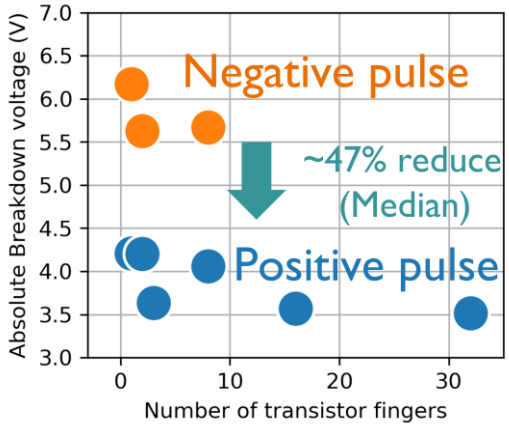
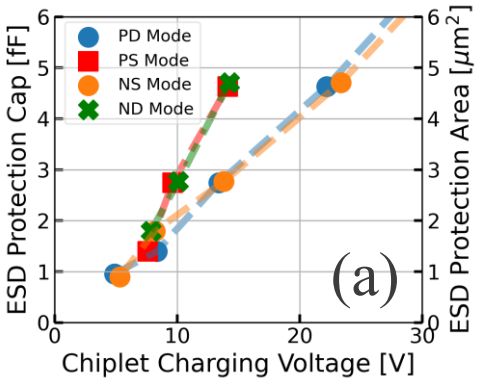


Figure 12. Breakdown voltage measurement with VF-TLP testing method on Rx circuits revealed a ~47% lower positive-pulse breakdown voltage compared to negative, attributed to gate stack differences, indicating potential NS/ND mode ESD vulnerability on Rx.



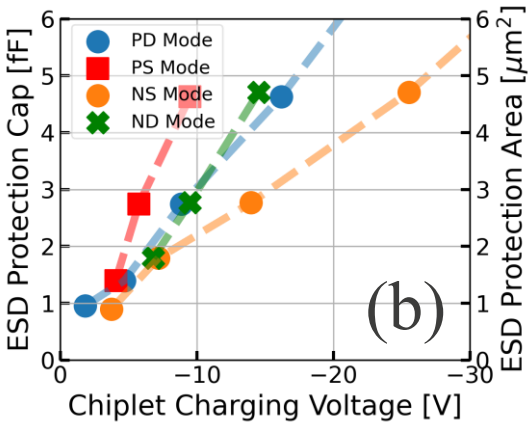


Figure 13. Rx ESD protection capacitance and area penalty as a function of chiplet charging voltage, extrapolated from VF-TLP failure current (I_{t2}). Plot shows required area for four VF-TLP modes (PD/PS/NS/ND), illustrating the required area for achieving different chiplet charging voltage from ESD event with both (a) Positive and (b) Negative polarity.

V. Conclusion

This paper presents and demonstrates a methodology for optimizing Chiplet ESD protection for reliable 2.5D/3D integration. The main purpose is to provide the systematic approach, which integrates measured chiplet ESD characterization—quantifying specific threats such as ~15% peak current (I_{peak}) asymmetry between polarities and faster pulses with dominant multi-GHz frequencies (3-4 GHz)—with assessments of device and circuit ESD robustness. Notably, full-chip dielectric breakdown testing with a floating substrate revealed the enhanced robustness compared to standard device-level tests. This methodology hinges on correlating such quantitative stress data and measured ESD vulnerabilities (e.g., using VF-TLP) to enable area-efficient protection design choices, such as selecting symmetric versus asymmetric protection structures. Demonstrated through a UCIe transceiver case study, the primary value of this work lies in its adaptable optimization process. This process provides an essential framework for developing robust ESD solutions applicable across diverse chiplet technologies requirements.

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