A 0.25-V-V_{DD} 0.93-nW 1-Kbps Amplifier-and-Bias-Free Time-Domain Wake-Up Receiver Occupying 0.045-mm^2 Achieving −66-dBm Sensitivity and −165.9-dB FoM

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***Abstract*—This paper presents a sub-0.3V-V_{DD} sub-nW wake-up receiver (WuRx). Utilizing our proposed voltage-controlled delay line (VCDL) based time-domain comparator (CMP), the amplifier along with its bias circuit can be removed. Thus, not only the power, area and noise are reduced, but also V_{DD} can be lower down to 0.25 V. Meanwhile, devising the sensitivity-optimized offset calibration loop (SO-OCL), a sufficient WuRx sensitivity at different V_{DD} can be achieved, ensuring the robust operation at sub-0.3-V V_{DD}. Fabricated in a 40-nm CMOS, our prototype can operate at 0.25-V V_{DD} with 1-Kbps chip rate, and achieves 0.93-nW power, 0.045-mm^2 core area, −66-dBm sensitivity, and −165.9-dB FoM. The measurement results also show robustness over V_{DD} variation.**

Keywords—Sub-0.3V-V_{DD} sub-nW wake-up receiver (WuRx), time-domain comparator, sensitivity-optimized offset calibration loop (SO-OCL), V_{DD} variation.

I. Introduction

To suppress redundant active power dissipation in the main radio, thereby alleviating maintenance overhead, the wake-up receiver (WuRx) is becoming indispensable for ultra-low-power applications such as wireless sensor networks [1]. Thus, tailoring a sub-0.3-V sub-nW compact WuRx is highly desirable to extend the battery lifetime or even enable battery-less operation by harvesting the energy from the environment. Several WuRxs have been reported, including the voltage-domain CMP (VD-CMP) based WuRxs [2-11] and time-domain CMP (TD-CMP) based counterparts [12-15], but they are challenging to achieve the above goals for the following reasons. In the VD-CMP based WuRx [Fig. 1(a)], the amplifier (AMP) consumes large portion of the whole power, and its noise and V_{DD} sensitivity worsens severely at sub-0.3-V supply voltage; meanwhile, the AMP along with its bias circuit and AC-coupling network, the capacitor array in the VD-CMP [3], and the resistor array occupy large area. In contrast, in the TD-CMP based WuRxs [Fig. 1(b)], both capacitor and resistor array are removed for area shrinkage, but the AMP issues still exist and the noise of voltage-controlled oscillator (VCO) degrades much at sub-0.3-V V_{DD}, hence worsening WuRx sensitivity. Furthermore, the delay difference Δt in the TD-CMP, which requires careful manual tuning for sensitivity optimization, varies much with V_{DD}, causing poor robustness.

To surmount these issues above, this paper proposes an ultra-low-power amplifier-and-bias-free wake-up receiver with a VCDL-based time-domain comparator and sensitivity-optimized offset calibration loop [Fig. 1(c)]. It features: 1) the AMP along with the bias circuit is removed to avoid AMP noise with lower power, smaller area and less V_{DD} sensitivity; 2) a VCDL-based TD-CMP is proposed to replace two noisy VCOs in prior TD-CMP with two high-tuning-gain VCDLs, thus avoiding sensitivity degradation even without AMP; 3) utilizing our devised SO-OCL, the tuning voltage V_{CAL} is adaptively adjusted so that not only the mismatch between two VCDLs is compensated but also the WuRx sensitivity can be optimized regardless of V_{DD} variation. Measurement results demonstrate that both sub-0.3-V operation and sub-nW power can be achieved concurrently with a smaller area (0.045 mm^2), better FoM (-165.9 dB), a superior sensitivity of -66 dBm at 1 Kbps and a well V_{DD} robustness.

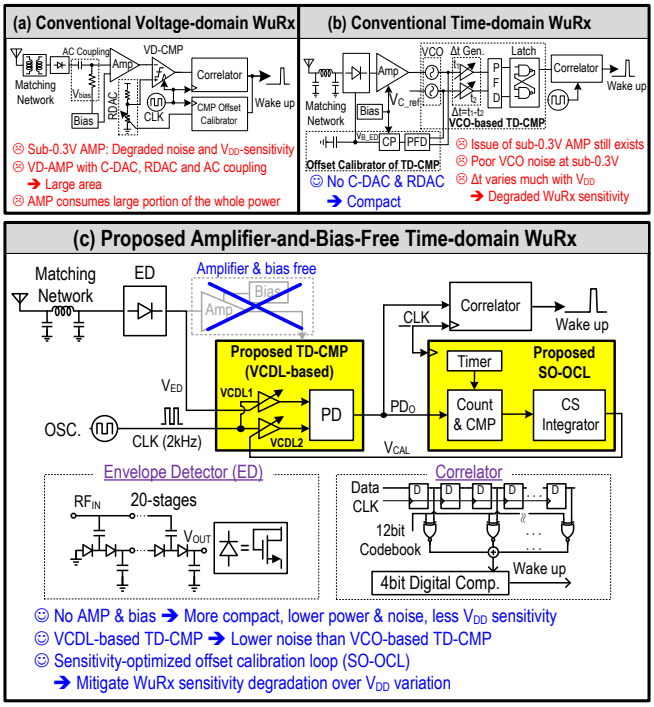


Fig. 1. Simplified block diagram: (a) conventional voltage-domain ED-first WuRx, (b) conventional time-domain ED-first WuRx, and (c) proposed amplifier-and-bias-free time-domain WuRx.

II. Design of The Proposed WuRx

A. Top Architecture

Fig. 1(c) shows the block diagram of our proposed amplifier-and-bias-free time-domain WuRx. It consists of a high-input-impedance 20-stages envelope detector with a off-chip π-type matching network, an on-chip 2-KHz ring oscillator (RO), a proposed VCDL-based time-domain comparator (TD-CMP), a developed sensitivity-optimized offset calibration loop (SO-OCL) including a timer, a counter,

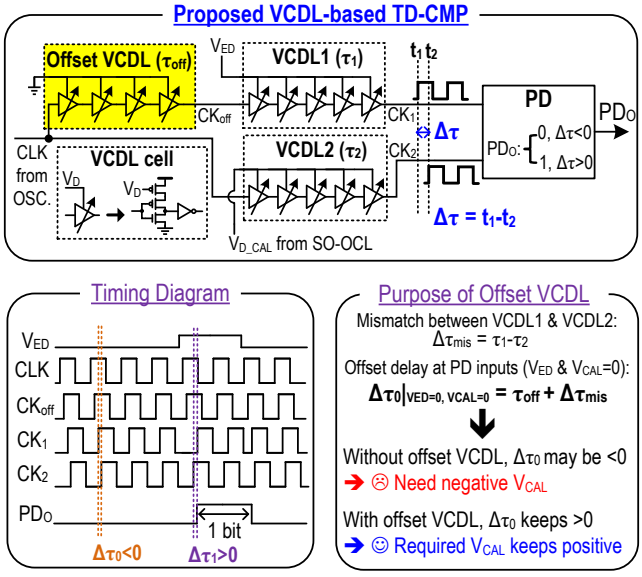


Fig. 2. Schematic of the proposed VCDL-based TD-CMP and its timing,and the explanation of the purpose of the offset VCDL.

a digital comparator and a charge-sharing (CS) integrator, and a 12-bit correlator with CMOS logic gates.

The overall operation principle is as follows. First, the ED with its input matching network demodulates the 433-MHz RF OOK signal with 1-Kbps data rate and outputs the demodulated OOK signal in voltage domain (V_{ED}). Then, the TD-CMP convert V_{ED} into a time difference $\Delta\tau$ by modulating the delay of VCDL1 through V_{ED}, and detect the polarity of $\Delta\tau$ to generate '1' and '0' output by a phase detector. Meanwhile, based on the TD-CMP output PD_O, the SO-OCL can adaptively tune the control voltage of VCDL2 (V_{CAL}) to the offset of two VCDLs and optimize WuRx sensitivity regardless of V_{DD} variation. Finally, a 12-bit correlator compares the TD-CMP output series with a dedicated wake-up pattern in the codebook, and a pulse will be generated and output as the wake-up indicator if the comparison matches. The RO, which oscillates at twice frequency of the input data rate, play the role of the global clock generator for the VCDLs, SO-OCL and correlator.

B. VCDL-based TD-CMP

Fig. 2 details our VCDL-based TD-CMP. The CLK signal is fed into two VDCL paths: one consists of VCDL1 and an offset VCDL with the total delay of ($\tau_1+\tau_{off}$), and the other one includes VCDL2 with the delay of τ_2. τ_1 is modulated by ED output voltage V_{ED}, and τ_2 is controlled by SO-OCL. The operation principle is illustrated in Fig. 2(bottom-left): when SO-OCL is settled, τ_2 is slightly higher than ($\tau_1+\tau_{off}$) so that the output of phase detector (PD) is zero with zero input of the WuRx (V_{ED}=0); if ED detects input bit 1, namely V_{ED}>0 and $\tau_2 < (\tau_1+\tau_{off})$, PD output goes to 1. Due to the sub-threshold operation, the VCDL current is sensitive to its tuning voltage, namely a high VCDL gain. Thus, the VCDL also plays the role of high gain AMP, enabling the removal of AMP without the penalty of sensitivity for lower power, smaller area and better V_{DD} robustness. As explained in Fig. 2(bottom-right), with offset VCDL, the settled V_{CAL} can be always positive to ensure the correct function of SO-OCL regardless the polarity of the delay mismatch between VCDL1 and VCDL2 ($\Delta\tau_{mis}$). This also enables DC-coupling between ED and VCDL without any reference voltage, hence avoiding bias circuit to generate V_{C_ref} in prior TD-CMP based WuRx [Fig. 1(b)] for small area.

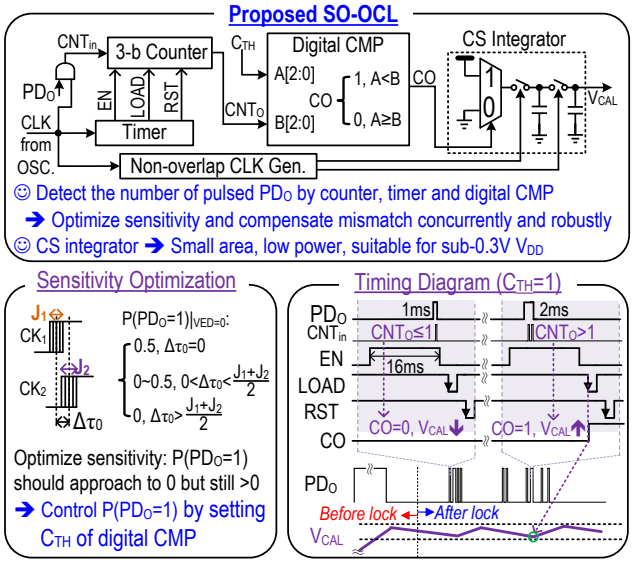


Fig. 3. Schematic of the proposed SO-OCL and its timing, and the principle of WuRx sensitivity optimization.

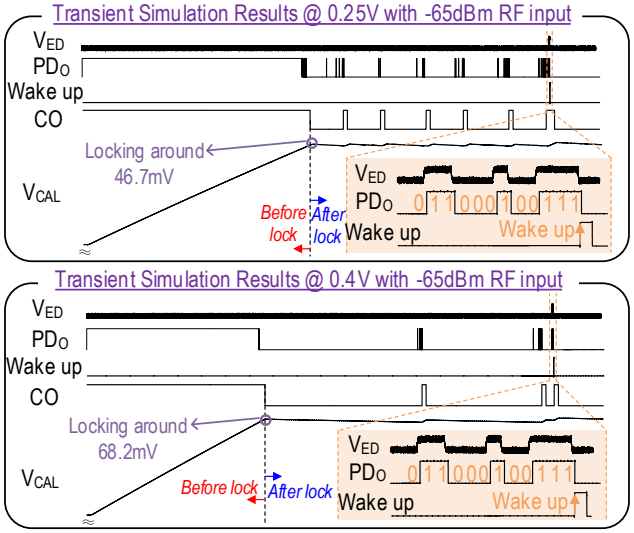
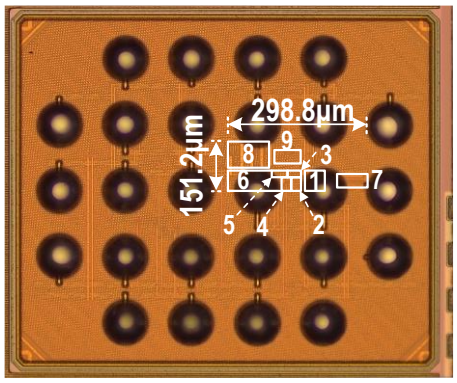


Fig. 4. Simulation results at 0.25-V and 0.4-V V_{DD}, respectively.

C. Sensitivity-optimized Offset Calibration Loop (SO-OCL)

With a time difference offset $\Delta\tau_0$ of the PD input at zero V_{ED}, which is mainly induced by the mismatch of VCDL, the minimal detectable power of the WuRx input signal is increased, causing degradation of WuRx sensitivity. Hence, the SO-OCL [Fig. 3(top)] is proposed to compensate such offset and optimize WuRx sensitivity concurrently by tuning τ_2 through V_{CAL}. V_{CAL} is adjusted based on the comparison result (CO) between the length of '1' of PD_O (CNT_O) and a threshold code C_{TH}. CNT_O is obtained by counting the pulsed PD_O in a specified period controlled by a timer. Thanks to its features of small area, low power consumption and suitability for sub-0.3-V operation, the charge-sharing (CS) integrator [16] is used to tune V_{CAL}, which increases (decreases) when CO=1 (0).

As analyzed in Fig. 3(bottom-left), if $\Delta\tau_0$ is calibrated to 0, the sensitivity even gets worse because the probability of PD_O=1 at zero V_{ED} [$P(PD_O=1)|_{VED=0}$] reaches its maximum value of 0.5 due to the jitter of VCDL (J_1 and J_2). In contrast, $P(PD_O=1)|_{VED=0}$ is absolutely zero if $\Delta\tau_0$ is obviously higher than $(J_1+J_2)/2$, also resulting in degraded sensitivity because the minimal detectable V_{ED} is increased. So, $P(PD_O=1)|_{VED=0}$



Time-domain CMP with SO-OCL:
1.VCDL, PD
2.Timer
3.Counter
4.Non-overlap CLK Gen.
5.Dig. CMP
6.CS Integrator

Others:
7.ED
8.Correlator
9.OSC.

Block	Time-domain Comparator	OSC.	Correlator	Total
Power	410.6 pW (44%)	63.4 pW (7%)	460 pW (49%)	0.93 nW

Fig. 5. Chip photograph and power consumption breakdown.

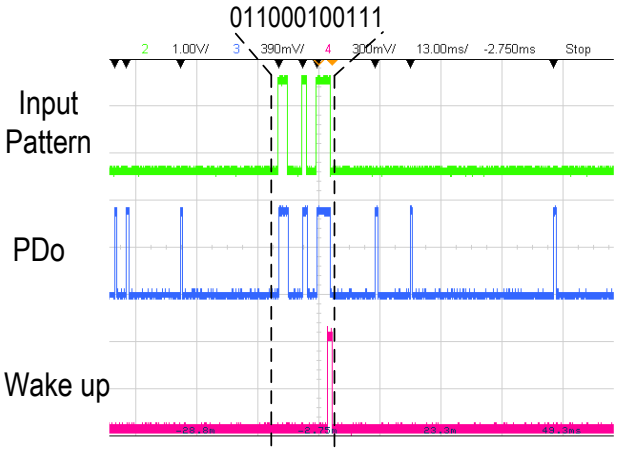


Fig. 6. Measured waveform.

should approach 0 but still be slightly higher than 0 to optimize sensitivity. This is done by manually tuning two extra VCDLs in prior TD-CMP based WuRx [Fig. 1(b)], leading to sensitivity degradation over V_{DD} variation because the delay of sub-threshold VCDL is very sensitive to V_{DD}.

Alternatively, our SO-OCL can adaptively control $P(PD_O=1)|_{VED=0}$, which is dominated by C_{TH} regardless of V_{DD} variation, thus improving the supply-voltage robustness. After careful simulation, we can get an adequate sensitivity when C_{TH}=1 with a counting period of 16 ms, as the timing shown in Fig. 3(bottom-right).

The operation process of the SO-OCL is as follows. Initially, with zero V_{ED} and $\tau_{off} > 0$, PD_O keeps 1 until $\tau_2 > (\tau_1+\tau_{off})$ in our TD-CMP. So, V_{CAL} gradually increases up. The SO-OCL starts to get into the locking state when the signal CO (Fig. 3 and Fig. 4) firstly goes to 0. At the locking state of SO-OCL, V_{CAL} keeps dynamically stabilized within a certain small voltage range [V_{CAL} gets increased (decreased) when $CNT_O > C_{TH}$ ($CNT_O \leq C_{TH}$)].

Fig. 4 presents transient simulation results with two different supply voltages, which matches well with the analysis of the operation process discussed before. Furthermore, V_{CAL} at the locking state is around 46.7 mV and 68.2 mV at V_{DD} of 0.25 V and 0.4 V, respectively, demonstrating the V_{DD} robustness of this work.

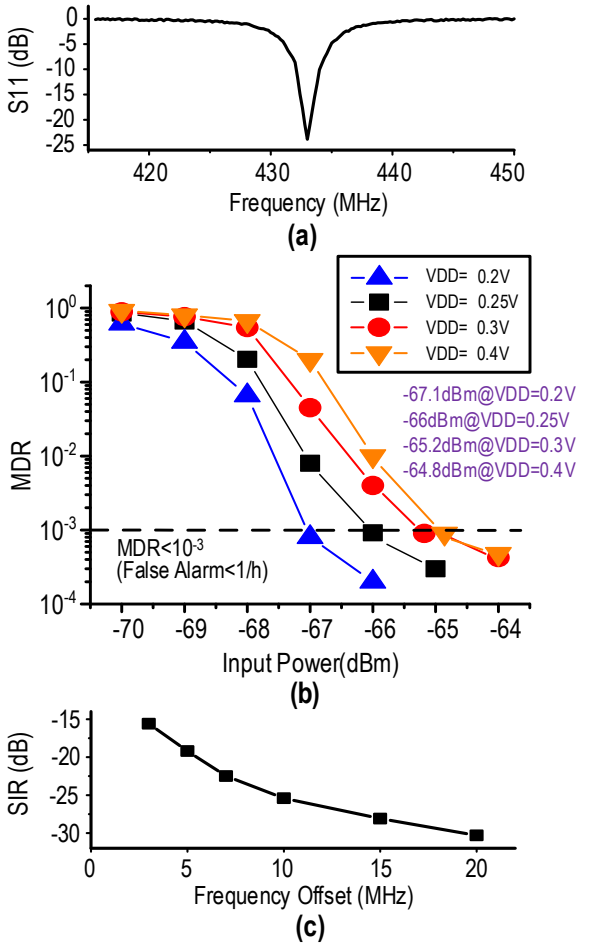


Fig. 7. Measured (a) S11, (b) MDR with 0.2~0.4-V V_{DD}, and (c) SIR.

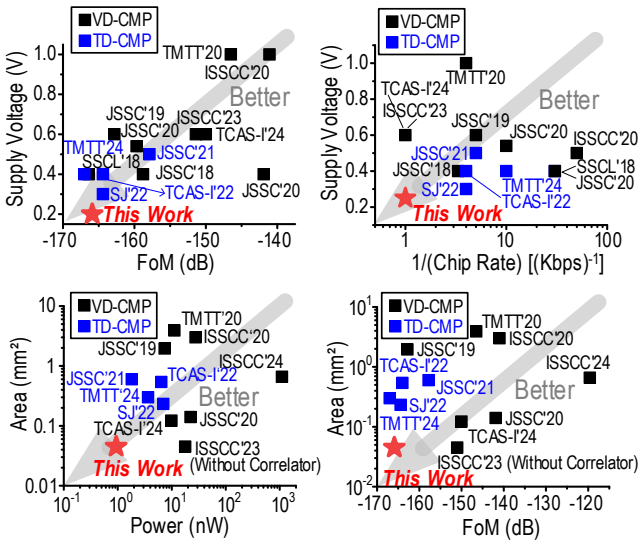


Fig. 8 Performance comparison with state-of-the-art WuRxs.

III. Measure Result

Fig. 5 exhibits our 40-nm CMOS wake-up receiver prototype. It consumes 0.93 nW at 0.25-V V_{DD} and occupies 0.045-mm^2 core area with 433-MHz carrier frequency and 1-Kbps chip rate of the input OOK signal. The measured waveform demonstrates the correct function, where the wake-up pulse is generated upon receiving the correct pattern, as shown in Fig. 6. In this work, the wake-up pattern is set to "111001000110", which has a duty cycle of 50% so as to achieve the largest detection margin in the presence of

TABLE I: PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WuRxs.

	This work	[9]ISSCC'24	[8]TCAS-I'24	[10]ISSCC'23	[14]TCAS-I'22	[13]SJ'22
Key Techniques	ED+TD-CMP (VCDL-based)	ED+AMP+VD-CMP	ED+AMP+VD-CMP	ED+BUF+VD-CMP	ED+AMP+TD-CMP (VCO-based)	ED+AMP+TD-CMP (VCO-based)
Process (nm)	40	40	65	65 LP	65	65 LP
V_{DD} (V)/V_{DD} range(V)	0.25/(0.2-0.4)	-	0.6/NA	0.6/NA	0.4/NA	0.3/NA
Modulation	OOK	OOK	OOK	OOK	OOK	OOK
Frequency (MHz)	433	433	900	920	434	434
Chip Rate (kbps)	1	1	1	1	0.25	0.25
Code Length (bit)	12	16	24	2	16	16
Power (nW)	0.93	1100	9.9	17.8	6.4	6.96
Passive Gain (dB)	28	-	29.6	-	25	24.7
Sensitivity (dBm)	-66	-51	-68	-60.4	-75	-75.8
Latency (mSec)	12	16	24	2	32.7	38.6
Normalized Sensitivity[1] (dBm)	-75.6	-60	-76	-73.9	-82.4	-82.9
SIR [3MHz off] (Cont. Wave) (dB)	-15.6	-	-22	-11	-15	-
FoM[2] (dB)	-165.9	-120	-156	-151.4	-164.4	-164.4
Area (mm^2)	0.045	0.66	0.122[3]	0.045[4]	0.54	0.232

1.Normalized Sensitivity = Sensitivity + 5log(Latency/1s)
2.FoM=Normalized Sensitivity + 10log(Power/1W)
3.Estimated from chip photo
4.Area without Correlator

interference [12]. Fig. 7(a) presents the measured S11. It shows -23.4 dB at 433 MHz. Besides, the π-type matching network contributes a passive gain of 28 dB at 433 MHz. The measured sensitivity (Fig. 7(b)) is -66 dBm at 0.25 V with the missed detection ratio (MDR) of $\leq 10^{-3}$, and it varies from -67.1 dBm to -64.8 dBm with V_{DD} range from 0.2 V to 0.4 V, showing robustness over V_{DD} variation. The MDR is tested with a 1-KHz with a 1-Kbps OOK-modulated wake-up pattern. The signal-to-interference ratio (SIR), which is tested using a continuous-wave interference at 3-MHz offset, is -15.6 dB with a MDR of 10^{-3}, as shown in [Fig. 7(c)].

Fig. 8 and Table I compare our work with prior state-of-the-art WuRxs. This is the first reported sub-0.3-V WuRx with sub-nW power. Our prototype consumes the lowest power and occupies the smallest area at the lowest V_{DD} with a better FoM and comparable sensitivity, compared to prior works. In addition, the chip rate is also among the highest reported to date.

IV. Conclusion

A amplifier-and-bias-free time-domain WuRx was proposed and implemented in a 40-nm CMOS process. Thanks to our proposed VCDL-based TD-CMP and SO-OCL, both sub-0.3-V operation and sub-nW power are achieved concurrently. Measurement results shows our prototype scores 0.93-nW power, 0.045-mm^2 core area, −165.9-dB FoM, and −66-dBm sensitivity at 0.25-V V_{DD}. Furthermore, this work also shows a well V_{DD} robustness.

Acknowledgment

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