

Negative Boosting Control of Channel Potential in Open Block Read Operation for 3D NAND Flash Memory

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Abstract—In this paper, we investigate the channel behavior in open block read operation for 3D NAND flash memory by using technology computer-aided design (TCAD) simulations. In the situation of an open block where the erased and programmed cells coexist, the difference of the channel potential at the cell string arises due to the difference of the cell pattern. This sudden change in channel potential generates hot carriers, and hot carrier injection (HCI) accelerated by the increased electric field causes read disturbance degradation. Additionally, the negative boosting of the channel potential causes unintended stress at the programmed cell region. To mitigate the read disturbance degradation, we propose an advanced scheme that controls the drain-select line (DSL) and the source-select line (SSL), as well as increases the word line (WL) discharge level, allowing the channel potential to recover more quickly.

Keywords—open block, read operation, hot carrier injection, electric field, negative boosting, read disturbance, DSL and SSL control, WL discharge level, channel recovery, technology computer-aided design simulations.

I. INTRODUCTION

To reduce the chip area and store more bits efficiently, the cell structure of NAND flash memories has been transitioned from 2D planar to 3D vertical structure [1]. In 3D NAND cell structure, NAND technology has advanced to further increase bit density and reduce the cell area by stacking the cells on the top of the peripheral circuits [2]. One of the significant challenges with the shift to 3D NAND is the increment in the number of word line (WL) layers which has resulted in larger block sizes and lower cell current. As the number of WL layers increases, the reliability characteristics can be degraded because cell current decreases, which lower the sensing margin [3]. Additionally, as the block size grows, the importance of disturbance increases [4]. The frequency of encountering unselected WLs also rises, leading to more unintended stress on the cells, which further accelerates the degradation of disturbance.

In addition to the architectural changes to 3D NAND, another critical development has been the shift towards multi-bit cells such as triple-level cell (TLC), and quad-level cell (QLC). Multi-bit cells allow for higher data density within each individual cell by storing more than one bit of data per cell [5]. Fig. 1 represents the threshold voltage (V_{TH}) distribution of the NAND cells for each multi-bit case. The gap margin refers to the region where the PV (Program Verify) states do not overlap, preventing errors from occurring. As the number of PV state increases, the gap

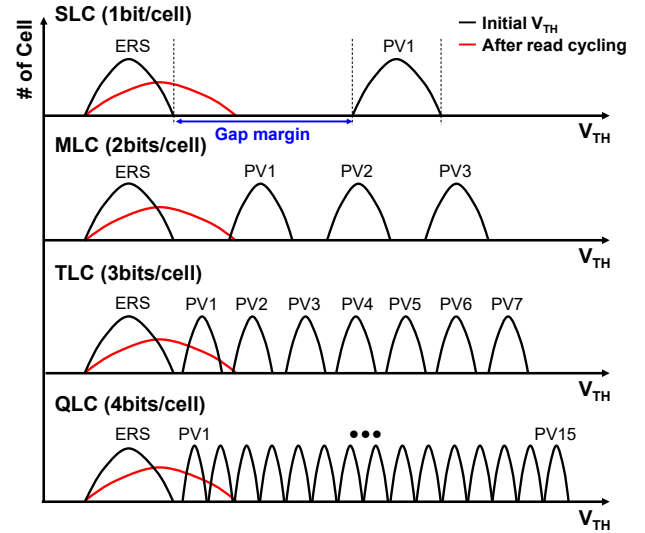


Fig. 1. The V_{TH} distribution of the NAND cells for each multi-bit case. As the number of bits per cell increases, the error rate of the data increases after read cycling.

margin is lowered, because the gap between the different states becomes smaller. This makes the cells more susceptible to the degradation of the reliability characteristics, especially the read disturbance. Compared to single-level cells (SLC), the probability of error bits occurring increases even with fewer read cycles, making the ability to manage read disturbance more critical.

The significance of read disturbance becomes more pronounced in open block situation, where the erased cells are remain in a block. Several previous papers have raised issues regarding the reliability problems in the open block operations in terms of the data retention and read disturbance [6], [7], [8]. To address the reliability degradation in open blocks, N. Papandreou et al. suggested the page grouping, as an effective approach to reduce the raw bit-error rate (RBER), by using read voltage (V_{READ}) calibration from NAND flash memory controller [7]. However, there are few research findings that analyze the device physics for the open block situation and attempt to improve the fundamental problems within the NAND flash memory itself.

Consequently, we focus on analyzing the physical phenomena occurring in the channel surface of the NAND cell string in an open block situation. The hot carrier injection (HCI) occurring in different bias potential of the channel can be a failure mechanism to degrade read disturbance [9]. We form an open block through partial programming, and perform read operation, conducting a

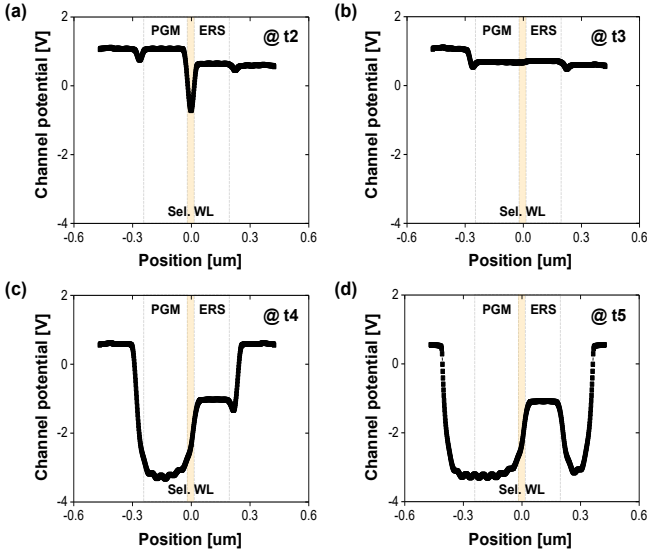


Fig. 4. The TCAD simulation results of the conventional scheme. It represents the channel potential according to the position in the y-direction at each time point. (a): t2, (b): t3, (c): t4, (d): t5.

order to determine whether the proposed scheme operates as intended.

III. SIMULATION RESULTS

A. Channel analysis of the conventional scheme

First of all, we analyze the channel behavior at the end of the read operation over time in the conventional scheme. Fig. 4 shows the simulation results that confirm how the channel potential changes at each time point. At the time of t1 and t2, V_{PASS} is applied to all of the Unsel. WLs, so the channel is connected BL and SL. However, Sel. WL cell has the V_{TH} higher than the V_{READ} applied to the gate, Sel. WL cell is in the turned-off state. Therefore, the localized channel of the Sel. WL cell is down-coupled [11]. At t3, the channel potential has little variation depending on the position, because all of the WLs including Sel. WL are equalized to V_{EQ} . The channel potential is partially down-coupled at t4, because all of the WLs are discharged from V_{EQ} to the ground. Due to the pattern difference of an open block, the channel of the programmed cell undergoes negative boosting, while the channel of the erased cell is less affected as it is connected to the SL. In this progress, a significant channel potential difference occurs across the Sel. WL. Finally, DSL and SSL are turned off at t5. At both ends of the cell string, a sharp distinction of the channel potential also occurs at each position. However, this can be easily resolved by placing dummy WLs near DSL and SSL, and adjusting the gate bias of dummy WL cells [12]. Therefore, this paper focuses on the physical phenomena occurring the only channel near the Sel. WL.

B. Validation the effect of the proposed scheme

Fig. 5 shows the simulation results of the proposed scheme which is turned off DSL and SSL earlier than the conventional scheme. The entire read timing diagram is shown in Fig. 5 (a). When all of the WLs are equalized to V_{EQ} level, DSL and SSL are discharged to the ground simultaneously. The goal of the proposed scheme is to turn

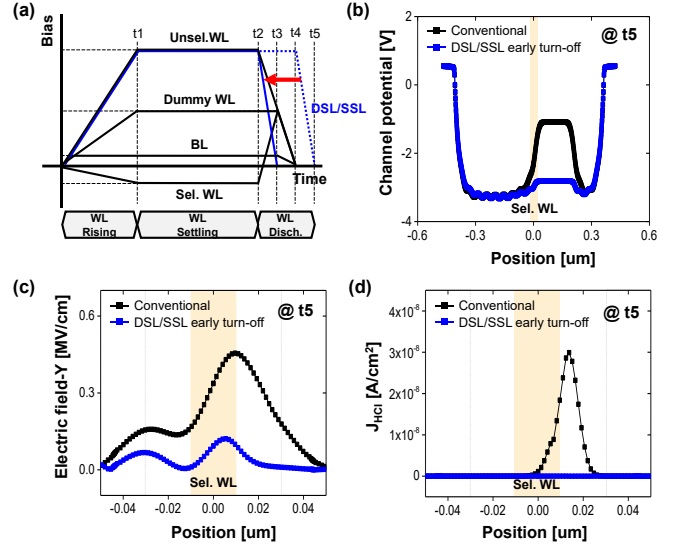


Fig. 5. The TCAD simulation results of the proposed scheme which is turned off DSL and SSL earlier than the conventional scheme. (a) A read timing diagram of the simulation. (b) Electrostatic potential of the Si channel. (c) Electric field in y-direction. (d) Current density of hot carrier injection according to the position at t5.

off DSL and SSL before WL is discharged, ensuring that the floating channel undergoes down-coupling in a nearly identical manner regardless of the pattern differences. The simulation result represents the electrostatic potential of Si channel at t5 is shown in Fig. 5 (b). Compared to the conventional scheme, the channel potential of erased region is also down-coupled. It can be seen that there is a little potential difference between the programmed and erased regions. In addition, it can be observed that the electric field in the y-direction decreases, and the HCI current density (J_{HCI}) caused by the band-to-band tunneling (BTBT) near the Sel. WL is almost removed at t5 from Fig. 5 (c) and (d) [10].

However, when applying the only previously mentioned scheme, there is another issue that the overall channel potential can be more down-coupled, resulting in an increased negative boosting. The simulation results of the additional scheme to resolve this issue are shown in Fig. 6. The entire read timing diagram for the simulation is shown in Fig. 6 (a). The diagram shows that a certain level of bias is maintained on the WLs to reduce the negative bias in the channel. And, the simulation result of the channel potential is shown in Fig. 6 (b). As the discharge voltage (V_{DISCH}) applied to the WLs is increased, the channel potential can be brought closer to the equilibrium state. In Fig. 6 (c) and (d), it can be seen that the electric field in the y-direction and the J_{HCI} also decreases as V_{DISCH} is increased. Through these simulation results, turning off DSL and SSL early and increasing the V_{DISCH} helps to mitigate the difference of Si channel characteristic caused by pattern variations at the open block situation, thereby preventing the degradation of NAND reliability characteristics.

C. Channel recovery of the proposed scheme

Fig. 7 shows the simulation results to observe the changes of the Si channel characteristics when the channel recovers after the read operation is completed. The entire sequence of the simulation is shown in Fig. 7 (a). After all of the read operations are completed, the channel situation is

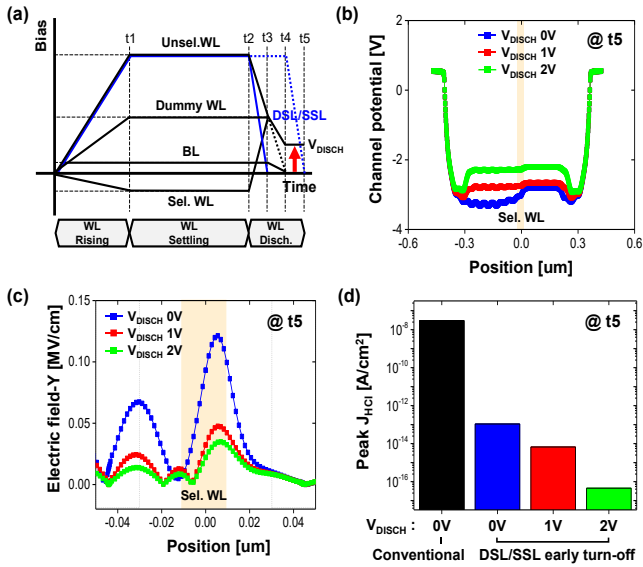


Fig. 6. The additional TCAD simulation results to overcome the negative boosting of the channel potential. (a) A read timing diagram of the additional simulation. (b) Electrostatic potential of the Si channel. (c) Electric field in y-direction according to the position at t5. (d) Current density of hot carrier injection for each case.

monitored up to 1ms in 100us intervals. According to the Fig. 7 (b) and (c), the channel potential is higher than that of Fig. 6 (b). The electrostatic potential of the channel is relaxed due to the leakage current of the DSL and SSL, and the recombination of electrons and holes of the channel. The channel potential is recovered more quickly when the higher V_{DISCH} is applied to the WLs, because the initial voltage level of the channel is increased. As a result, the proposed scheme reduces read disturbance degradation while shortening the time it takes for the channel to recover after the read operation is completed.

IV. CONCLUSION

In this paper, we investigated the channel behavior in open block read operation. And then, we proposed an advanced scheme to reduce the difference of the channel potential at the open block situation. To improve the read disturbance and HCI issue of the open block, we suggested that DSL and SSL are turned-off before all of the WLs are discharged. And also, increasing the V_{DISCH} helps to mitigate the channel potential difference, and reduce the negative boosting. Furthermore, the time to recover the channel potential in idle state is much shorter than that of the conventional scheme. The significance of this paper lies in preventing the read disturbance degradation caused by the partial down-coupling phenomenon of the Si channel at the open block case within NAND flash memory itself.

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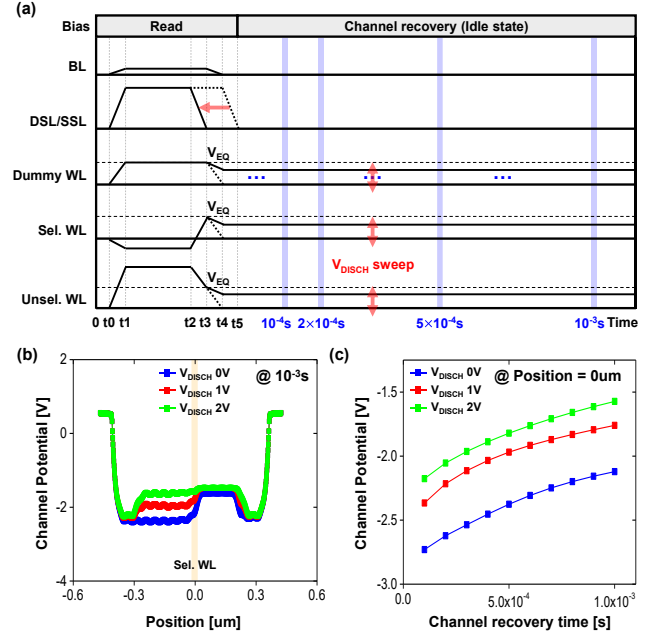


Fig. 7. The TCAD simulation results of the channel changes when the channel recovers after the read operation is completed. (a) The entire timing diagram of the simulation. (b) The electrostatic potential of the Si channel surface at 10^{-3} s. (c) The channel potential according to the channel recovery time.

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