A 14.9-to-16.9GHz Cryogenic PLL with Digitally Tunable-K_{vco} for Quantum Computing

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***Abstract*— A fully differential cryogenic PLL with tunable K_{vco} in a 14nm CMOS FinFET for transmon qubit control electronics is realized using a digitally controlled varactor with independent optimization of the common mode ($K_{VCO,CM}$) and differential VCO gains ($K_{VCO,DIFF}$) and $K_{VCO,DIFF}$ linearization. Operating at 15.5GHz, the PLL achieves a $K_{VCO,DIFF}$ of 81.4MHz/V and phase noise (PN) of -135.4dBc (10MHz offset) at an ambient temperature of 6K.**

Keywords—cryogenic CMOS, RF AWG, ultra-low power, qubit controller, varactor linearization

INTRODUCTION

A clock source that operates at cryogenic low temperatures (LT) and achieves low PN is a key component for the development of highly-integrated cryo-CMOS qubit interface electronics for realizing large scale quantum computing systems. The use of highly integrated cryo-CMOS circuits for control and readout of superconducting qubits reduces the number of RF cables between the quantum processor and room temperature (RT) electronics. Fully integrated cryogenic PLLs can generate and distribute clock signals for downconversion and upconversion mixers used in qubit readout and control [1]. Based on the model in [2], the proposed PLL in this work could allow an error rates < 10^{-4}, which is lower than the threshold for fault tolerant quantum operations. The cryo-PLL presented in this paper is low-power and operates from 14.9-16.9GHz with a tunable VCO gain K_{vco} satisfying performance requirements with the following key features: (a) LT-friendly digitally programmable varactors, realized using switchable metal capacitors and configurable MOS transistor on-resistance, (b) linearization of the $K_{VCO,DIFF}$ varactor to enable peak $K_{VCO,DIFF}$ reduction to reduce VCO PN, and (c) independent tuning of $K_{VCO,CM}$ and $K_{VCO,DIFF}$, reducing the impact of common mode noise on the PLL PN. The proposed varactor and tuning schemes also serve to reduce the $K_{VCO,DIFF}$ variability between RT and LT, which can be as large as 5x [3], offering a path to improved correlation between RT and cryogenic part screening results.

I. PLL DESIGN

For transmon qubit dispersive readout, a low IF or direct conversion IQ receiver using quadrature LOs generated by a divide-by-2 circuit enables power savings and increases isolation between the VCO and the RF signals. For signal generation above 15 GHz, only two cryogenic VCOs have been reported [3, 5]; but they do not address CMOS modeling shortcomings at cryogenic temperatures. The proposed PLL uses a fully differential integer-N design (Fig. 1) to reduce the charge-pump (CP) and loop filter (LF) noise sensitivity.

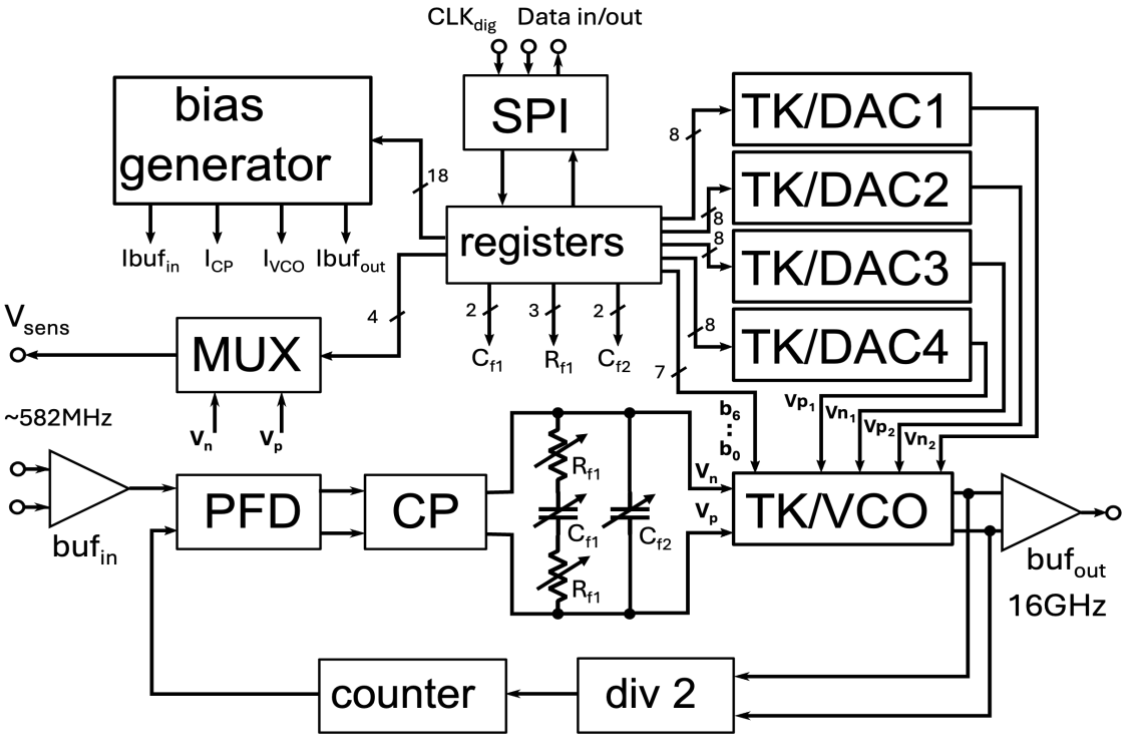

Fig. 1. Differential PLL with tunable VCO gain.

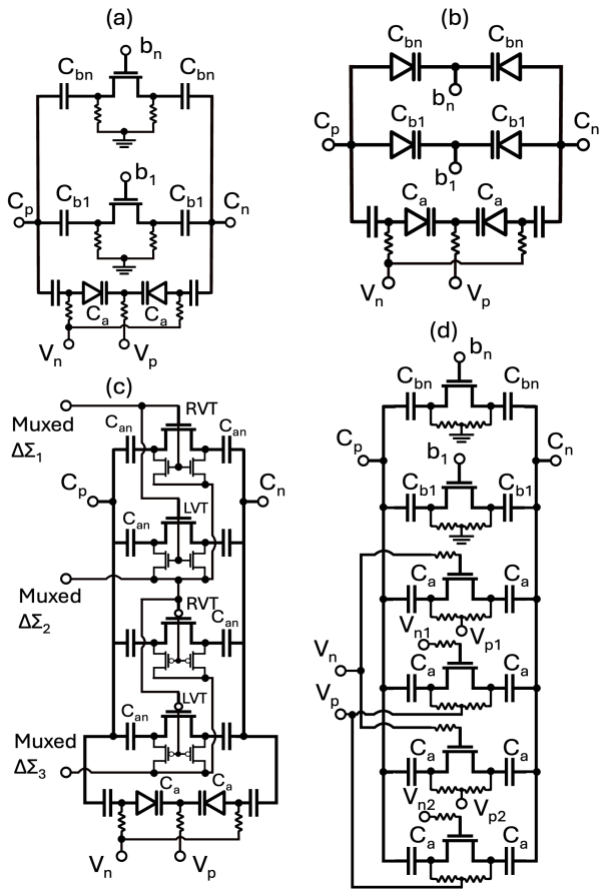

Fig. 2. Varactor gain reduction using (a) switched cap bank [6], (b) digitally controlled varactor bank [7], (c) folded analog controlled switched cap [8], and (d) proposed scheme using switched cap bank and linearized analog controlled switched cap varactors.

The use of low voltage supply in advanced CMOS technologies leads to high varactor voltage gain $\Delta C/\Delta V$ resulting in high gain VCO and excess phase noise. As shown in Fig. 2 several differential varactor design techniques have been developed to reduce the varactor gain. For CMOS design the varactor gain is high only in the center of the tuning curve. Therefore, the main idea is to divide the capacitor in multiple capacitors where most of them are turned on or off. These digitally controlled varactors are biased at the edge of the tuning curve where the varactor gain is low. The analog tuning is achieved with a differential varactor covering a fraction of the total capacitance thus decreasing the K_{vco}. Fig. 2(a) shows the baseline scheme of varactor element along with switchable capacitor arrays that implement coarse tuning [6]. Fig. 2(b) shows the use of a digitally controlled varactor bank which has the advantage of providing a good matching between the LSB and analog varactor [7]. Fig. 2(c) implements a continuous linear varactor using a large array of switched cap varactors with a voltage variable resistor realized using MOS transistors in linear region driven by a ΔΣ. It uses NFET and PFET and multiple threshold voltages FET to linearize the switched cap varactor [8]. A major limitation of the linearization schemes presented in 2(c) is the high PVT variation of K_{VCO} which is unsuitable for operation over wide temperature range. To address these challenges, we propose a linearization technique [9] where the same type of transistor is used for both branches and the differential control voltage is provided between the gate and source terminals of the transistor. By minimizing the K_{VCO} variation over temperature, it provides robust PLL stability over temperature.

The LC-VCO core (Fig. 3 (a)) is implemented with a cross-coupled current reuse g_m cell with 7-bit binary weighted capacitor bank (C_{b0} to C_{b6}) and two differential varactors with separately controlled adjustable thresholds to achieve nearly constant $K_{VCO,DIFF}$ across a wide temperature range. This approach supports achieving small tuning ranges and lower PN per coarse capacitor setting. A 2nd harmonic trap at the PFET sources was implemented with L_2 and C_2 to reduce jitter.

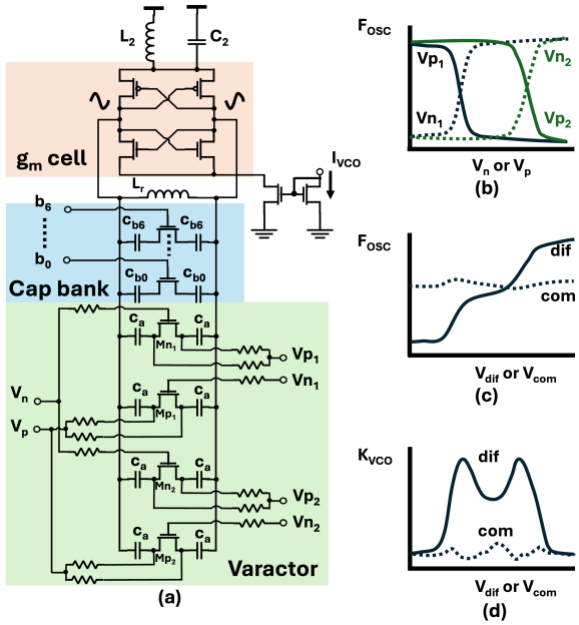

Fig. 3. VCO architecture with digitally switched capacitor bank and linearized analog controlled differential switch cap varactors. Showing differential and common mode tuning and linearization concept.

The design uses four compact 8-b DACs that produce low noise DC voltages (V_{p1}, V_{n1}, V_{p2}, V_{n2}), thus enabling realization of a VCO with independently tunable $K_{VCO,DIFF}$ and $K_{VCO,CM}$. A divide-by-2 circuit is used to generate quadrature LO signals. The VCO, CP, LF, and input and output buffers' biases are digitally programmable to compensate for the FET V_T shift between ambient and cryogenic temperature.

II. Differential Varactor with Linearization

The lack of accurate cryogenic CMOS models presents challenges in designing a low tuning range accumulation varactor that achieves required frequency overlap with the capacitor bank C_{b0}. To address this challenge, the same structure as was used for the C_{b0} digital capacitor bank was used for the varactor design (Fig. 3 (a)). The value of capacitor C_a is identical to that of C_{b0}, therefore, when all 4 varactors are on, the total varactor capacitance is 4x higher than Cb_0, thus guaranteeing acceptable frequency overlap from one frequency band to the next. The negative varactor control V_n is connected to the LVTNFET gate of 2 identical varactors, where the Mn_1 and Mn_2 source and drain are

connected to the 8b DACs generating the Vp_1 and Vp_2 voltages. When V_n-V_{p1} is lower than V_T, Mn_1 is off, and C_a is in series with the extrinsic parasitic capacitances C_{gsx} and C_{gdx}. When V_n-V_{p1} is higher than V_T, Mn_1 is on, and C_a is in series with the transistor on-resistance. By increasing Vp_1 from 0 to AVDD, the effective threshold voltage, V_T, can be changed from V_T to AVDD+V_T. Fig 3 (b) shows the frequency variation as either of the analog control voltages for the varactors M_{nx} or M_{px} is swept using V_n or V_p, respectively, while the other varactors are kept off. With 2 varactors Mn_1 and Mn_2, we can set the off-to-on transition voltage to be below or above the common mode voltage AVDD/2 (Fig. 3 (b)). For the design of the complementary varactor, the same capacitor C_a and same LVTNFET are used for each segment. However, V_p, the filtered charge pump analog control voltage, is now connected to the source and drain of Mp_1 and Mp_2, and the gates of those devices to the tuning voltages Vn_1 and Vn_2. When V_p is increased, the oscillation frequency increases when V_p-Vn_1 or V_p-Vn_2 is equal to the transistor V_T. We set the same transition voltage for Mn_1 and Mp_1, and Mn_2 and Mp_2, respectively, to minimize $K_{VCO,CM}$ (F_{VCO} vs V_{CM}), as shown in Fig. 3 (c). One drawback of using an NFET switch as a varactor is its sharp frequency-versus-control voltage transition; however, by using multiple NFET switches and by tuning their V_T values as described above, $K_{vco,diff}$ can be linearized. Linearization can be optimized by controlling the V_T values to achieve the desired separation between the two peaks of the varactors' tuning curves (Fig. 3 (d)).

III. Measurements

The PLL occupies 790um x 646um; the four K_{vco} tuning DACs occupy 166um x 70um (~1.4% of the total chip area). The PLL was packaged and inserted in a socket mounted on

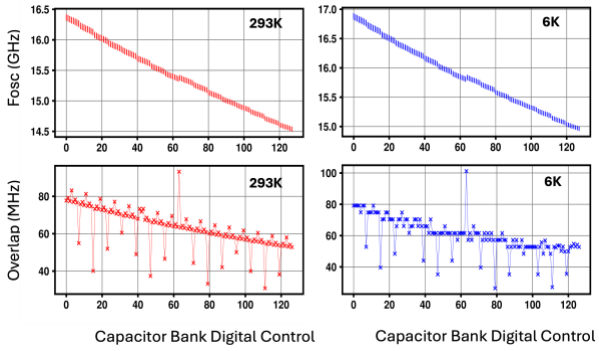

Fig. 4. Measured frequency versus digital and analog control codes for the capacitor ay 293K and 6K.

a PCB and was tested at both 293K and 6K, the latter in a He-cooled cryostat. The PLL operated between 14.5-16.4GHz at 293K and 14.9-16.9GHz at 6K (Fig. 5); the 520MHz frequency increase at 6K is attributed to substrate freeze-out which increases the inductor's self-resonant frequency. The measured within-band frequency tuning range is between 68 and 94 MHz at 293K and 64 and 101 MHz at 6K. Average frequency band overlap between 55 and 80MHz is achieved for all 128 bands at both 293 and 6K. Fig. 5 shows the result of linearization optimization for 3 different settings, indicating the reduction of peak K_{vco} by at least 2X ($K_{vco,diff}$ variation: 294.7➔156.1MHz/V at 293K and 194.6➔81.4MHz/V at 6K). The tuning curve shifts by <54mV between 293 and 6K leading to nearly same

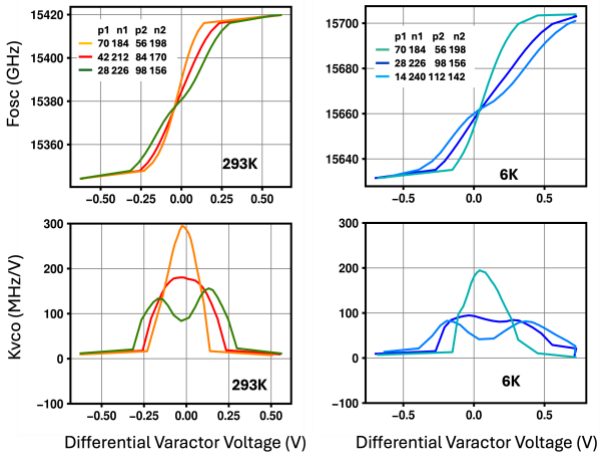

Fig. 5. Measured frequency and VCO gain versus differential varactor voltage at 293K and 6K for three different vectors {(p1, n1), (p2, n2)}.

linearization settings for both temperatures, promising to simplify the test/screen process.

The measured PLL PN at 293 and 6K is shown in Fig. 6; the out of band PLL PN at 10MHz offset frequency improves by 10.5dB from 293K to 6K due to the increase in resonator Q and decrease in NFET thermal noise. The in-band PLL PN at 100KHz improves only by 3.3dB from 293 to 6K due to the increase in NFET flicker noise at 6K.

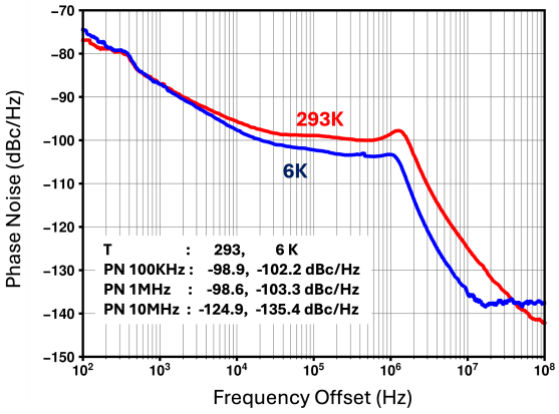

Fig. 6. PLL phase noise at 15.3GHz from 100Hz to 100MHz measured at 293K and 6K.

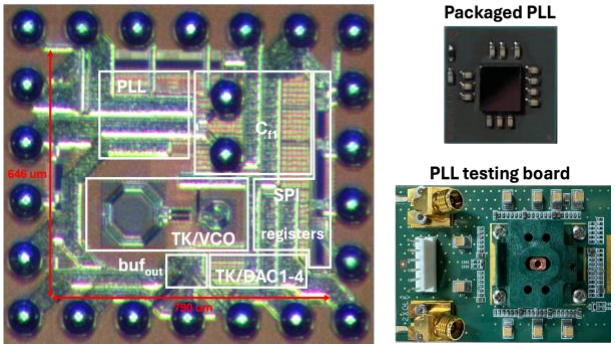

Fig. 7. Die photo of the PLL IC fabricated in 14nm CMOS, corresponding package, and test board.

Table-I. Performance comparison with state-of-the-art cryogenic VCO and PLL

		This Work		JSSC'23 [4]		ISSCC'22 [5]		ISSCC'23 [3]	
Architecture		Tuned-K_{vco} Analog PLL		Integer-N DAPLL		LC-VCO		LC-VCO	
Technology		CMOS 14nm FinFET		CMOS 40nm		SiGe 130nm		CMOS 65nm	
VCO type		LC tuned-K_{vco} VCO		LC-VCO		Class B/C mode switching		Class F	
Core Area VCO/PLL [mm²]		0.048 / 0.51		0.11 / 0.67		0.05		0.093	
Supply [V]		0.75 – 0.9		1.1		1.35-1.4		0.63-1.2	
Temperature [K]		293	6	300	4.2	295	3.5	300	4.2
Freq [GHz]		14.50~16.41	14.93~16.93	8.9~11.1	9.4~11.6	13.4~17.0	13.9~18.1	12.3~15.8	12.8~16.5
Center Freq drift over T [%]		3.1		5		5.3		4.3	
Peak K_{vco} [MHz/V]	**No Linearization**	294.7	194.6	N/A	N/A	N/A	128	N/A	210~380
	With Linearization	156.1	81.4	N/A	N/A	N/A	N/A	N/A	N/A
Phase Noise [dBc/Hz]	**100KHz**	-98.9 at 15.5GHz	-102.2 at 15.5GHz	-130.4 at 2.5GHz	-132.7 at 2.5GHz	-88.5~-82.9	-93.1~-84.2	-90.6~-86.3	-90.7~-84.1
	10MHz	-124.9 at 15.5GHz	-135.4 at 15.5GHz	-142.5 at 2.5GHz	-149.0 at 2.5GHz	-132.6~-123.1	-141.7~-133.6	-138.0~-135.2	-140.1~-135.3
Power VCO [mW]		0.57	0.9	3.1	1.7	3.55	3.08	17	1.1
FoM VCO at 10MHz [dB]		191	200	186	195	181~190	193~201	186~188	197~202
Power PLL [mW]		1.84	2.8	4	2.7	N/A	N/A	N/A	N/A
RMS Jitter, σ_j (fs) [Integ. Bandwidth]		239 [10KHz-30MHz]	124 [10KHz-30MHz]	75 [10KHz-30MHz]	38 [10KHz-30MHz]	N/A	N/A	N/A	N/A
FoM PLL [dB]		250	254	256	264	N/A	N/A	N/A	N/A

FoM VCO = $|PN| + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(Pdc/1mW)$ FoM PLL = $|20\log_{10}(\sigma_j/1s)| - 10\log_{10}(Pdc/1mW)$

The VCO and PLL consume 900µW from 0.75V and 2.4mW from 0.9V, respectively, at 6K. Fig. 7 shows the die photo of the 14nm CMOS PLL prototype along with package and testing boards.

Compared to previous SoTA cryogenic PLLs, the measured PLL exhibits a 5dB higher VCO FOM than [4] at RT and LT. The VCO FoM is 1dB higher than [3, 5] at RT. The PLL in [4] shows 6 to 10dB FOM difference between RT and LT. With linearization, the measured peak $K_{VCO,DIFF}$ of 81MHz/V is 1.6x lower at LT than SoTA VCO [5] as shown in table-I. The peak $K_{VCO,DIFF}$ between 293K and 6K varies by 1.9x and 1.5x with or without linearization, respectively, and the center frequency drift from RT to LT is only 3.1% versus 4.3% for previous work [5].

IV. Conclusion

A low-power fully-differential CMOS PLL that features independently tunable $K_{VCO,DIFF}$ and $K_{VCO,CM}$ using digital control to avoid uncertainties of varactor modeling at LT is presented. It uses similar transistors in linearization segments leading to minimum variation of K_{VCO} over temperature, leading to robust PLL stability. This should enable the screening of PLL parts at RT. It achieves <-135dBc/Hz PN at 10MHz offset 124fS jitter and 254dB FOM. Compared to the previously reported designs, this work provides the lowest variation of $K_{VCO,DIFF}$ over a wide temperature range (from 293K to 6K).

V. References

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