An 80 mV 0.54 nW, 32 kHz Crystal Oscillator Using Capacitive Positive Feedback in 180 nm CMOS for Real-Time Clock Applications

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***Abstract*—This paper presents an ultra-low voltage (ULV) and ultra-low-power (ULP) 32 kHz crystal oscillator (XO) designed in 180 nm CMOS technology for real-time clock (RTC) applications in energy-harvesting Internet of Things (IoT) systems. The proposed XO features a capacitively-coupled positive feedback transconductance (g_m) cell with 4 transistors and 2 capacitors, enabling operation at an ultra-low supply voltage of 80 mV while consuming only 0.54 nW of power at 37 °C. The other operating mode incorporates on-chip regulation circuits with a higher voltage of 240 mV, allowing this work to operate in a wider range of temperatures (-20 °C~85 °C). Compared to prior work, this work offers the lowest power consumption at 80 mV, advancing the feasibility of autonomous, long-term RTC solutions.**

***Keywords*— ultra-low voltage, ultra-low-power, 32 kHz crystal oscillator, real-time clock, energy harvesting**

I. Introduction

Real-time clocks (RTCs) based on 32.768 kHz (32 kHz) crystal oscillators (XOs) are widely used as wake-up timers in wireless sensor nodes for Internet of Things (IoT) applications. IoT sensor nodes use these wake-up timers to duty cycle the power-hungry components, like radios and processors, hence extending their battery lives. The effectiveness of this method depends on both the XO's power consumption and its timing accuracy: being the only always-on component, the XO's power accounts for a substantial fraction of the system's total power, yet timing inaccuracies will lead to wrong wake-up times, wasting power on the system-level for proper synchronization [1]. This has motivated much recent research in ultra-low-power (ULP) crystal oscillator design [2-6].

Leveraging locally harvested energy can further extend the battery life of these wireless IoT sensor nodes. Typical harvested energies have a power level of 8.75 µW, but the voltage can be as low as 350 mV (for instance, from a photovoltaic (PV) cell) [7]. This is especially the case for the implantable Internet of Medical Things (IoMT) [8], within which battery life is the utmost concern. Yet biopower harvesting *in vivo* is even more challenging. For instance, the open circuit potential generated electrochemically from adenosine triphosphate (ATP), if harvested, is less than 80 mV [9]. Ultra-low voltage (ULV) RTCs that can effectively use this low voltage can thus reduce

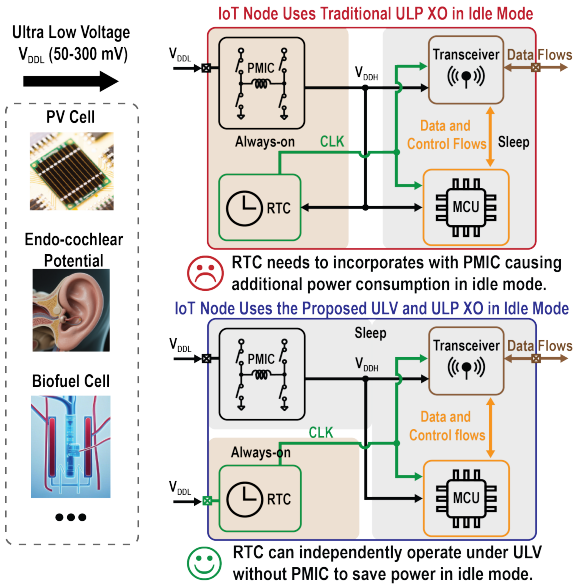

Fig. 1. Proposed ULV and ULP RTC for IoT applications.

system complexity during idle mode, allowing accurate and autonomous operations with time stamps, expanding the effectiveness in such systems, as illustrated in Fig. 1. However, there is a limited amount of research focusing on ULV XOs. Most recent sub-nW XOs typically operate with supply voltages over 0.38 V [3-6], and their complex circuit design makes them challenging to operate at ULV. The ULV XO presented in [2] can operate at 60 mV, however, it consumes 2.26 nW of minimum power and operates with a constrained operating temperature range (25 °C~62 °C), limiting its applicability.

This paper presents a ULV and ULP XO incorporating a sustaining transconductance (g_m) cell with 4 transistors (4T) and 2 capacitors (2C) in 180 nm CMOS technology. A positive feedback loop is created to enhance g_m by capacitively coupling the signal back to the bulk of the transistors. The proposed design incorporates two operation modes, covering different application scenarios. The ULV mode uses only the core 4T-2C components, achieving an 80 mV of ultra-low supply voltage

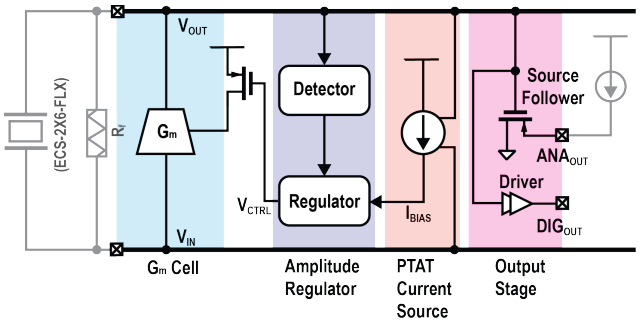

Fig. 2. Top level of the proposed crystal oscillator.

within typical body temperature range (37 °C~70 °C) while consuming only 0.54 nW of power at 37 °C. The second mode, referred to as wide-temperature-range (WTR) mode, incorporates additional on-chip supply regulation circuits, allowing the proposed XO to operate reliably over a temperature range from -20 °C to 85 °C with a higher supply of 240 mV, and achieves a power consumption of 1.55 nW at 25 °C room temperature.

II. Overview of the Operation

The proposed XO top-level diagram is depicted in Fig. 2. When operating in the deep sub-threshold region, the transconductance g_m of the transistors exhibits an exponential dependence on supply voltage. Hence, the most critical challenge in ULV operation is to obtain enough g_m to produce sufficient negative resistance to sustain the oscillation in the crystal. The g_m-cell in this work achieves effective g_m boosting by using a positive feedback loop, ensuring the ULV mode down to 80 mV, targeting IoMT applications that offer a stable operating temperature.

The other challenge in ULV operation is the g_m's strong dependency on temperature, which becomes critical when the XO is deployed in a generic IoT device working in outdoor environments. A separate WTR mode is included to address this problem. In the WTR mode, the amplitude of the XO's output, V_{OUT}, is extracted to generate a control voltage V_{CTRL} to form a negative feedback loop that limits the current supply to the g_m-cell. Thus, low-temperature-induced g_m reduction can be compensated internally by a higher bias current. A minimum of 240 mV of supply voltage is required to ensure operation down to -20 °C. The PTAT current source provides bias current I_{BIAS} for the regulator. The feedback resistor R_f establishes a defined dc voltage for V_{IN}, facilitating the startup of the oscillator.

III. Circuit Overview and Implementation

A. 4T-2C positive feedback g_m-cell

The idea of using positive feedback to boost g_m at ULV was previously demonstrated in [2]. However, a problem with the conventional Schmitt trigger is that there is a non-negligible turn-on current caused by transistors M_3 and M_6 in oscillator applications, as illustrated in Fig. 3(a). This contributes to the high power consumption observed in [2]. To address this problem, the proposed capacitively coupled positive feedback

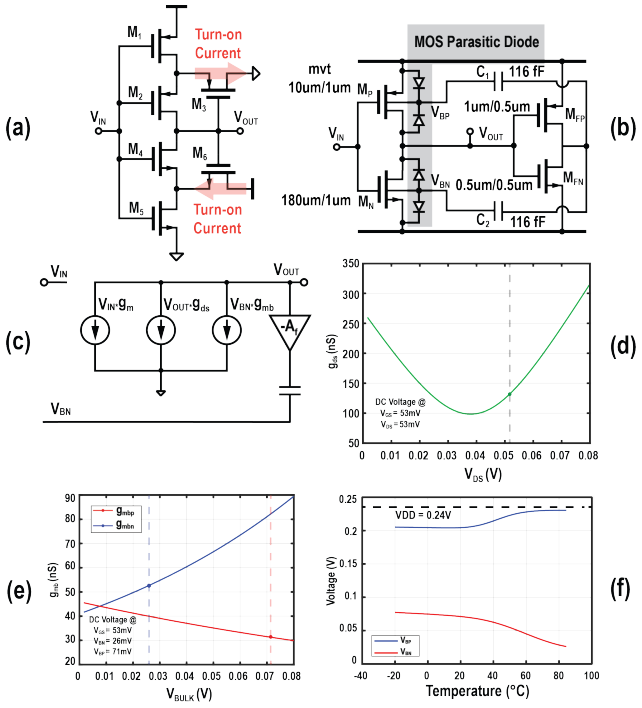

Fig. 3. (a) Schematic of convential 6T Schmitt trigger. (b) Schematic of proposed 4T-2C positive feedback g_m-cell. (c) Small signal model of the g_m-cell. (d) Simulation results of g_{ds} (e) Simulation results of g_{mbp} and g_{mbn}. (f) Simulation results of V_{BP} and V_{BN} across different T.

g_m-cell employs a two-inverter topology, improving energy efficiency compared to the conventional Schmitt trigger. The circuit diagram and component parameters are depicted in Fig. 3 (b).

The four transistors in the circuits are arranged as two inverters. The first inverter composed of M_P and M_N resembles the traditional Pierce oscillator, with the bulk of the M_P and M_N in the inverter available as the back gate for g_m boosting. It is designed to provide a sufficient equivalent transconductance $G_{m,eq}$ for negative resistance [10]. The second inverter, comprising M_{FP} and M_{FN}, provides feedback signals to bulk terminals of M_P and M_N through capacitors C_1 and C_2. This inverter operates with a negligible load because the other sides of C_1 and C_2 connect to the bulk terminals, that see a high equivalent resistance from the bulk diodes. Consequently, small transistor sizes are selected to minimize power consumption while maintaining sufficient driving capability. The small signal model of the g_m-cell is shown in Fig. 3 (c), from which we can obtain the $G_{m,eq}$ from V_{IN} to V_{OUT}:

$$G_{m,eq} = g_m/(1 - A_f \frac{g_{mb}}{g_{ds}}) - (1 - A_f \frac{g_{mb}}{g_{ds}})g_{ds} \quad (1)$$

Where A_f is the absolute value of the voltage gain of the feedback inverter, which is designed to be approximately 0.25. The transconductance parameters (g_m, g_{mb}, g_{ds}) are contributed by M_P and M_N together. Fig. 3 (d) and (e) present the simulated results of the transconductance parameters under an 80 mV

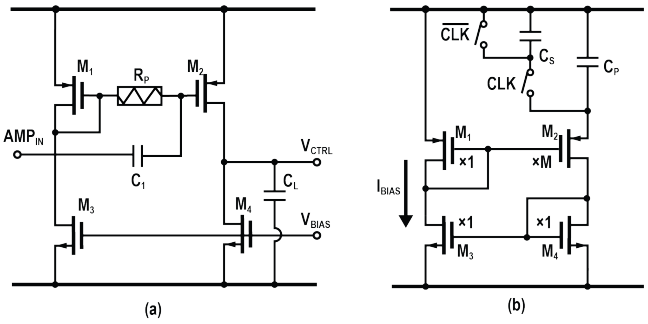

Fig. 4. (a) Schematic of the amplitude regulator. (b) Schematic of the PTAT current source.

supply voltage. At dc, V_{IN} and V_{OUT} are 53 mV (defined by the feedback resistor R_f mentioned in Section II), leading to g_{ds} = 137 nS. V_{BP} and V_{BN}, settled by the leakage currents from bulk diodes, are 72 mV (g_{mbp} = 31 nS) and 26 mV (g_{mbn} = 53 nS), respectively. Thus, the g_{mb} (g_{mbp} + g_{mbn}) sums up to 83 nS. The loop gain ($A_f \cdot g_{mb}/g_{ds}$) is calculated as 0.15, which is below 1 to guarantee stable positive feedback operation. This results in a 30.6% enhancement in $G_{m,eq}$ (517 nS from simulation) compared to a standard inverter implementation.

Another benefit of the capacitor-coupled feedback path is that it can help compensate for the temperature sensitivity of $G_{m,eq}$. Since the bulk potentials, V_{BP} and V_{BN} of M_P and M_N, are exclusively determined by the I-V characteristics of the bulk diodes, temperature will influence their value through the changes in these diodes' current. Fig. 3 (f) shows the simulation results of V_{BP} and V_{BN} across temperatures ranging from -20 °C to 85 °C. As temperature decreases, the dc operating point of V_{BP} will decrease, and that of V_{BN} will increase, both contributing to a larger g_m in transistor M_P and M_N, reducing the dependence of $G_{m,eq}$ on temperature.

B. Amplitude Regulator

Fig. 4 (a) depicts the circuit diagram of the amplitude regulator. This nonlinear regulator is based on an RC filter composed of the pseudo-resistor R_p and capacitor C_1, similar to the design presented in [11]. When the amplitude of V_{OUT} is zero, the circuit is designed such that the drain current of M_4 is greater than M_2. This imbalance ensures that the dc value of V_{CTRL} across C_L remains zero, which will generate the maximum $G_{m,eq}$ from the g_m-cell for start-up. As the amplitude sensed by the RC filter increases, V_{CTRL} begins to increase to keep the drain current of M_4 constant. This will keep the $G_{m,eq}$ just enough for oscillation through a negative feedback loop, avoiding excess power consumption.

C. PTAT Current Source

The ULP PTAT current source used in this design is based on [3], which provides current bias to the amplitude regulator, as shown in Fig. 4 (b). The capacitor C_s and two switches constitute a switched-capacitor resistor. Driven by the 32 kHz XO output, it generates the required current at a nominal value of 20 pA (simulated). The PTAT current can be expressed as:

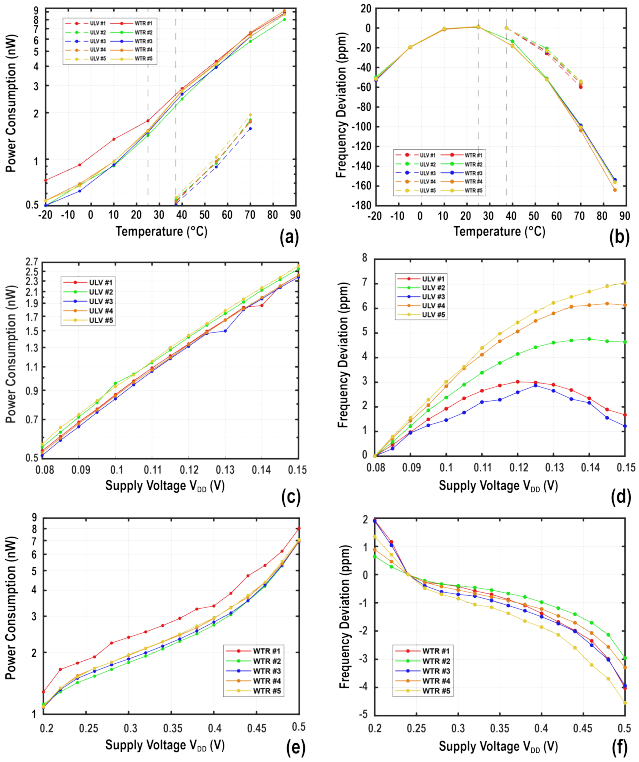

Fig. 5. (a)-(b) Measured results of the two modes across different temperatures (ULV mode: V_{DD}=80 mV, WTR mode:V_{DD}=240 mV). (c)-(d) Measured results of the ULV mode across different supply voltages (@37℃). (e)-(f) Measured results of the WTR mode across different supply voltages (@25℃).

$$I_{PTAT} = \ln(M) \cdot f_{OSC} C_S \cdot \frac{nk_B T}{q} \quad (2)$$

The generated current can compensate for the temperature dependence of transistors' transconductance when operating in the deep sub-threshold region.

IV. Measurement Results

The proposed 32 kHz XO is fabricated in 180 nm CMOS technology. The chip photo is shown in Fig. 6 (a), where the 4T-2C positive feedback gm-cell occupies an area of 0.011 mm2 and the total area including the regulator and PTAT current source is 0.038 mm2. An extra on-chip driver and a PMOS source follower were included for testing purposes.

The measurement data was collected from 5 samples for performance evaluation. The crystal ECS-2X6-FLX (nominal 6 pF) is used for testing with no extra on-board load capacitance. In ULV mode, measurement shows all 5 samples can operate at 80 mV within a temperature range of 37 °C to 70 °C, with an average power consumption of 0.54 nW (worst-case: 0.57 nW), an output frequency of 32773.8 ± 0.2 Hz, and an average line sensitivity of 59.3 ppm/V for VDD in between 0.08 V and 0.15 V (37 °C). In the WTR mode, all 5 measured samples can operate at 240 mV within a temperature range of -20 °C to 85 °C, with an average power consumption of 1.55 nW (worst-case: 1.77 nW), an output frequency is 32774.6 ± 0.6Hz, and an

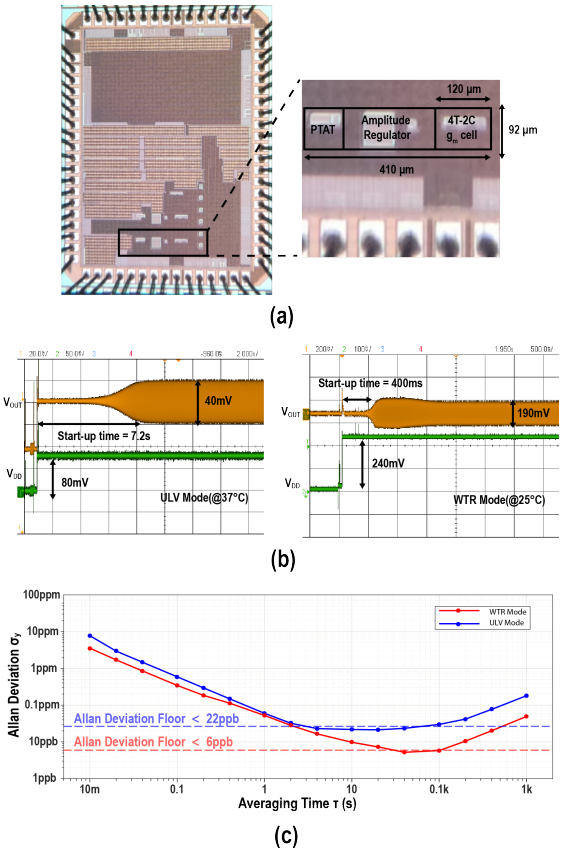

Fig. 6. (a) Die photo. (b) Start-up time. (c) Allan deviation.

average line sensitivity of 19.8 ppm/V sweeping V_{DD} from 0.2 V to 0.5 V. The WTR mode demonstrates an average of 150 ppm frequency deviation within its temperature range, which is primarily dominated by the crystal's intrinsic properties. Fig. 5 (a)-(f) presents the power and frequency deviation details of these two modes across different temperatures and supply voltages. Fig. 6 (b) shows the transient waveform during start-up, demonstrating a 7.2 s start-up time under the ULV mode, and a 0.4 s start-up time under the WTR mode. Fig. 6 (c) shows the Allan deviation floor: 22 ppb and 6 ppb respectively for the two modes, showing its long-term stability. The performance of this work is summarized in Table I, comparing it with the state-of-the-art ULP XOs. This work achieves the lowest power consumption among those that can operate down to 80 mV of supply voltage thanks to the proposed capacitively-coupled positive feedback g_m-cell.

V. Conclusion

This paper presents a ULP and ULV 32 kHz XO that operates at nano-Watts of power consumption at a power supply voltage down to 80 mV. It also shows state-of-the-art performance, satisfying the requirements for wake-up timers in IoT sensors. Its ability to operate under ULV allows it to further simplify system-level requirements during the idle mode, making it a promising candidate for RTC solutions in emerging energy-harvesting IoT systems.

TABLE I. Comparison With State-of-the-Art Works

	[2]	[3]	[4]	[5]	[6]	This work	
						ULV	WTR
Tech. (nm)	130	65	22	28	180	180	
Supply voltage (V)	0.06	0.5	0.46	0.38	0.9	**0.08**	**0.24**
Area (µm²)	3300	27000	29000	820	47000	11040	37720
Temperature Range (°C)	25/62	-20/80	-20/80	-20/85	-25/85	37/70	-20/85
Power @25°C (nW)	2.26	0.55	0.95	0.36	0.36	**0.54**[a]	1.55
Line Sensitivity (ppm/V)	8.4	13	22	16	60[b]	59.3[a]	19.8
Temperature Stability (ppm)	62	80	139	144	152	58	159
Allan Deviation Floor (ppb)	30	14	6	7	7	22[a]	6
Samples Reported	N/A	20	5	10	1	5	

[a.] Data measured at 37 °C

[b.] From Figure 4.4.4 in [6]

Ackowlegement

This work was supported by the Hong Kong University of Science and Technology under Grant R9867.

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