A 6.5pJ/Step Highly Linear Readout IC with Duty-Cycled Resistor and Switched Capacitor for Resistive and Capacitive Sensor Interface

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***Abstract*—This paper proposes a time-domain reconfigurable resistive and capacitive sensor interface for temperature and humidity sensing. A Wheatstone bridge combined duty-cycled resistor and switched capacitor is proposed, enabling pulse-width locked loop and frequency locked loop to perform high linear and energy-efficient R&C sensor readout. Fabricated in 65nm CMOS process, the chip achieves the highest reported linearity of R^2>0.99993 in state-of-the-art R&C sensor interfaces, along with a wide R&C sensing range for multi-type sensing applications. In addition, the system consumes 5.7-6.2μW power with extremely low FoM of 0.75-6.5pJ/step and compact area of 0.022mm^2.**

***Index Terms*—Reconfigurable sensor interface, time-domain readout, ultra-low power, high linearity**

I. Introduction

Sensor readout ICs for internet-of-things (IoT) systems use resistive or capacitive transducers to sense temperature, humidity, pressure, proximity and so on. Conventionally, a dedicated capacitance-to-digital converter (CDC) [1] and resistance-to-digital converter (RDC) [2] is used for specific resistive or capacitive transducers. To combine resistance and capacitance sensing, reconfigurable R&C-to-digital-converters (RCDC) that multiplex R&C sensors with a shared front end to save chip area have been proposed [3–7]. However, these RCDCs still fall short of achieving the linearity and energy efficiency of standalone RDCs or CDCs (Fig. 13).

The Wheatstone bridge (WhB) is a widely used architecture for high resolution and linear R/C sensor readout [8]. As shown in Fig. 1(a) on the left, conventional WhB sensor interfaces operate in the voltage domain and require high-performance instrumentation amplifiers (IA) and analog-to-digital converters (ADC), but their performance is often limited by IA noise and energy efficiency [9]. Besides, the WhB is power hungry with I_{WhB}=V_{DD}/R_{sen} which is unsuitable for normal commercial resistive sensor (<100kΩ). Moreover, the open loop structure has poor linearity across PVT variation. Recently, closed-loop time-domain WhB sensor interfaces have gained significant attention for simplifying IA design and achieving high linearity [5] [10] [11]. Prior design in Fig. 1(a) right uses a large R_{sen} (330kΩ) to reduce WhB current. Additionally, a MHz-range ring voltage-controlled oscillators (VCO) is used which is excessive for low system bandwidth (<10kHz) [5] [10], leading to unnecessary power consumption. To digitize the time domain signal, oversampling

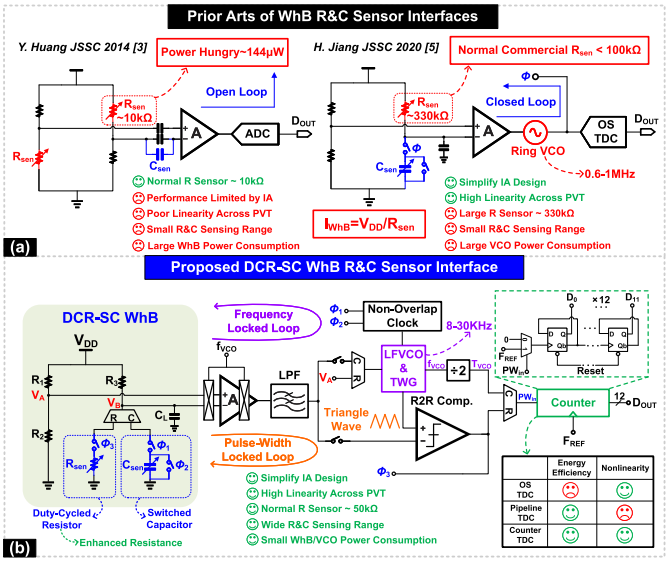

Fig. 1: (a) Prior art WhB based R&C sensor interfaces and (b) proposed DCR-SC WhB R&C sensor interface.

time-to-digital converter (OS TDC) [5] [10] and pipeline TDC [11] are used, but they reduce energy efficiency or introduce nonlinearity. Furthermore, prior WhB based R&C sensor interfaces have small R&C sensing range, which does not accommodate multi-type sensing applications.

We propose a R&C WhB sensor interface combining a frequency locked-loop (FLL) and a pulse-width locked-loop (PWLL), as illustrated in Fig. 1(b). This system consists of a WhB, a chopper-stabilized error amplifier (AMP), a lowpass filter (LPF), a low frequency VCO (LFVCO) with triangle-wave generator (TWG), a rail-to-rail comparator (R2R Comp.) and a counter-based TDC. The following are the key contributions and advantages of the proposed architecture:

- Combined duty-cycled resistor (DCR) and switched capacitor (SC) in WhB, incorporating an FLL and a PWLL to achieve high linearity, resolution and energy efficiency;
- An LFVCO is used instead of a ring VCO, significantly reducing power consumption, improving loop stability, and providing digital compatibility with the counter;
- A pulse-width readout counter running at the Nyquist rate is designed to further enhance energy efficiency without adding nonlinearity to the system.

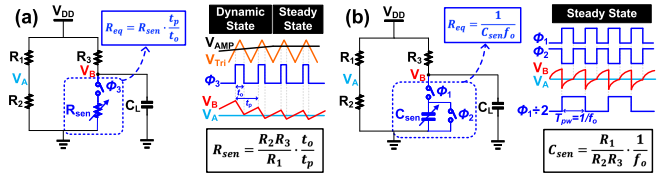

Fig. 2: Operating principle and waveforms of (a) DCR and (b) SC based WhB.

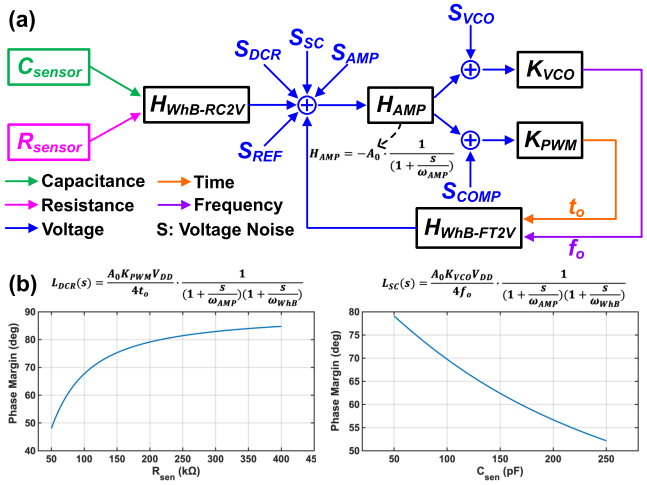

Fig. 3: (a) Small-signal block diagram of FLL and PWLL and (b) Simulated phase margin.

- Rail-to-rail operation is implemented in all key blocks to enable a wide R&C sensing range, allowing for the support of a broader variety of commercial sensors.

The rest of this paper is organized as follows: Section II presents the system dynamic analysis of the proposed R&C sensor interface. Circuit implementation of key blocks is detailed in Section III. Measurement results are presented in Section IV. Finally, conclusions are drawn in Section V.

II. System Dynamic Analysis

Fig. 2 illustrates the operating principle and waveforms of the DCR-SC WhB. R_1, R_2, and R_3 are set to 500kΩ which sets VA to $V_{DD}/2$. An external 1.5nF capacitor (C_L) is used to determine the average error voltage at V_B. When the feedback loop is balanced, V_B equals V_A. The equivalent resistance (R_{eq}) of the DCR and the SC is determined by the output pulse width (t_o) or frequency (f_o), which is locked by the PWLL or FLL. Using the balanced condition and R_{eq}, R_{sen} and C_{sen} can be calculated. The results show that R_{sen} and C_{sen} are linearly proportional to t_o or f_o. A frequency divider converts the period into a pulse-width signal, allowing the same type of counter to be used for digitizing both outputs.

Fig. 3(a) shows the small-signal block diagram of the system which has two poles. We choose the AMP pole to be the dominant pole and WhB pole to be the second pole. K_{VCO} is the VCO gain in Hz/V, while K_{PWM} is the pulse-width modulation (PWM) gain in s/V which is a constant value. Given the feedback nature of the system, stability and phase margin becomes a critical consideration. Once the loop is balanced, we simulated the loop gain and pole based on R or C

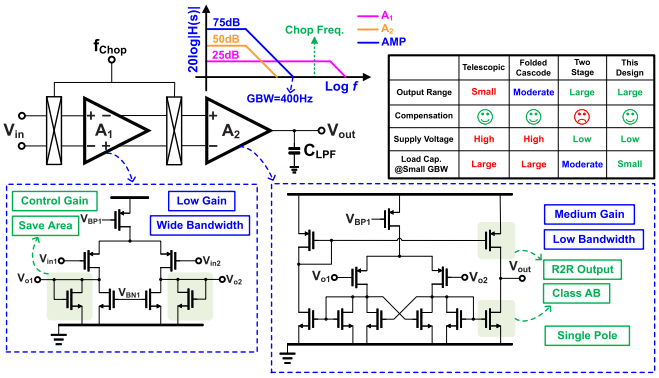

Fig. 4: Schematic and design considerations of the chopper-stabilized error amplifier.

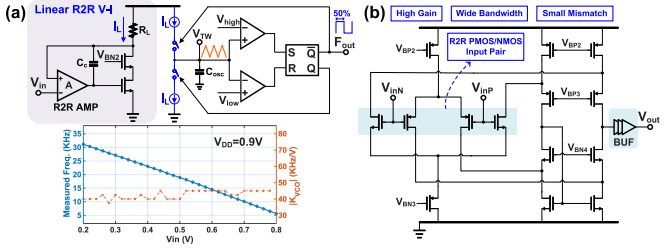

Fig. 5: (a) VCO&TWG with measured frequency tuning range and (b) R2R comparator.

input. Using a behavioral model for the loop we calculated the phase margin versus the input value of R&C sensor with the aim of keeping the minimum phase margin above 45 degrees in the target sensing range, as shown in Fig. 3(b). Phase margin and sensing range can be adjusted by changing the WhB resistors (R_1, R_2, R_3) and poles in the design stage.

III. Circuit Implementation

A. Chopper-Stabilized Error Amplifier

Fig. 4 depicts the chopper stabilized error amplifier that serves as the loop filter, providing high DC gain for system linearity and rail-to-rail output to support a wide sensing range. Standard telescopic and folded-cascode topologies are unsuitable due to an insufficient output range. The standard cascode design also demands more complex bias circuits, leading to higher power consumption. The traditional 2-stage design is similarly unsuitable, as the second pole's position heavily depends on the transconductance of the second stage, requiring significantly more power for stability. Additionally, achieving very low bandwidth with this design would require a large Miller capacitor and low second-stage transconductance, which would introduce a low-frequency right half-plane zero that cannot be easily eliminated. We propose a two-stage design with independent stages: the first stage is optimized for low noise and consumes most of the power; the second stage operates at low power (100nA) and enables dominant pole compensation, achieving a 400Hz gain-bandwidth product. The second stage also features a class AB output, which enhances large-signal response and reduces settling time. The system's step response has a settling time of 1-2ms.

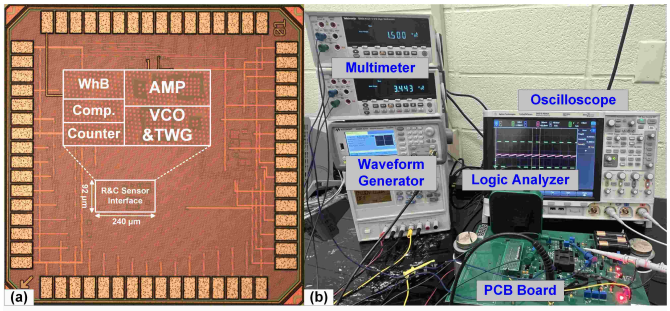

Fig. 6: (a) Chip micrograph and (b) measurement setup.

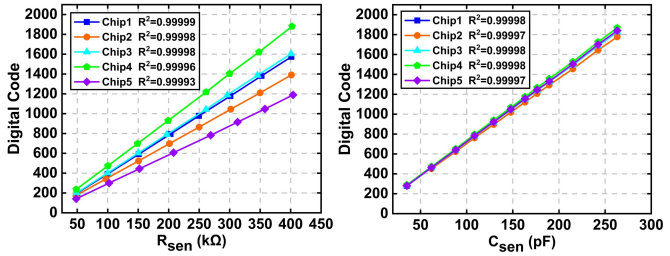

Fig. 7: Measured digital output and R^2 linearity versus R_{sen} and C_{sen} input across five chips.

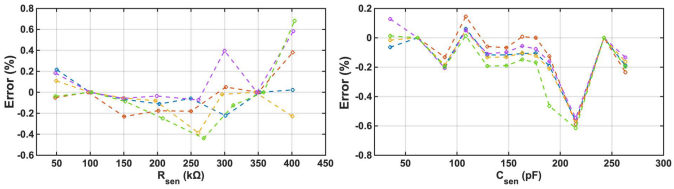

Fig. 8: Read-out error after applying two-point calibration.

B. LFVCO and R2R Comparator

The VCO and TWG are implemented with a relaxation-based structure shown in Fig. 5(a). The first component is a linear R2R voltage-to-current converter that generates an output current with a wide input range and high linearity. To minimize the loading effect on the AMP and prevent gate leakage, thick-oxide transistors are used in the input pairs of the R2R amplifier. A Miller compensation capacitor is also added between the R2R amplifier's output and R_L to stabilize the feedback. The second component consists of two cascode current mirrors that replicate I_L (20-950nA) to charge the capacitor C_{OSC}. V_{high} ($3V_{DD}/4$) and V_{low} ($V_{DD}/4$) are generated through a diode-connected PMOS voltage divider, providing a low-quiescent-current reference with minimal area overhead. The measured linearity of K_{VCO} (40-45kHz/V) makes the loop gain more stable which is beneficial for loop stability analysis. Additionally, the low-frequency output characteristic makes this system well-suited for counter with large time resolution (20-100ns), enabling lower power consumption. Fig. 5(b) shows the schematic of R2R comparator which uses a PMOS/NMOS differential input pair to achieve R2R input capability. The comparator is designed with high gain, wide bandwidth and small mismatch to perform the PWM. An output buffer is implemented to drive the load while maintaining signal integrity and minimizing distortion.

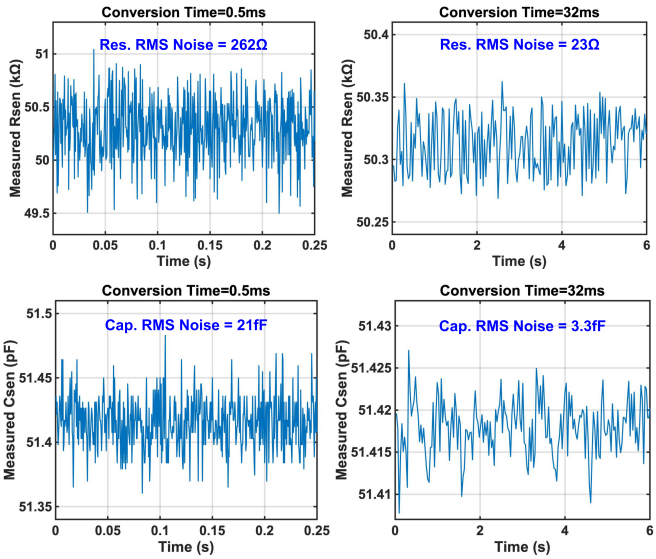

Fig. 9: RMS noise of the R&C sensors measurements.

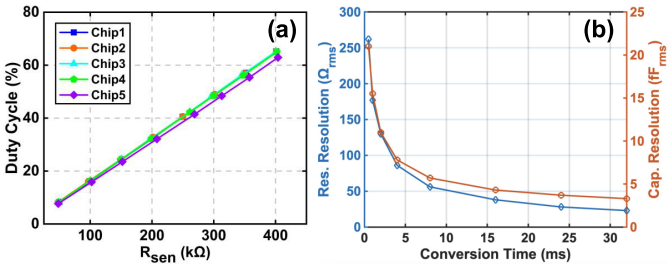

Fig. 10: Measurement results of (a) duty-cycle ratio versus R_{sen} and (b) R&C sensing resolution versus conversion time.

IV. Measurement Results

The proposed R&C sensor interface was fabricated in 65nm CMOS process with an active area of $0.022mm^2$ [Fig.6(a)]. Fig. 7 shows the relationship between the input R&C sensor values and the digital output codes across five chips. Both R_{sen} and C_{sen} demonstrate excellent linearity, with R^2>0.99993 for R_{sen} and R^2>0.99997 for C_{sen}. For capacitance measurements, we implemented a capacitive DAC on the PCB with a range of 3.3pF to 250pF and an LSB of 3.3pF. The actual capacitance value of each bit (including switches) was measured using an LCR Meter (0.1 pF accuracy). For resistance measurements, we used a 500kΩ variable resistor and measured the resistance values with a TektronixDMM4020 (5Ω accuracy). The digital output for R_{sen} shows a gain error primarily due to variations in the VCO&TWG center frequency, caused by variation in R_L and C_{OSC}. However, the duty-cycle ratio of R_{sen} remains stable across chips [Fig. 10(a)]. The gain error can be calibrated by using two-point calibration. Fig. 8 presents the readout error after two-point calibration, the peak-to-peak error for R&C sensor is about 1% and 0.8%, respectively. Fig. 9 illustrates the RMS noise measurements, with the digital output averaged over 0.5ms and 32ms. Fig. 10(b) shows the measured resolution versus conversion time. Fig. 11 presents the measurements of using TI TMP63-Q1 temperature sensor and IST P14-W humidity sensor. Compared to the sensor model, the average

TABLE I: Comparison with State-of-the-Art R&C Sensor Interfaces

	This Work		JSSC 2014 [3]	ISSCC 2020 [4]	JSSC 2020 [5]	TCAS-I 2022 [6]	CICC 2023 [7]
Sensor Type	R&C		R&C&V&I	R&C	R&C	R&C	R&C
Application	Temp./RH		Prot./Gluc.	Temp./Prox.	Temp./RH	Temp./RH	Temp./Prox.
Process (nm)	65		350	130	180	180	65
Active Area (mm^2)	0.022		11.25	0.04[a]	0.72	0.175	0.038[a]
Supply Voltage (V)	AVDD: 0.9 DVDD: 0.8		1.8	1.2	1.5-2	1	1.2
ADC Type	Counter		SAR ADC	Counter	OS TDC	Counter	ΔΣ ADC
Conv. Time (ms)	0.5	32	5[b]	32[c]	1	2.93	37.5
Res. Meas. Range	50-400kΩ		*9.8-10.5kΩ*[b]	20-249kΩ	260-380kΩ	10MΩ	22-910kΩ
Res. Meas. Resolution	262Ω	23Ω	*0.13Ω*[b]	32.5Ω	N/A	0.37Ω -0.66Ω	286Ω
Res. ENOB[d]	8.9	12.4	10.9	11.4	8.22[c]	*15.3*[b]	10.13
Cap. Meas. Range	35-260pF		6-10.5pF	0-100pF	*3.5-4pF*[b]	46nF	36-1000pF
Cap. Meas. Resolution	21fF	3.3fF	*0.23fF*[b]	13.75fF	N/A	0.11fF -0.22fF	162fF
Cap. ENOB[d]	11.9	14.6	12.8	11.3	8.22[c]	*15.7*[b]	10.5
Linearity (R^2)	0.99993		0.996	*<0.999*[b]	N/A	0.9991[f]	0.998
Power (μW)	R Mode: 6.2 C Mode: 5.7		*R: 172*[b] *C: 28.4*[b]	2.2[g]	15.6	140	0.74[g]
FoM (pJ/step)[e]	R Mode: 6.5[h] C Mode: 0.75[h]		R: 450 C: 19.9	27.8	52.3	R: 10.2 C: 7.7	R: 24.8 C: 19.1

(a) Total area/# of Channel (b) Calculated from paper data (c) Data calculated from paper [7]
(d) R(C) ENOB=$\log_2$(R(C) Range/$2\sqrt{2}$·Resolution) (e) FoM=Power×Conv. Time/2^{ENOB}
(f) Capacitance-to-time conversion (g) Total power/# of channel (h) For a conversion time of 0.5ms

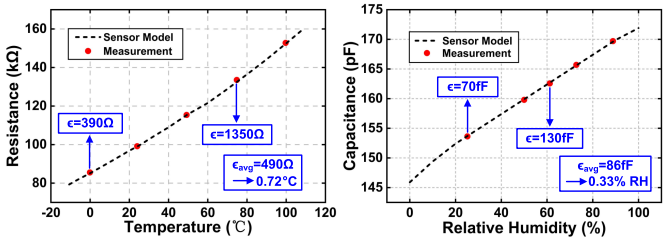

Fig. 11: Temperature and rel. humidity measurements.

error for R&C corresponding to temperature and relative humidity (RH) deviations of 0.72°C and 0.33% RH.

Table I summarizes the performance of the proposed R&C sensor interface and compares it with state-of-the-art works. This work supports a wide R&C input range, achieving 12.4 and 14.6 ENOB with 32ms conversion time, demonstrates the highest linearity with R^2>0.99993. It operates with only 5.7-6.2μW of power, achieving an FoM of 6.5pJ/step in R-mode and 0.75pJ/step in C-mode.

V. Conclusion

This work presents a time-domain RCDC for temperature and humidity sensing. An FLL and a PWLL are employed in a DCR-SC WhB to enable highly linear and energy-efficient R&C sensor readout. The system incorporates an error amplifier, an LFVCO, and a pulse-width readout counter, each specifically designed to enhance various performance of the RCDC. Rail-to-rail operation is implemented in all key blocks to extend R&C sensing range to accommodate multi-type commercial sensors. As shown in Fig. 13, the prototype chip fabricated in 65nm CMOS process demonstrates significant improvements in linearity and energy efficiency over previous RCDC designs, making it a promising candidate for next-generation multi-type wearable sensing applications.

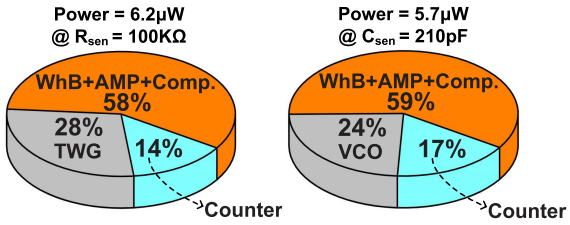

Fig. 12: Breakdown of the measured power consumption.

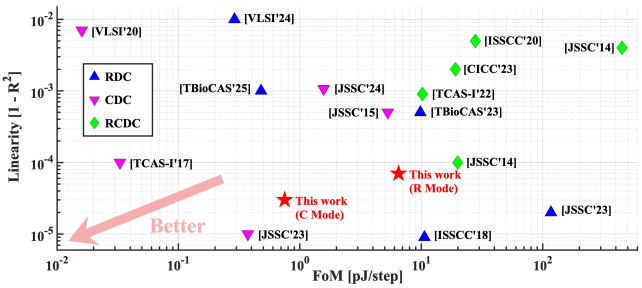

Fig. 13: Survey of state-of-the-art RDCs, CDCs and RCDCs.

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