A ±1V DC-Coupled 20-GHz Bandwidth Front-End Chipset with 1.14Vpp Output for High-Speed Digital Real-Time Oscilloscopes in SiGe BiCMOS

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Abstract—**This paper presents a DC-coupled 20-GHz RF/Analog front-end chipset for high-speed real-time oscilloscopes (RTO). The chipset consists of a DC-cancelling amplifier (DCCA), a zero-volt coupled symmetric distributed active balun (SDAB), and a dual differential-output variable gain amplifier (DDO-VGA). Prototyped in a 0.18-μm SiGe BiCMOS, the work achieves –1-to-1 V input DC range, <0.46-dB/V gain variation, zero-volt interstage adjustment, DC-to-20 GHz bandwidth, 5.5-to-7.7 dB noise figure (NF), 25.7-to-33.7 dB maximum gain, 20.5 dB gain variable range, ≥1.14Vpp maximum differential output, 0-to-0.7 V tunable output DC bias for ADCs, and an additional output for triggering.**

Keywords—real-time oscilloscopes, front-end, DC coupling

I. INTRODUCTION

High-speed digital oscilloscope is vital for testing of high-speed digital and communication systems, which can be classified into equivalent time sampling oscilloscope (SO) and real-time oscilloscope (RTO). Compared to SO, RTO can capture a non-repetitive signal or trigger off the data signal itself, making it much more suitable for debugging the signal behavior. In addition, RTO can provide extensive support for decoding as well as testing of protocols and standards.

RF/analog front-end designs are pivotal for RTOs' performance, and their architecture can be classified into digital bandwidth interleaving (DBI) and direct sampling (DS), as shown in Fig. 1. Leveraging on multiple sub-band divisions, DBI alleviates broad band requirement of front-end circuits and ultra-high sampling rates of ADCs. Nevertheless, the subsequent waveform reconstruction of DBI consumes massive resources, and the degradation of signal integrity is always inevitable [1]-[3] (LeCroy). DS distinguishes itself by real-time performance and simplicity in digital processing.

In literatures, several remarkable front-ends can be found that reveal DS RTO designs [4]-[6]. In [4] (ZMD) and [5] (Yokogawa), operational transconductance amplifiers (OTAs) are proposed as the first stage to cancel input DC and amplify AC weights. Since operational frequencies of OTAs are theoretically limited, such topology demonstrates well in below GHz frequency ranges. Notable work in [6] (Agilent) reports a high-speed DS RTO architecture. Instead of OTA, it utilizes a broadband differential amplifier (DA) at the first stage to cancel DC weight and amplify AC/RF parts, promoting the operation frequencies to GHz. Here, one input of DA is used as signal testing input, and the other is for
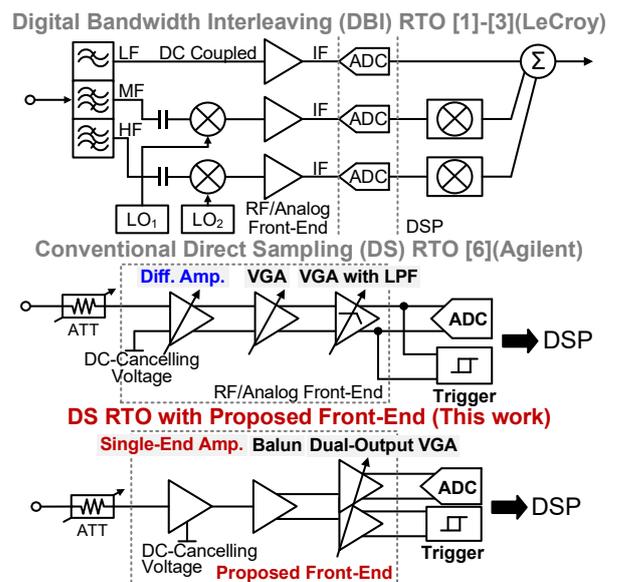

Fig. 1. Structures of the DBI, the conventional DS RTO and the DS RTO with the proposed front-end.

feeding of DC cancellation voltage. The first stage of DA functions as Balun for the signal to be tested, thereby, leading to fine compatibility with high-speed ADCs which typically have differential inputs. However, compared to conventional low-noise RF amplifiers, such a configuration of DA presents a doubled noise figure. Moreover, feeding DC cancellation voltage through one of the inputs reduces the swing range of the signal to be tested. In other words, trade-offs exist in-between input 1 dB compression point (IP1dB) and DC weight, leading to failure in sampling of signals with small AC swings and large DC bias. Although several RTO products have been proven successful in the market, other design essentials of the RF/analog front end are hardly found in the literatures.

In this paper, a DC-coupled 20-GHz RF/Analog front-end chipset for high-speed DS RTO is proposed, as shown in Fig. 2. Different to wideband RF and optical designs, the proposed work features the following functions. 1) The DC-cancelling amplifier (DCCA) is able to cancel an input DC weight of ±1 V, thus it enhances the AC sampling with larger DC weights as compared to ±400 mV DC cancellation of [6]. 2) As the first stage, DCCA can achieve lower noise figure (NF) compared to the SE-to-differential conversion using a differential amplifier in [6], thanks to its SE low-noise amplification structure. The single-to-differential conversion is achieved by symmetric distributed active balun (SDAB) in
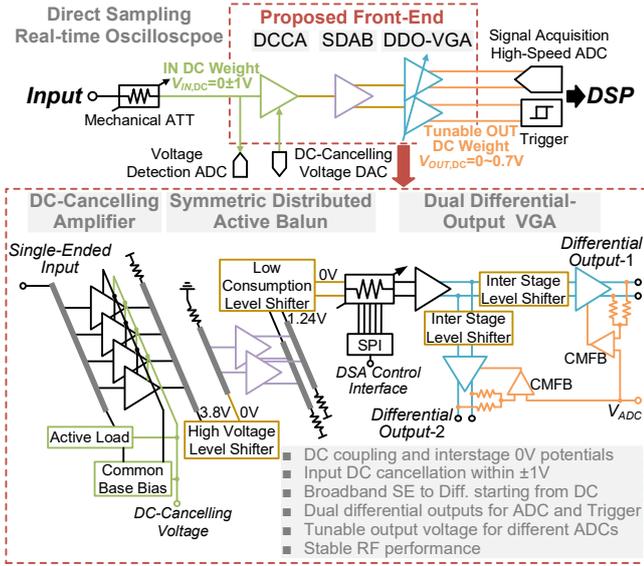
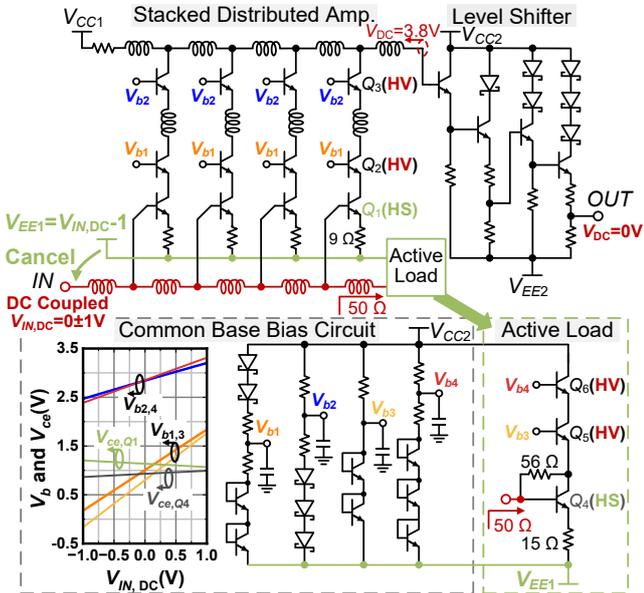Fig. 2. Structures of the proposed RTO and front-end.

Fig. 3. Schematic of the DC-cancelling amplifier (DCCA), and simulations of node voltages versus cancelling voltage.

the second stage. 3) All circuits are DC-coupled, and the inter-stage DC points are aligned to 0 V. Therefore, correct amplifications of ultra-low frequency components can be attained. 4) Performances of the chipset have little sensitivity to varying input DC weights, presenting <0.46-dB/V gain change, negligible NF, and consistent linearity. This eases digital processing within RTO. 5) An additional output enables the trigger function in the analog domain, leading to rapid response of the oscilloscope. Both outputs are equipped with adjustable DC voltages from 0 to 0.7 V, in order to align with various input DC needs of ADCs. The proposed front-end chipset is prototyped in a 0.18-μm SiGe BiCMOS.

II. CIRCUIT DESIGN

A. The Proposed Front-End Architecture

Fig. 2 shows the proposed three-stage front-end architecture for DS RTO. The first stage is DCCA which is designed in an all-SE structure. Theoretically, it presents ~3-dB lower NF as compared to the SE-to-differential
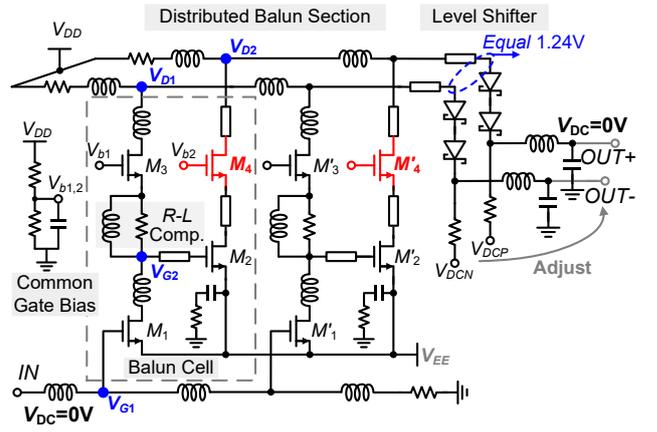

Fig. 4. Circuit schematic of the proposed symmetric distributed active balun (SDAB).
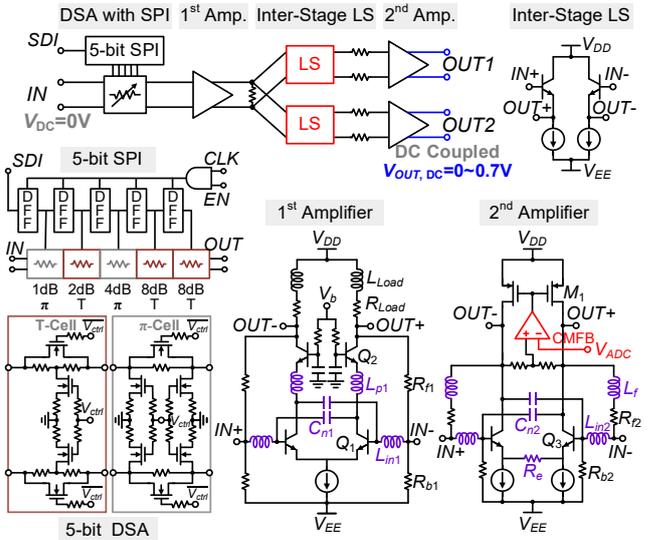

Fig. 5. Block diagram and schematic of the proposed dual differential-output variable gain amplifier (DDO-VGA).

conversion using a differential amplifier [6]. In the second stage, SDAB is responsible for broadband SE-to-differential conversion, thanks to its distributed structure. Dual differential-output variable gain amplifier (DDO-VGA) at the last provides sufficient dynamic range to both sampling ADC and triggering port.

B. DC-Cancelling Amplifier

Fig. 3 shows the proposed DCCA with a 4-stage stacked distributed structure. An active load in the gate line enhances low-frequency noise performance. HBT transistors are used to minimize the noise. The DC cancellation is achieved by a voltage node of V_{EE1} (–2-to-0 V) that dynamically adjusts in proportion to the input DC weight ($V_{IN, DC}$, –1-to-1 V). The common base (CB) stage uses a stacked structure with high-voltage (HV) transistors to tolerate large inner voltage variations caused by input DC changes. Voltage division circuits are designed for bias voltages of the CB stage (V_{b1}-V_{b4}). V_{b1}-V_{b4} track the $V_{IN, DC}$ variation, effectively stabilizing the collector-emitter voltages (V_{ce}) of the high-speed (HS) transistors (see simulations in Fig. 3). Thereby, optimal operations of the common-emitter stage and active load can be ensured. Besides NF, the SE structure avoids differential DC offset issue in [6]. A hybrid of transistors and diodes forms a four-stage level shifter. This level shifter shifts the
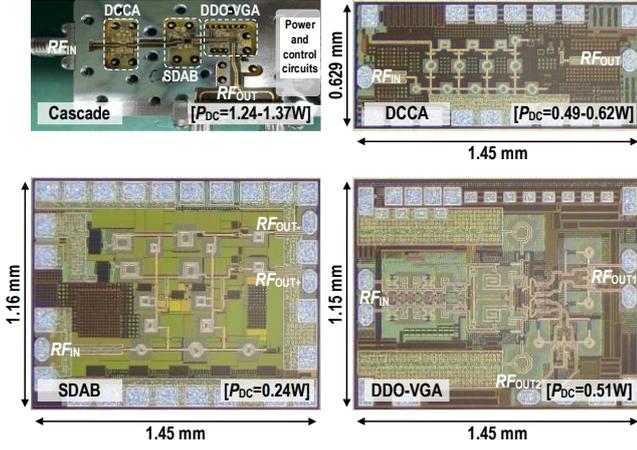
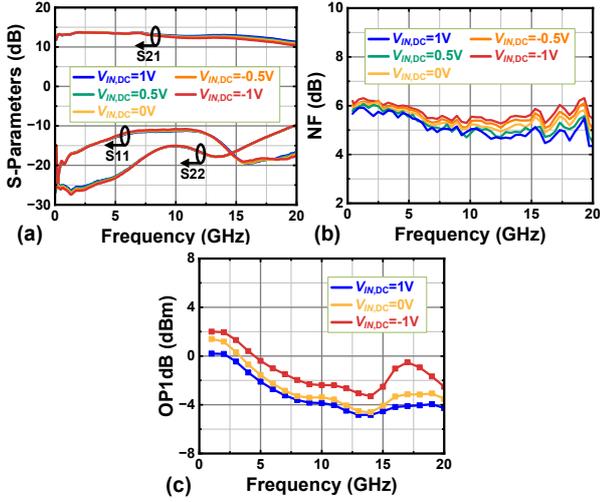Fig. 6. Micrograph of prototyped chipset, and cascade assembly fixture.

Fig. 7. Measurement results of the proposed DCCA versus different input DC weight. (a) S-parameters, (b) NF, and (c) OP1dB.
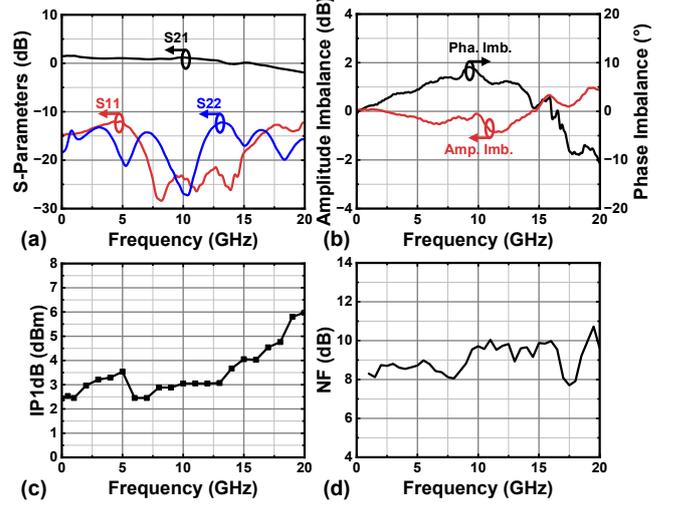

Fig. 8. Measurement results of the proposed SDAB, (a) S-parameters, (b) Imbalance, (c) IP1dB, and (d) NF.
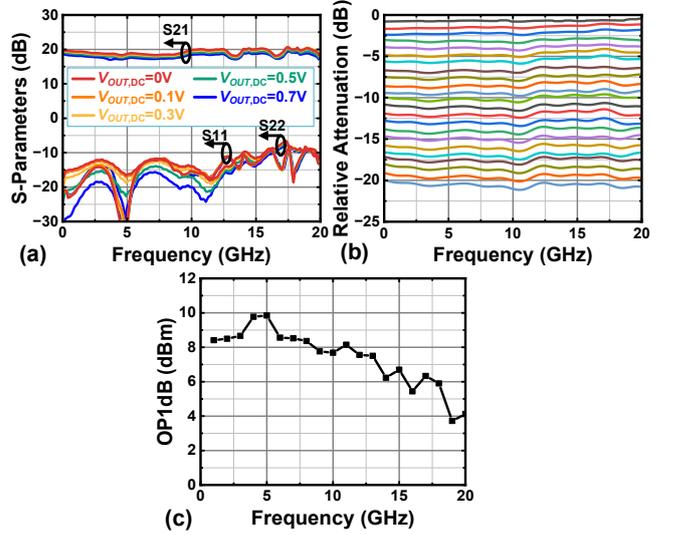

Fig. 9. Measurement results of the proposed DDO-VGA, (a) S-parameters versus different output DC weight, (b) Relative attenuation, and (c) OP1dB at $V_{OUT, DC}$=0V.

output DC voltage from 3.8 V to 0 V to match the input level of the SDAB. The low insertion loss and good RF performance are maintained simultaneously.

C. Symmetric Distributed Active Balun

In Fig. 4, the SDAB also adopts a distributed structure. NMOS transistors are used to attain a better IP1dB. Different from reported distributed baluns, a common-gate transistor M_4 and M_4' are inserted into the in-phase paths. Transistors in the in-phase and out-of-phase branches are identical, so are V_{G1} and V_{G2}. The output DC voltages of V_{D1} and V_{D2} are equal. Thanks to the insertion of M_4 and M_4', the output impedance of the cascode pair is similar. This facilitates the maintenance of output balance and output matching by simply using identical matching circuits. Parallel R-L networks are used to extend the bandwidth. For DC coupling, a pair of level shifters is constructed using diode-resistor divider structures. These shifters shift V_{D1} and V_{D2} down to zero, while providing 50 Ω SE and 100 Ω differential output impedance. Here, tail nodes V_{DCN} and V_{DCP} are left open to compensate for process variations.

D. Dual Differential-Output Variable Gain Amplifier

In the DDO-VGA design shown in Fig. 5, a pair of 5-bit digital step attenuators (DSAs) is followed by two stages of amplifiers. This structure presents favorable NF for weak

input signals, while good linearity for large input. The DSAs use a hybrid T-type/π-type cascaded structure for broadband, 20.5-dB gain variation, and low insertion loss. The first amplifier employs a cascode structure with peaking inductor L_{p1}, providing high gain and low noise. The second amplification stage provides two identical differential outputs for sampling and trigger. In front of the 2nd amplification stage, a pair of emitter followers is used for level shifting, which also enhances the isolation in-between sampling and trigger outputs. An adjustable output DC voltage (0-to-0.7 V) to ADC and the trigger are directly ensured by the common-mode feedback (CMFB) circuit at the second amplifier. Emitter degeneration resistors R_e are used to improve linearity. A peaking inductive feedback L_f assists on flatten the in-band gain. Both amplifiers use input-peaking inductors L_{in1} and L_{in2} and neutralizing capacitors C_{n1} and C_{n2} to improve high-frequency performance and extend bandwidth.

III. MEASUREMENT RESULTS

The proposed chipset is prototyped in a 0.18-μm SiGe BiCMOS process. The total consumption is 1.24-1.37 W. Fig.

Reference		This work	[1] 07'IMS (LeCroy)	[2] 10'OFC (LeCroy)	[3] 14'BCTM (LeCroy)	[6] 10'CSICS (Agilent)
Technology		Direct Sample	DBI	DBI	DBI	Direct Sample
Topology		DCCA, SDAB, DDO-VGA	Multiplexer, Convertor	Multiplexer, Convertor	Multiplexer, Convertor	3×Diff VGAs, 2×LPFs
Functions	SE IN	Yes	-	-	-	Yes
	Diff. OUT	Yes	-	-	-	Yes
	Additional OUT to trigger	Yes	-	-	-	Yes
Frequency Bandwidth		20GHz	[3]6GHz, [4]18GHz	[3]16GHz, [4]30GHz	[3]36GH, [4]100GHz	32GHz, 16GHz
Max. Gain		25.7-33.7dB	[5]14dB	[5]14dB	[5]14dB	18dB
Gain Variable Range		20.5dB	[5]40dB	[5]34dB	[5]18dB	15dB
NF		5.5-7.7dB	-	-	8-18dB	-
IN DC OC Range		±1V	-	-	-	±400mV
Gain Sensitivity to $V_{IN,DC}$ across whole Bandwidth		<0.46dB/V	-	-	-	-
OUT DC Range		0-0.7V	-	-	-	-
Max. Output Amplitude		[1]1.14Vpp	[5]500mVpp	[5]500mVpp	[5]500mVpp	500mVpp
Process		0.18µm SiGe	-	-	-	Agilent InP
Power Consumption		[2]1.24-1.37W	-	-	-	1.7 W

[1] Calculated from OP1dB. [2] Varies with DC-cancellation voltage. [3] BW of DC-coupled channel. [4] BW of overall DBI. [5] Read from high-band channel block diagram in [1]-[3].
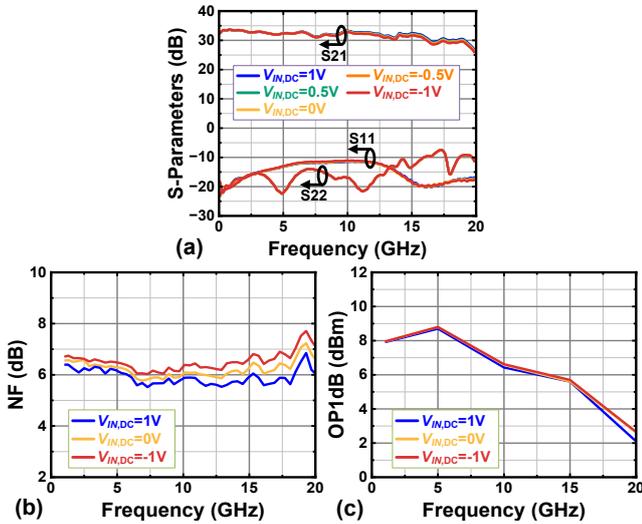SE: Single-Ended, Diff: Differential, OC: Offset Cancellation.

Fig. 10. Measured results of proposed chipset at the maximum gain versus different $V_{IN, DC}$ at $V_{OUT, DC}$=0V, (a) S-parameters, (b) NF, and (c) OP1dB.

6 shows microphotographs of dies and the testing fixture. The DCCA, SDAB and DDO-VGA occupy the chip area of 0.91 mm², 1.68 mm², and 1.67 mm², respectively with pad frame.

Fig. 7 measures the performance of DCCA versus different input DC weights. Consistent performances of 10.4-to-13.8 dB gain, 4.3-to-6.3 dB NF, >9.8 dB return loss and –4.8-to-2 dBm output 1dB compression point (OP1dB) are obtained with $V_{IN, DC}$ from –1 to 1 V. Fig. 8 shows measurements of SDAB. The gain measures –1.9 to 1.5 dB with good matching from DC to 20 GHz. The amplitude imbalance is less than ±1 dB and the phase imbalance is less than ±10°, which can be further rectified by DDO-VGA. The NF is 7.7-to-10.7 dB and the IP1dB is 2.4-to-6 dBm. Fig. 9 shows the DDO-VGA's measured results. The maximum gain is 16.9-to-20.6 dB, which is insensitive to $V_{OUT, DC}$ ranging from 0-to-0.7 V. The gain variable range is 20.5 dB with 24 attenuation states. The OP1dB is 3.7-to-9.8 dBm at maximum gain and $V_{OUT, DC}$=0 V.

The whole chipset is measured at an extreme condition of maximum gain and $V_{OUT, DC}$=0 V, as shown in Fig. 10. The proposed front-end chipset shows a 25.7-to-33.7 dB gain, and <0.46 dB/V gain variation over –1-to-1 V $V_{IN, DC}$ across DC-to-20 GHz. At 1-to-20 GHz RF band, it presents 5.5-to-7.7 dB NF and 2.1-to-8.8 dBm OP1dB (1.14-to-2.46Vpp) within –1-to-1 V $V_{IN, DC}$. Gigahertz RTO front-end designs that can be found in the literature are used for comparison, see Table I. This work introduces a different front-end structure, proposes several topologies for DS front-end circuits, presents all RTO circuit details that were not revealed by prior literatures, and demonstrates promising performance for RTO applications.

IV. CONCLUSION

In this paper, a novel front-end architecture for RTOs is proposed. Functions and designs are illustrated in detail. The design solutions for input DC offset cancellation, NF, gain sensitivity, SE-to-differential, output DC adjustment and trigger output are presented. The chipset is prototyped in a 0.18-μm SiGe process. The results demonstrate its potential for facilitating the digital processing capabilities of RTOs.

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