An Area-Efficient and Low-Power Switched Capacitor Integrator for Discrete-Time Delta Sigma Modulators

Hossein Esmailbeygi, Elham Hatamzadeh, and Farshad Moradi
Department of Electrical and Computer Engineering, Aarhus University, Aarhus, Denmark

***Abstract*—This paper presents a novel switched-capacitor integrator for discrete-time delta-sigma modulators (DT-DSM) that eliminates the trade-off between integrator voltage gain and noise performance. By splitting the sampling capacitor and introducing a discharging phase into the circuit, the proposed architecture significantly reduces the required total capacitance. In addition to area reduction, the integrator dramatically decreases the current drawn from the reference node in DSMs, leading to a reduction in overall power consumption. As a proof of concept, a third order DT-DSM was implemented by incorporating the proposed integrator in a 180nm CMOS technology, where the area required for implementing the first-stage capacitor array was reduced by 61.5% compared to a conventional integrator with the same performance. Measurement results show that the prototype achieves an SNR and SNDR of 104.9dB and 101.2dB, respectively, at fin = 66.185Hz.**

Keywords*—Switched Capacitor Integrator, Discrete-Time Delta Sigma Modulator (DT-DSM), Analog-to-Digital Converter (ADC).

I. Introduction

Switched-capacitor (SC) integrators play a key role in discrete-time delta-sigma modulators (DT-DSMs). Conventional SC integrators can be implemented using either a shared or dedicated capacitor for sampling and DAC conversion/subtraction, with each configuration having its advantages and disadvantages that affect the overall performance of the DT-DSM. As shown in Fig. 1, although employing separate capacitors provides high isolation between the input signal and the reference voltage (V_{REF}), the mismatch between the sampling and DAC capacitors (C_S and C_{DAC}) limits the gain error of the integrator. This mismatch can result in a gain accuracy of less than 0.1% for the overall DSM, which does not meet the requirements for some applications [1]. Moreover, to meet the thermal noise requirements of the DSM, the sampling capacitor typically has a capacitance in the range of a few picofarads (pF), making the implementation of two separate capacitors inefficient in terms of chip area. Although the gain error issue is solved in the shared capacitor configuration, this architecture suffers from the leakage path between the input signal and the reference voltage. This leads to degradation in the performance of the integrator unless a voltage buffer featuring low output impedance is employed, which comes at the cost of higher power consumption due to providing V_{REF} with sufficiently low impedance.

Another important parameter that affects DT-DSM performance is power consumption, which can be reduced by decreasing the output swing of the integrator. A reduced output swing not only enables the circuit to operate at a lower supply voltage but also decreases the energy required to charge and discharge the capacitors. To achieve a lower output swing in SC integrators, the gain must be reduced,

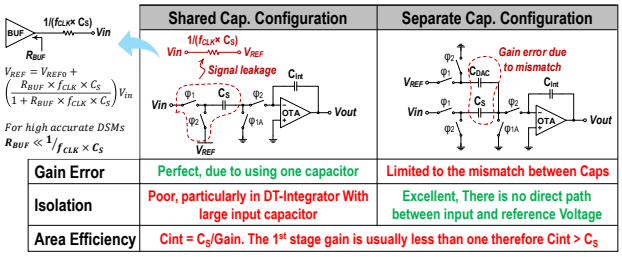


Fig. 1. Two conventional configurations for switched capacitor integrators and their pros and cons

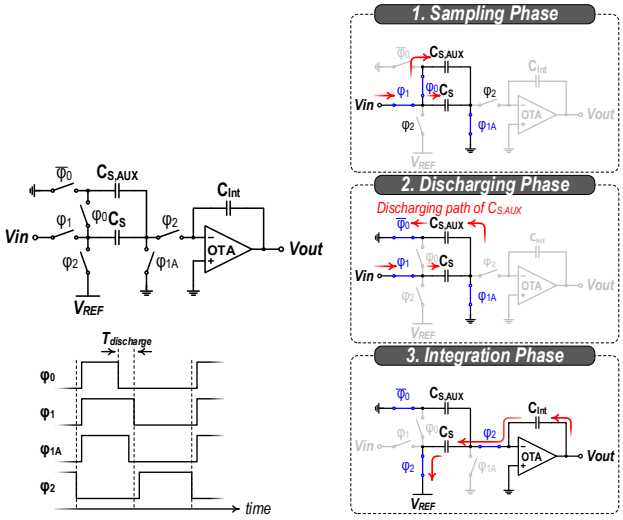


Fig. 2. a) Circuit diagram of the proposed integrator along with the required phases, and b) detailed operation of the proposed integrator in different phases

which is defined by the ratio of the sampling capacitor (C_S) to the integration capacitor (C_{Int}). Since the value of C_S is dictated by thermal noise requirements, achieving lower gain necessitates a larger C_{Int}, resulting in increased chip area. This highlights the trade-off in conventional SC integrators between gain, area, and noise performance.

To address this issue in SC integrators, this paper presents a new technique for sampling the input signal that maintains the same noise performance as conventional configurations while enabling the use of a smaller integration capacitor. This results in a significant reduction in the required area for the capacitor array by eliminating the gain-area-noise trade-off in SC integrators. In addition to chip area improvement, high-gain accuracy is ensured by employing a shared capacitor for both sampling and DAC functions, while the mentioned leakage path associated with shared-capacitor architectures is attenuated using the proposed sampling technique. To validate the functionality and reliability of the proposed integrator, a third-order DT-DSM was implemented using the

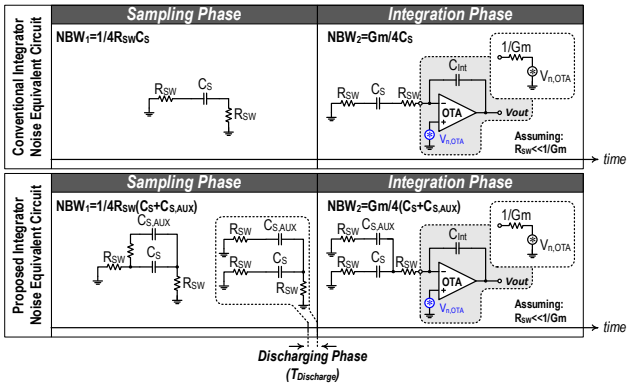


Fig. 3. NBW calculation in the proposed and conventional integrators

proposed circuit, resulting in a 61.5% reduction in the first-stage capacitor array area compared to conventional implementations. Measurement results demonstrate that the prototype achieves an SNR and SNDR of 104.9dB and 101.2dB, respectively.

II. Proposed Discrete Time Integrator

Fig. 2(a) illustrates the proposed integrator along with the required clock signals. In this architecture, the sampling capacitor is divided into two separate capacitors, C_S and $C_{S,AUX}$, with the total capacitance determined based on the required noise performance. As shown in Fig. 2(b), during the sampling phase, the input signal is sampled onto both capacitors, ensuring that the desired signal-to-noise ratio (SNR) is achieved by limiting the noise bandwidth (NBW) using the combination of C_S and $C_{S,AUX}$. To eliminate the contribution of $C_{S,AUX}$ in the integrator gain, while preserving its role in limiting NBW, this capacitor must be discharged slightly before the integration phase. To facilitate this, a new switching phase, referred to as the discharging phase, is introduced, which occurs slightly before the end of the sampling phase. During this phase, $C_{S,AUX}$ is detached from the input signal and discharged by connecting its bottom plate to the virtual ground. Consequently, only the charge captured on C_S is transferred to C_{Int} during the integration phase. As a result, the gain of the proposed integrator is derived as in (1):

$$\text{Voltage Gain} = C_S/C_{Int} \tag{1}$$

while $C_{S,AUX}$ solely contributes to limiting the NBW of the proposed integrator.

Based on the previous explanations, the proposed integrator allows the desired gain to be achieved using a significantly smaller C_{Int} since the noise performance is determined by the combined capacitance of C_S and $C_{S,AUX}$. In this design, the insufficient capacitance of C_S to meet the desired SNR requirements is compensated by the capacitance of $C_{S,AUX}$, resulting in an area-efficient integrator. Alternatively, a low-power design approach can be employed by utilizing the same C_{Int} as in conventional integrators while using a smaller C_S to decrease the integrator gain and, consequently, the integrator output swing, while the NBW is limited by $C_{S,AUX}$. This reduction in output swing enables the integrator to operate at a lower supply voltage, thereby decreasing the overall power consumption of the circuit.

A. Noise

To demonstrate that the proposed integrator does not introduce any noise penalty, its noise equivalent circuit in each phase is depicted in Fig. 3, alongside the noise equivalent circuit for a conventional SC integrator [2]. As illustrated, the NBW of the proposed integrator is similar to that of the conventional configuration and is determined by the total capacitance of $C_S + C_{S,AUX}$ during the sampling and integration phases. During the discharging phase, a first-order approximation of the circuit reveals that the NBW in this phase is also similar to that of the sampling phase. Therefore, the proposed integrator maintains noise performance while, as discussed earlier, enabling either a low-area or low-power implementation for SC integrators.

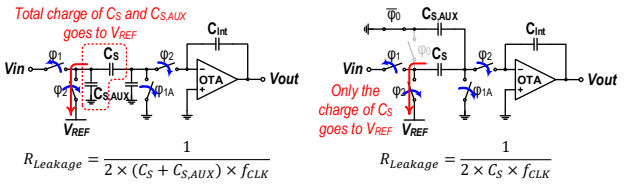


Fig. 4. The importance of the discharging phase in decreasing the leakage current between Vin and V_{REF}

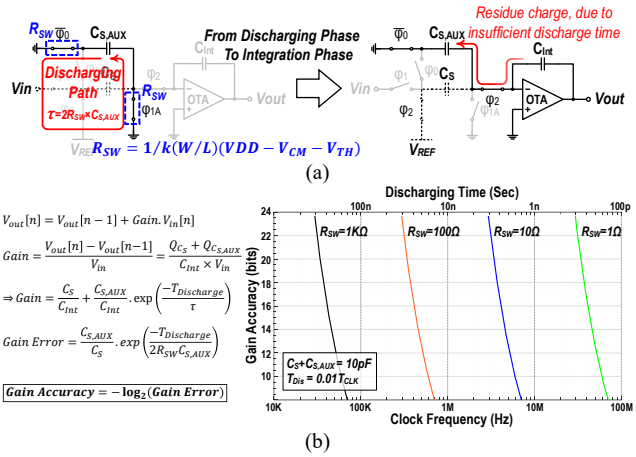
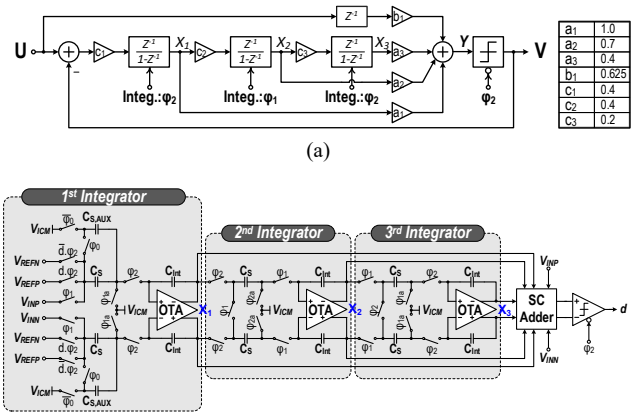


Fig. 5. a) The introduced gain error associated with the discharging time, and b) the minimum required discharging time versus switch resistance

It should be noted that although $C_{S,AUX}$ only serves to limit the NBW of the integrator, it must not be placed directly at the input and summing node of the OTA. In this case, as shown in Fig. 4(a), the total charge captured on C_S and $C_{S,AUX}$ is injected into V_{REF} during the transition from the sampling phase to the integration phase. This increases the leakage between V_{in} and V_{REF}, similar to what occurs in shared sampling capacitor architectures. In contrast, as shown in Fig. 4(b), in the proposed configuration, thanks to the discharging phase, only the charge stored on C_S is injected to V_{REF}, which is only a fraction of the total charge of C_S and $C_{S,AUX}$. This significantly reduces the leakage between Vin and V_{REF}. As a result, the required V_{REF} can be provided by a voltage buffer with a higher output impedance, thereby reducing overall power consumption while maintaining the same performance.

B. Linearity

As explained above, the discharging phase plays a crucial role in breaking the gain-area-noise trade-off. As shown in Fig. 5(a), if the duration of this phase is insufficient to completely discharge $C_{S,AUX}$, the residual charge will be transferred to C_{Int}, introducing an extra gain error. This gain error depends on the discharging time, the time constant of



(a)

(b)

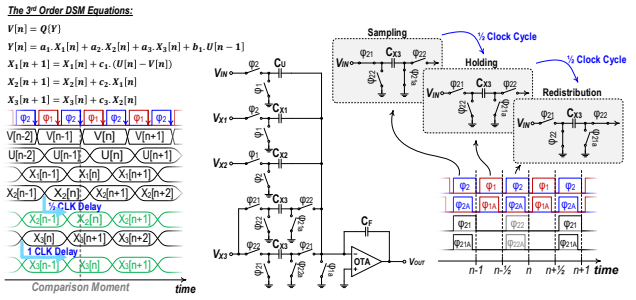
Fig. 6. The implemented third-order DSM incorporating the proposed integrator. a) Block diagram of the implemented modulator, and b) circuit implementation

the discharging path, and the ratio of $C_{S,AUX}/C_S$, all of which are independent of the input voltage level. As a result, insufficient discharging time does not introduce nonlinearity into the circuit, and the resulting gain error can be minimized by allocating sufficient time to the discharging phase, which is easily achievable in DT-DSMs. Fig. 5(b) demonstrates the gain accuracy of the integrator versus its clock frequency for various discharging path time constants, assuming $C_{S,AUX}/C_S$=10, a total capacitance of 10pF, and assigning 1% of the clock period to the discharging phase. As shown, the gain error introduced by insufficient discharging time is not the design bottleneck, even in high-frequency integrators.

III. Delta Sigma Modulator

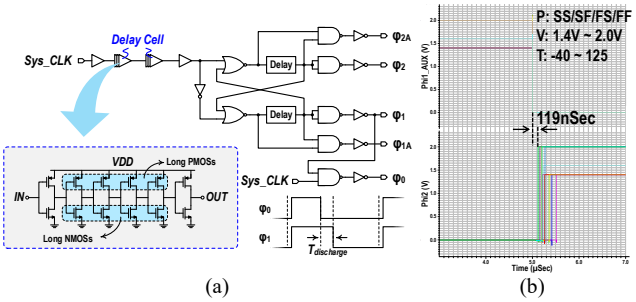
In this work, as a proof of concept, a third-order DT-DSM was implemented by incorporating the proposed integrator into the first stage of the modulator. Fig. 6 shows the detailed implementation of the DSM, which employs a CIFF architecture along with a single-bit quantizer to achieve maximum linearity due to the inherent linearity of single-bit DACs. To meet the required SNR, 2.1pF and 6.3pF capacitors were utilized to implement C_S and $C_{S,AUX}$, respectively, resulting in a total capacitance of 8.4pF. Thanks to the proposed integrator, only a 9.5pF capacitor was needed to realize C_{Int}, instead of a 38.2pF capacitor required in conventional configurations to achieve the same voltage gain, resulting in a 61.5% reduction in total capacitance. Furthermore, to relax the speed requirements of the OTAs and reduce the overall power consumption, integrators with a delaying architecture were employed in the DSM.

As shown in Fig. 7, employing delaying integrators introduces timing misalignment in the signals required at the input of the quantizer (X1 to X3). To ensure correct data is available before the comparison moment (falling edge of φ_2), each signal must be delayed by a specific number of clock cycles, as indicated in Fig. 7(a). A non-delay (Z^0) and a half–delay ($Z^{-½}$) sampling network are implemented by appropriately arranging the sampling and charge redistribution phases. In this work, to implement a full–delay (Z^{-1}) sampling network, a switched capacitor sampling circuit is proposed in which the sampling phase is aligned with the previous charge redistribution phase of the half–delay network. However, before the charge redistribution phase begins, a half–clock cycle is intentionally skipped, resulting in a sampling network with one clock cycle of delay.



(a) (b)

Fig. 7. Time misalignment issue in DT-DSMs due to the use of delaying integrators. a) The required data, and b) the proposed SC adder to provide appropriate data for the quantizer



(a) (b)

Fig. 8. The circuit diagram of the phase generator, along with its PVT simulation results

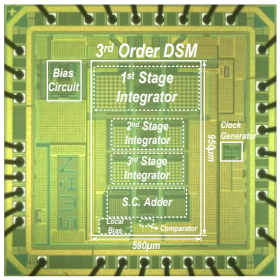


Fig. 9. Chip micrograph

Additionally, to avoid missing data caused by the skipped half–cycle, a ping-pong configuration is implemented for the full–delay network.

Lastly, Fig. 8(a) shows the circuit diagram of the phase generator, where the required discharging time is created using a cascade of two delay cells. To ensure allocating sufficient time to this phase to meet the required gain accuracy (>18bit) despite process, supply voltage, and temperature (PVT) variations, several simulations were performed under various PVT conditions in the presence of parasitic capacitance from the metallization, and the result is also shown in Fig. 8(b).

IV. Measurement Results

Fig. 9 shows the die micrograph of the DSM prototype, fabricated using a 180nm CMOS technology, occupying an area of 0.56mm^2. The modulator was tested using a 1.6V supply voltage and a 100KHz clock signal with an oversampling ratio (OSR) of 250. Fig. 10 presents the measured output spectrum of the modulator along with its input-referred noise. In this spectrum, two distinct harmonics at 100Hz and 150Hz are visible, originating from the input signal source, as confirmed by the output spectrum of the function generator, shown in Fig. 10. The DSM achieves an SNR of 104.9dB and an SNDR of 101.2dB at an input frequency of 66.185Hz (one-third of the DSM bandwidth to

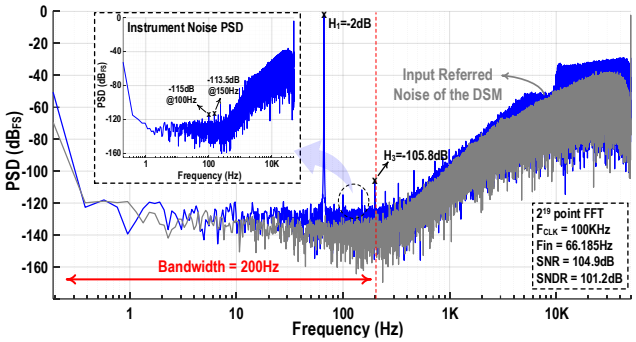


Fig. 10. The measured output spectrum of the DT-DSM, including the output spectrum of the function generator

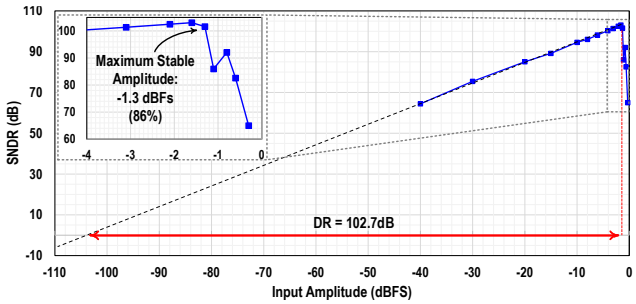


Fig. 11. The measured dynamic range of the DT-DSM

introduce the worst distortion). Additionally, the DSM exhibits a dynamic range of 102.7dB, as shown in Fig. 11. To evaluate the performance of the proposed integrator, the SNDR was measured across different input frequencies and supply voltages using five chips. The measurement results are depicted in Fig. 12(a) and 12(b), confirm that the performance of the DSM remains stable under various conditions, demonstrating the robustness of the proposed integrator.

The DSM consumes 53.5µW at a 1.6V supply voltage, with the power breakdown shown in Fig. 12(c), resulting in a figure of merit (FOM) of 166.9dB. The performance of the DSM is summarized in Table I, along with a comparison to state-of-the-art DT-DSMs. Although the designed DSM targets a relatively low bandwidth – constrained by the requirements of the intended project – the proposed integrator can be employed in various DSM topologies with wider bandwidths, supporting clock frequencies up to 100MHz, as demonstrated earlier in Fig. 5(b).

V. Conclusion

This paper presents a proposed SC integrator suitable for DT-DSMs, in which the gain-area-noise trade-off in conventional integrators is eliminated by splitting the sampling capacitor and introducing a new phase, referred to as the discharging phase. In the proposed integrator, the sampling and integration capacitors can be selected to define the desired gain in a way that either decreases the total chip area or reduces the power consumption, while the required SNR can be achieved by selecting the proper value for the auxiliary sampling capacitor. In this work, as a proof of concept, a third-order DT-DSM was successfully implemented using the proposed integrator in a 180nm CMOS technology. Measurement results demonstrate the performance and robustness of the proposed integrator under various conditions.

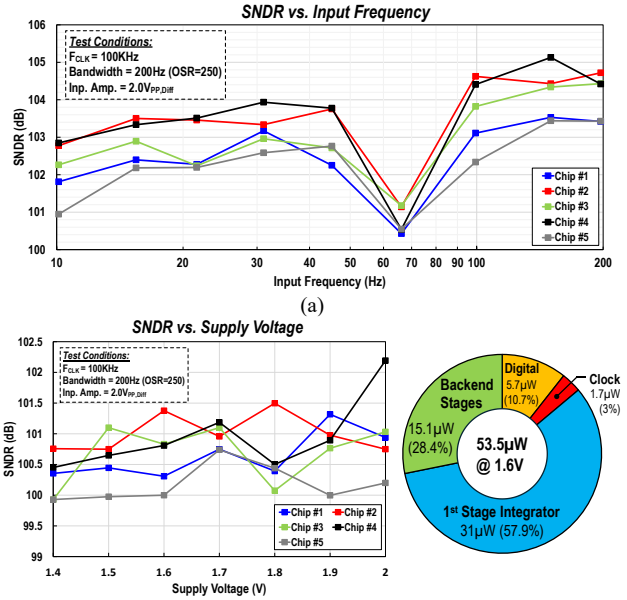


Fig. 12. The Measured SNDR versus a) input frequency, b) supply voltage, and c) the power breakdown of the DSM

Table I. Performance summary of the DT-DSM along with the state-of-the-art works

	This Work	ISSCC'18 [3]	VLSI'18 [4]	JSSC'19 [5]	ASSCC'22 [6]	TBCAS'24 [7]
Technology (nm)	180	180	180	65	180	180
Supply Voltage (V)	1.6	3	3	1.2	1.8	1.8/1.2
Architecture	DT-ΔΣ	Incremental DT-ΔΣ	Two Step IADC	IADC	Two Step IADC	Zoom DT-ΔΣ Counting
Area (mm²)	0.56	0.363	0.72	0.13	0.139	0.75
Sampling Freq. (MHz)	0.1	30	55	10.24	0.96/0.64	0.256
BW (KHz)	0.2	100	625	20	20	1
SNR (dB)	104.9	87.3	97.3	NA††	NA††	104.9
SNDR (dB)	101.2	86.6	96.6	100.8	89.1	99.3
DR (dB)	102.7	91.5	100.1	101.8	91	107.6
Power (µW)	53.5	1098	27700	550	358.4	130
FOM† (dB)	166.9	166.2	170.1	176.4	166.6	168.2

†FOM = SNDR + 10log(Bandwidth/Power) ††Not Available

Acknowledgment

This work was supported by the SWAN-on-Chip project, funded by the European Union's Horizon 2021-CL4-2021-Digital-Emerging.

References

[1] Q. Fan et al., "A 1.8 µW 60 nV/√Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," IEEE JSSC, vol. 46, no. 7, pp. 1534-1543, July 2011, doi: 10.1109/JSSC.2011.2143610.

[2] Pavan, Shanthi., Schreier, Richard., Temes, Gabor C., "Understanding Delta-Sigma Data Converters" Germany: Wiley, 2016.

[3] P. Vogelmann et al., "A 1.1mW 200kS/s incremental ΔΣ ADC with a DR of 91.5dB using integrator slicing for dynamic power reduction," ISSCC, 2018, doi: 10.1109/ISSCC.2018.83110271.

[4] T. Katayama et al., "A 1.25MS/S Two-Step Incremental ADC with 100DB DR and 110DB SFDR," VLSI, 2018, doi: 10.1109/VLSIC.2018.8502298.

[5] B. Wang et al., "A 550- µ W 20-kHz BW 100.8-dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC With 256 Clock Cycles in 65-nm CMOS," IEEE JSSC, vol. 54, no. 4, pp. 1161-1172, April 2019, doi: 10.1109/JSSC.2018.2888872.

[6] J. -S. Huang et al., "A 91-dB DR 20-kHz BW 5th-Order Multi-Step Incremental ADC for Sensor Interfaces by Re-Using a MASH 2-1 Modulator," A-SSCC, 2022, doi: 10.1109/A-SSCC56115.2022.9980590.

[7] L. Fang et al., "A 107.6 dB-DR Three-Step Incremental ADC for Motion-Tolerate Biopotential Signals Recording," TBCAS, vol. 18, no. 1, pp. 111-122, Feb. 2024, doi: 10.1109/TBCAS.2023.3312976.