A 12-to-20Gb/s, 2.93-pJ/bit Jitter-Filtering Retimer with High Input Jitter Tolerance in 28nm CMOS

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***Abstract*—A jitter-filtering retimer is presented with a wide-bandwidth injection-locked oscillator (ILO) based input clock-and-data recovery (CDR) unit cascaded with a jitter filter phase-locked loop (PLL) that generates low-jitter clocks for the output transmitter that serializes and retimes the recovered data. The input ILO-based CDR employs a quarter-rate architecture for efficient wide-range operation and utilizes a digital loop filter with pattern filtering for robust input delay line and ILO frequency control. Fabricated in 28nm CMOS, the proposed retimer operates from 12-20Gb/s, achieves the widest-reported 20Gb/s jitter tolerance (JTOL) of 1UI$_{PP}$ at a 173MHz sinusoidal jitter (SJ) frequency and an estimated JTOL bandwidth in excess of 500MHz, and consumes 58.66mW.**

***Index Terms*—Clock and data recovery (CDR), injection-locked CDR, jitter-filtering, jitter tolerance (JTOL), retimer IC.**

I. Introduction

Serial I/O data rates are increasing in order to support the bandwidth requirements of image sensors for automotive applications such as advanced driver assistance systems (ADAS). As the data symbol times shrink with higher data rates, this results in an increased amount of inter-symbol interference (ISI) for transmission over severe low-pass channels and increased sensitivity to overall jitter with higher frequency content. To address this, retimer ICs are required that have both high input jitter tolerance (JTOL) and low output jitter for destination IC receivers to track the recovered data. However, there are challenges associated with wide-bandwidth CDR implementations, as stability and power considerations make achieving CDR bandwidths greater than 100MHz prohibitive in conventional PLL-based [1] and phase rotator (PR)-based [2] CDRs. Achieving wide input bandwidth and maintaining low output jitter also often contradict each other because wide bandwidth also allows more input jitter to pass through to the CDR. This results in increased output jitter, causing the recovered clock and data signals to exhibit high-frequency jitter beyond the tracking bandwidth of the destination receiver's CDR.

While prior works have demonstrated the effectiveness of injection-locked oscillator (ILO)-based CDR in achieving high JTOL performance [3], [4], a fundamental trade-off remains unaddressed. Specifically, the high JTOL of CDR implies minimal filtering of input jitter, which may result in substantial residual jitter on the recovered clock. This leads to degradation in bit-error rate (BER) performance when evaluating the output of the CDR directly. Consequently, previous works have resorted to either on-chip PRBS checkers or BER testing on deserialized data to circumvent this limitation, as direct BER measurement on the CDR output is affected by jitter.

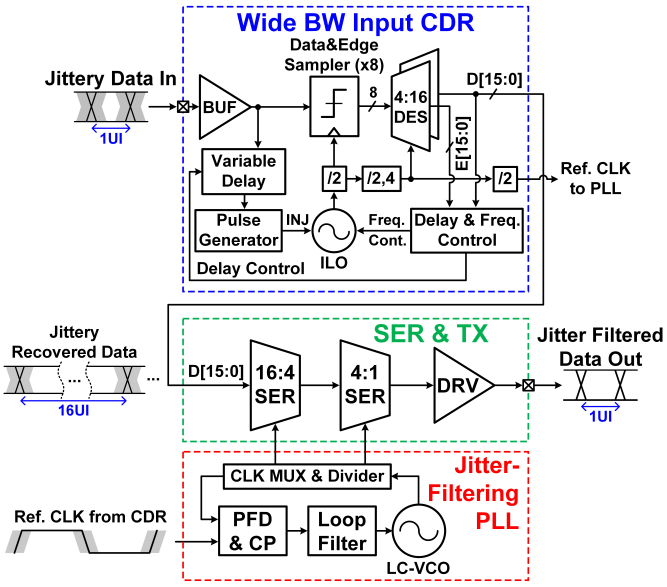

Fig. 1. Block diagram of proposed retimer.

In this work, a jitter-filtering retimer with a wide-bandwidth CDR is proposed to provide both high input JTOL and low output jitter. The proposed retimer consists of a wide-bandwidth ILO-based CDR unit, a cascaded low-bandwidth LC phase-locked loop (PLL) for jitter filtering, and a transmitter (TX) for serialization. Measurement results show that the proposed retimer achieves the widest-reported JTOL bandwidth in excess of 500 MHz at 20Gb/s.

II. Retimer Architeture

Fig. 1 shows the block diagram of the proposed retimer. After passing through an input buffer that includes T-coil termination and ESD circuitry, the data goes to the input CDR that has a quarter-rate architecture and utilizes an ILO. While the input CDR offers high input JTOL capability, its recovered clock can still exhibit a significant amount of jitter due to its wide jitter transfer bandwidth. Consequently, it is not ideal for achieving a low-jitter retimed TX output. To

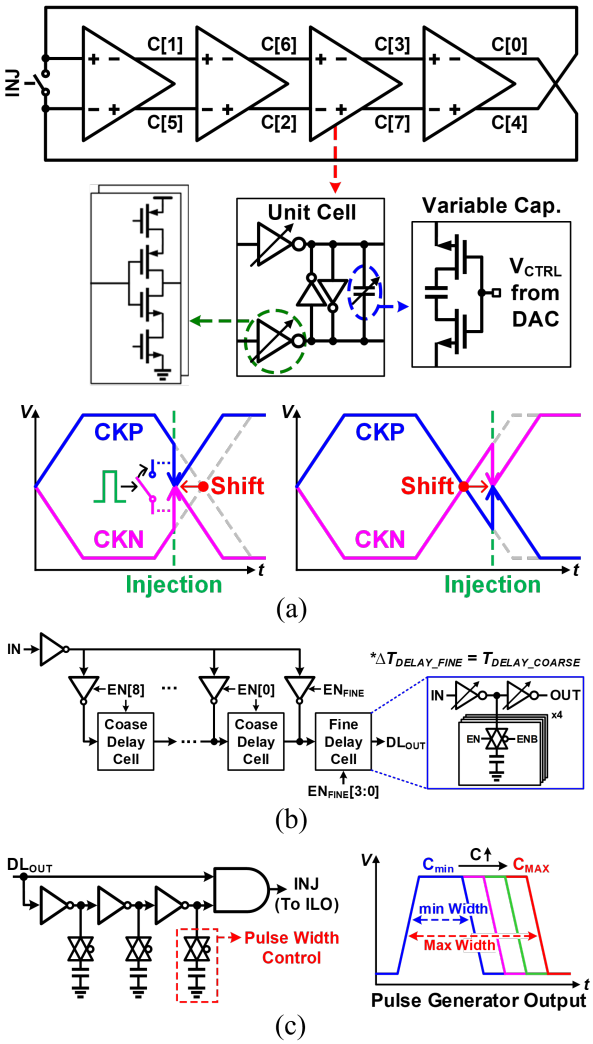

Fig. 2. (a) Input CDR ILO and illustration of injection effect. (b) Variable delay line. (c) Pulse generator.

address this challenge, a cascaded low-bandwidth LC-PLL is designed, leveraging the recovered clock of the input CDR as the reference clock source for jitter filtering. Clocked by the jitter-filtering PLL, the output TX performs data retiming and serialization. T-coil termination and ESD circuitry are also included in the TX output driver.

III. Circuit Implementation

A. Wide Bandwidth Input CDR

To achieve wide bandwidth, an ILO-based input CDR is implemented. Compared to a conventional second-order CDR, the ILO-based CDR achieves wider input bandwidth by directly injecting the incoming data transitions and correcting the clock phase without being constrained by the low-pass characteristics of a loop filter.

Main building blocks of the input CDR are ILO, variable delay line, pulse generator, and delay/frequency control loop. The ILO block diagram is shown in Fig. 2(a). ILO segment control provides coarse frequency tuning and a variable capac-

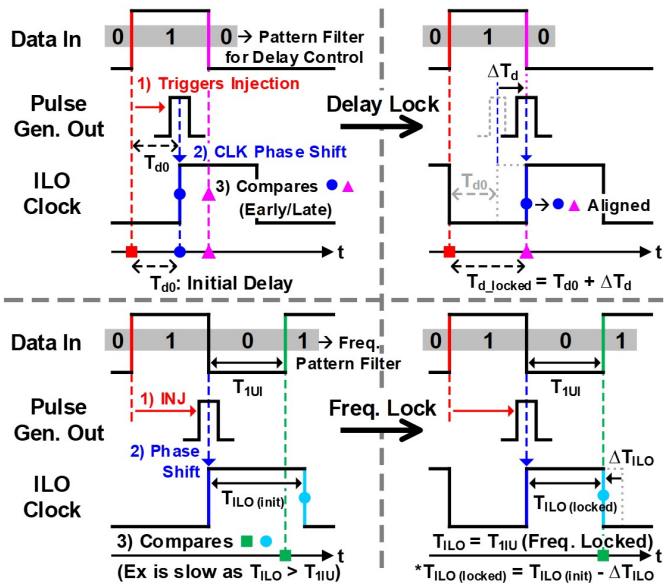

Fig. 3. Delay line control (top) and ILO frequency control (bottom).

itor is used for fine frequency tuning. This frequency tuning scheme does not change the output common mode level of the ILO, thereby rendering it suitable for driving the following inverter-based circuitry. Upon the arrival of the injection pulse, the injection switch shorts the differential clock of the ILO to shift the zero-crossing point. The variable delay line and pulse generator are shown in Fig. 2(b). While the delay line can also be implemented with logic gates [3], an inverter-based delay line is chosen to support higher data rates of up to 20Gb/s. The pulse generator, which is driven by the delay line, takes the rising edge of the data and generates an injection pulse to drive ILO. To modulate the pulse width according to the various data rates, switched capacitors are added.

While the ILO has the capability to adjust its clock phase to incoming injection pulse rapidly, it does this without discerning if the data is being sampled at the ideal timing center point. To maximize timing margin and thereby JTOL performance, a digital-loop filter (DLF) controls both the delay line and ILO free-running frequency. Fig. 3 describes how the DLF robustly controls the delay line and ILO frequency by utilizing data transition pattern filtering. A rising edge in the data stream (red) triggers pulse injection, making the ILO clock edge (blue circle) aligned with the injection. For delay control, the DLF generates early/late decisions by comparing the ILO clock edge with the falling data edge (pink triangle). The DLF then controls the delay between rising edge in the data stream and injection pulse (T_d). Similarly, the DLF can determine if ILO is running faster or slower than the data by comparing ILO clock edge (light blue circle) with data edge (green square).

B. Jitter-filtering PLL

Details of the jitter-filtering LC-oscillator-based PLL are shown in Fig. 4. A low PLL loop bandwidth of below 5MHz is intended to effectively suppress the high-frequency jitter

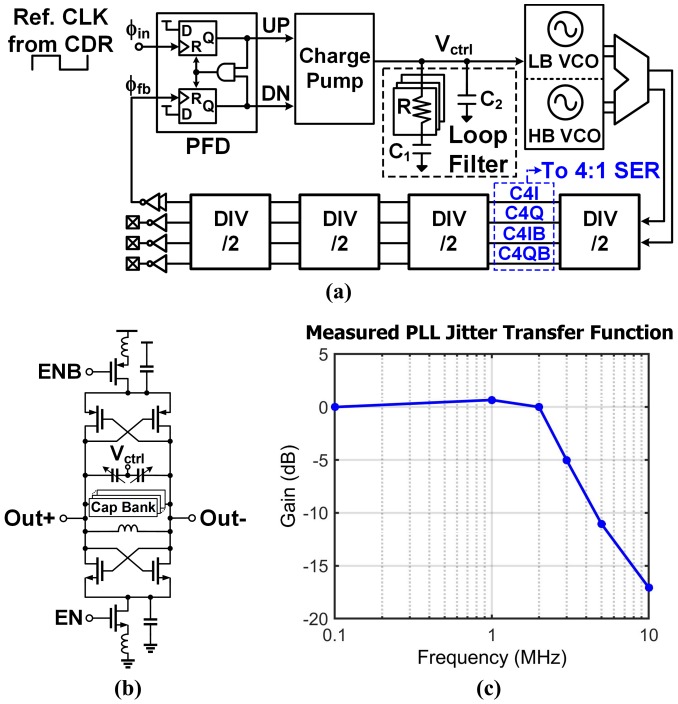

Fig. 4. (a) Jitter-filtering PLL block diagram. (b) LC-VCO schematic. (c) Measured jitter transfer function of the PLL.

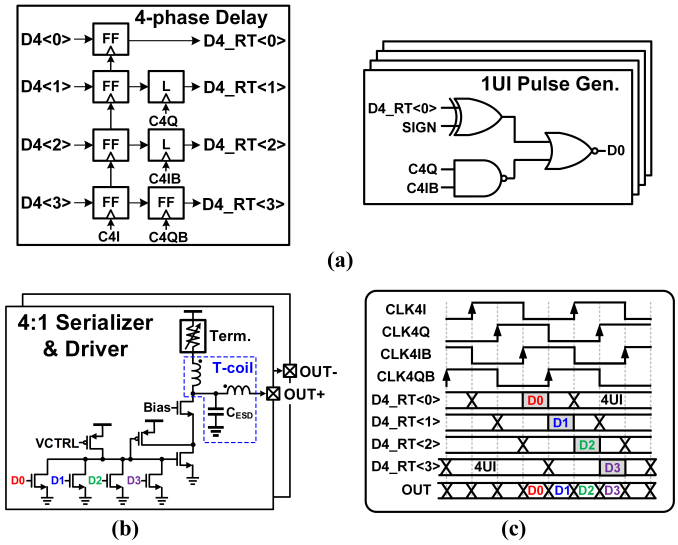

Fig. 5. (a) 4-phase delay and 1UI pulse generator block diagram. (b) Unstacked 4:1 serializer and tail-less output driver schematic. (c) Transmitter timing diagram.

that the input CDR recovered clock might possess. In contrast to the input CDR, an LC-VCO is selected for the oscillator architecture due to its lower phase noise relative to the ring-VCO alternative. A tail LC-filtering, shown in Fig. 4(b), achieves additional phase noise improvement. Two VCOs are implemented to cover the required clock frequency range and CML MUX selects between the two VCO outputs. The VCO output is then passed through a divider that generates 4-phase clock signals for the quarter-rate serializer in the output TX.

C. Serializer and output TX

The TX consists of a two-stage cascaded full-rate 16:4 serializer, an unstacked quarter-rate serializer, and a tail-less output driver. The full-rate 16:4 serializer initially outputs four parallel bits using clocks divided down from the PLL.

For 4:1 serialization, the 4UI-wide data must be segmented into 1UI-wide pulses before being passed to the unstacked quarter-rate 4:1 serializer. A 4-phase delay circuit staggers the data by 1UI, as shown in Fig. 5(a). This 4-phase delay enables carving of the 1UI-wide data at the third UI out of the four, providing sufficient timing margin for all four parallel bits. A double pass-transistor logic (DPL) NAND gate is used to generate a 1UI pulse and extract the third UI from the 4UI-wide data window.

The unstacked 4:1 serializer then delivers full-rate data to the tail-less output driver as shown in Fig. 5(b). The unstacked topology minimizes output bandwidth degradation along the full-rate data path [5]. To reduce parasitic capacitance, the pull-up resistor is implemented using a PMOS transistor. Fig. 5(c) shows the timing diagram of TX. The four-input unstacked device is driven directly by the 1UI-pulsed data.

A load-matched quadrature divider and integrated duty cycle correction (DCC) and quadrature error correction (QEC) circuits ensure accurate 4-phase clock generation, preventing increases in deterministic jitter (DJ). The output network comprises the output driver, ESD protection, and a T-coil. The T-coil compensates for bandwidth degradation introduced by the 2 kV Human Body Model (HBM) ESD protection and enhances return loss. Additionally, a programmable termination is incorporated to account for 3-sigma variations in the poly-resistor termination within the output network.

IV. Experimental Results

Fig. 6(c) shows the chip micrograph of the proposed retimer, which was fabricated in a 28nm CMOS process and occupies 0.4mm^2. The retimer operates from 12Gb/s to 20Gb/s with a 0.9V supply, consuming 58.66mW at 20Gb/s. Fig. 6(b) shows a BER=10^{-12} JTOL measurement with a PRBS7 input pattern from a BERT (Keysight M8050A). The jitter filtering capability of the retimer allows for excellent jitter tracking performance beyond the instrument's tracking limit at the jitter frequencies greater than 2MHz. At 20Gb/s, the JTOL is measured to be $1UI_{PP}$ at 173MHz sinusoidal jitter (SJ) frequency and $0.57UI_{PP}$ at 500MHz SJ frequency. Due to the equipment jitter generation limit of 500MHz, the JTOL floor does not appear in the plot. Fig. 6(a) demonstrates the jitter filtering effect of the proposed retimer by comparing the eye diagram measured at the input and output of the retimer. While the input eye diagram is completely closed due to $1UI_{PP}$ SJ being added, the retimed TX output has a wide eye opening. Table I summarizes the key performance of this work in comparison with state-of-the-art ILO-based CDRs, demonstrating the best JTOL performance at the highest data rate. It is important to note that as previous works only have

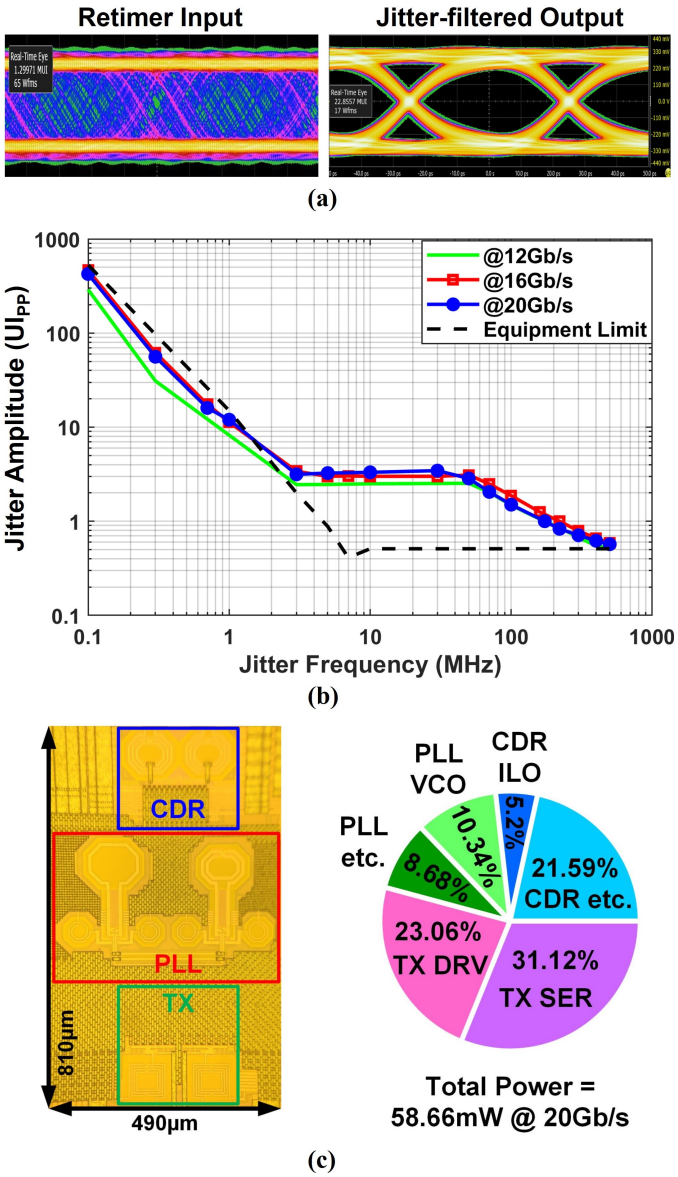

Fig. 6. Measurement results. (a) 20Gb/s eye diagram measured at the retimer input (left) and output(right). (b) JTOL measurements. (c) Die micrograph and power breakdown.

wide bandwidth CDR without jitter filtering feature, the BER had to be measured by either using an internal error checker [4] or at a deserialized rate [3] due to the recovered data still having a significant amount of jitter that exceeds the JTOL limit of most test equipment. The input CDR of this work also achieves the best energy efficiency of 0.79pJ/bit at 20Gb/s, which can be attributed to the power efficient quarter-rate architecture.

V. Conclusion

In this work, we present a jitter-filtering retimer that combines a wide input bandwidth—two features that are often at odds in conventional designs. The ILO-based CDR enables fast tracking of high-frequency input jitter, while a subsequent low-bandwidth PLL effectively filters out unwanted jitter components. The measured 20Gb/s JTOL bandwidth in excess of 500MHz and JTOL of $1UI_{PP}$ at 173MHz—obtained without the use of the internal BER checker—demonstrate the superior input jitter tracking and robust jitter filtering capability of the proposed retimer.

TABLE I. Performance Comparison

		ISSCC'08 [6]	JSSC'16 [4]	JSSC'19 [3]	This Work
Technology		250nm	28nm	28nm	28nm
Supply		3.3/1.8V	0.9V	0.9V	0.9V
Data Rate (Gb/s)		10.3125	1 – 12	10	12 – 20
Architecture		Full-rate	Half-rate	Half-rate	Quarter-rate
BER		< 1e-12	< 1e-9	< 1e-12	< 1e-12
JTOL	$1UI_{pp}$	@22MHz[1]	@120MHz[2]	@31MHz	@220[3]/173[4]MHz
	@300MHz	-[5]	$0.56UI_{pp}$[2]	$0.2UI_{pp}$	0.79[3]/0.71[4]UI_{pp}
	@500MHz	-[5]	-[5]	-[5]	0.59[3]/0.57[4]UI_{pp}
Jitter Filtering?		No	No	No	Yes
Energy Efficiency (pJ/bit)		83.01[6]	1.9[2,6]	1.28[6]	0.79[4,6] 2.93[4,7]

[1]Estimated from the JTOL measurement of 0.27UIPP @ 80MHz.
[2]At 12Gb/s. BER was measured using an internal error checker (Not external equipment).
[3]At 16Gb/s. [4]At 20Gb/s. [5]Not reported.
[6]CDR and receiver part only (Does not include jitter-filtering PLL and TX).
[7]Includes CDR, PLL, and TX.

Acknowledgment

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References

[1] A. Roshan-Zamir *et al.*, "A 56-Gb/s PAM4 receiver with low-overhead threshold and edge-based DFE FIR- and IIR-tap adaptation in 65-nm CMOS," *IEEE JSSC*, vol. 54, no. 3, pp. 672-684, Mar. 2019.

[2] G. Shu *et al.*, "A Reference-Less Clock and Data Recovery Circuit Using Phase-Rotating Phase-Locked Loop," *IEEE JSSC*, vol. 49, no. 4, pp. 1036-1047, April 2014.

[3] M.-S. Choo *et al.*, "A 10-Gb/s, 0.03-mm2, 1.28-pJ/bit half-rate injection-locked CDR with path mismatch tracking loop in a 28-nm CMOS technology," *IEEE JSSC*, vol. 54, no. 10, pp. 2812– 2822, Oct. 2019.

[4] T. Masuda *et al.*, "A 12 Gb/s 0.9 mW/Gb/s wide-bandwidth injection-type CDR in 28 nm CMOS with reference-free frequency capture," *IEEE JSSC*, vol. 51, no. 12, pp. 3204–3215, Dec. 2016.

[5] Z. Toprak-Deniz *et al.*, "A 128-Gb/s 1.3-pJ/b PAM-4 Transmitter With Reconfigurable 3-Tap FFE in 14-nm CMOS," *IEEE JSSC*, vol. 55, no. 1, pp. 19–26, Jan. 2020.

[6] J. Terada *et al.*, "A 10.3125Gb/s burst-mode CDR circuit using a ΔΣDAC," *IEEE ISSCC Dig. Tech. Papers*, pp. 226–609, Feb. 2008.