

# A 97% Peak-Efficiency Dual-Channel 3-Fine-Level Buck-Boost Converter with Capacitive Inrush Current Reduction and Seamless Mode Transition Using a Slim 0.65-Thickness Inductor

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**Abstract**—This paper presents a dual-channel 3-fine-level buck-boost converter designed for slim form-factor mobile devices with restricted component thickness. The proposed converter enables the use of a low-inductance (1 $\mu$ H) inductor by employing 3-fine-level operation while supporting heavy load current through current path distribution and inrush current reduction. Additionally, dynamic ramp offset control ensures seamless mode transitions. The converter, fabricated in a 0.25 $\mu$ m process, achieves a peak efficiency of 97% despite using a 0.65mm-thickness inductor with a volume of 2.08mm<sup>3</sup>.

**Keywords**— hybrid converter, inrush current reduction, low inductance, seamless mode transition, slim-form factor devices, three-level buck-boost converter

## I. INTRODUCTION

In battery-powered mobile devices such as smartphones and wearable devices, buck-boost converters are widely used to convert an input voltage ( $V_{IN}$ ) from a Li-ion battery (2.9 to 4.2V) into the required output voltage ( $V_{OUT}$ ) for various systems, including analog I/O (3.3V), OLED drivers (2.5 to 3.7V), etc., while handling heavy load current ( $I_{LOAD}$ ) of over several hundred milliamperes. As mobile devices become thinner, the thickness of external inductors becomes a key constraint in implementing a slim form-factor for power management system. Low-thickness (low-T) inductors typically exhibit the characteristics of small-volume inductors, where the parasitic resistance (DCR) rises sharply when the inductance increases, as shown in Fig. 1. Compared to inductors with a conventional thickness, low-T inductors experience much steeper increase in DCR with respect to their inductance, leading to reduced power efficiency, increased heat generation, and a limited voltage conversion ratio (VCR= $V_{OUT}/V_{IN}$ ) due to IR drop. Therefore, a buck-boost converter for slim form-factor devices should be designed based on the use of a low-inductance (low-L) inductor with lower DCR, to ensure high power efficiency across a wide VCR even under heavy  $I_{LOAD}$  conditions.

A buck-boost converter for a low-L inductor can be implemented by increasing the switching frequency or reducing the voltage swing across the inductor ( $\Delta V_L$ ). However, raising the switching frequency is typically constrained by factors such as switching losses, EMI noise, and the passive component characteristics. On the other hand, reducing  $\Delta V_L$  comes at the cost of a narrower VCR range, making single-mode buck-boost converters in [1-4] unsuitable for wide VCR applications when using a low-L inductor. Multi-mode converters in [5-9] may be employed to reduce  $\Delta V_L$  or extend the VCR range compared to single-mode designs. Notably, the converters in [8] and [9],

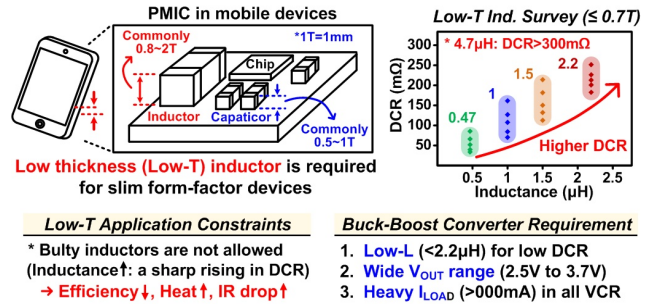


Fig. 1. Slim form-factor application with low thickness inductor.

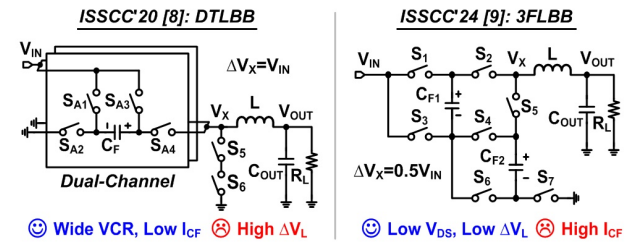


Fig. 2. Prior 3-level buck-boost converter topologies.

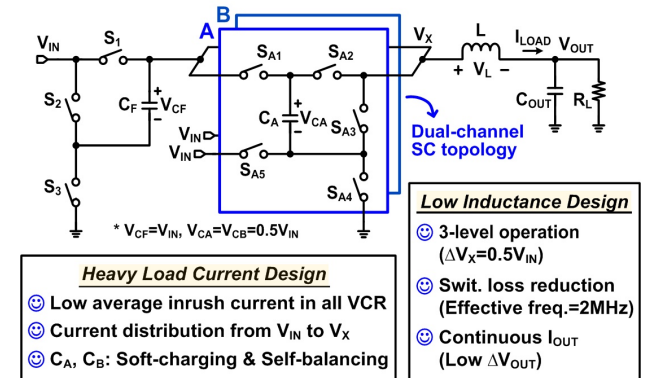


Fig. 3. Proposed dual-channel 3-fine-level buck-boost converter topology.

depicted in Fig. 2, adopt 3-level operation that offers lower  $\Delta V_L$  and continuous output current solely through an inductor path, resulting in low  $V_{OUT}$  ripple and eliminating RHP zero, which is beneficial for using a low-L inductor. However, although the converter in [9] is more advantageous for low-L design by reducing  $\Delta V_L$  to half compared to that in [8], its VCR range is also halved, potentially leading to a high inrush current issue. For example, when the VCR range closely matches to the operating range, the duty cycle ( $D$ ) is more likely to approach 0 or 1, shortening the hard-charging time relative to the soft-charging time. It causes excessive capacitive inrush current ( $I_{CF}$ ), which can decrease efficiency, potentially damage components, and limit the

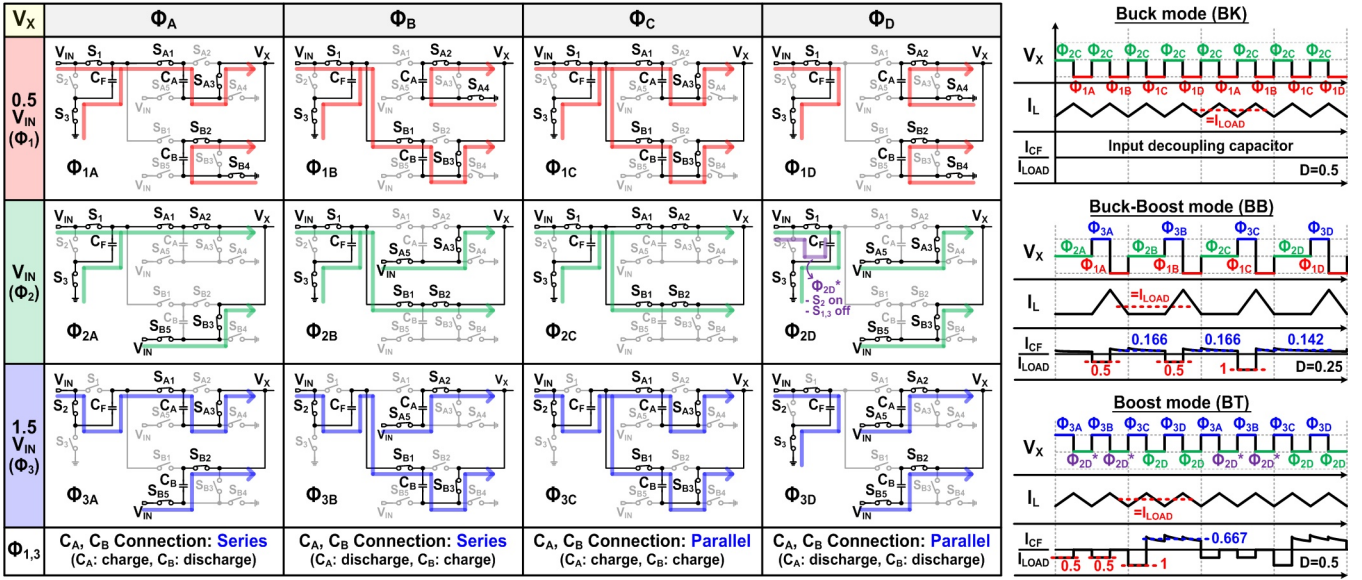


Fig. 4. Operation principle of the proposed converter with the conceptual waveforms in buck, buck-boost, and boost modes.

TABLE I. NUMBER OF SWITCHING EVENTS PER SWITCH IN 4 CYCLES OF  $V_X$

SW	$5V (V_{IN})$					$2.5V (0.5V_{IN})$					$5V (V_{IN})$				
	$S_1$	$S_2$	$S_3$	$S_{A1}$	$S_{A2}$	$S_{A3}$	$S_{A4}$	$S_{A5}$	$S_{B1}$	$S_{B2}$	$S_{B3}$	$S_{B4}$	$S_{B5}$		
BK	0	0	0	2	2	2	2	2	2	2	2	2	2		
BB	3	3	3	2	2	2	2	2	1	3	3	2	2		
BT	1	1	1	2	2	2	0	2	2	2	2	0	2		

- ☺ Number of switching events per switch in one period < 1
- ☺ Each channel has half-sized switches due to current distribution

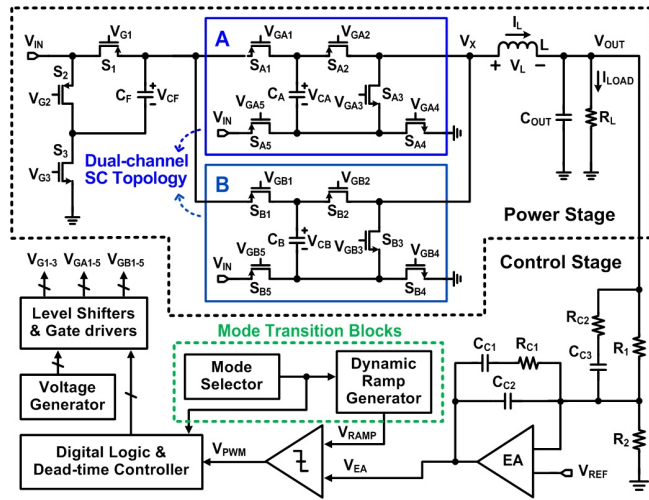


Fig. 5. Overall system architecture of the proposed converter.

$I_{LOAD}$  range. Thus, it is important to optimize  $\Delta V_L$  for the target operating range while balancing inductance and VCR range, with careful consideration of the high inrush current caused by hard-charging of capacitors.

## II. PROPOSED CONVERTER AND CONTROL SCHEME

### A. Dual-Channel 3-Fine-Level Buck-Boost Converter

To address the abovementioned issues, this paper presents a dual-channel 3-fine-level converter, as illustrated in Fig. 3, which operates with low  $\Delta V_L$  of  $0.5V_{IN}$  over the required VCR range while being optimized to use the low-L inductor with the 3-level topology that achieves reduced switching loss and continuous output current delivery. Additionally, the proposed converter adopts a soft-charging-based dual-channel switched-capacitor (SC) topology to

### Dynamic Ramp Offset Control

$$\text{Ramp offset} \rightarrow \begin{cases} W_{BB1} = W_{BK} - 0.5T_s \\ W_{BT} = W_{BB2} - 0.5T_s \end{cases}$$

- Same VCR is maintained  
→ Seamless mode transition

- BK ↔ BB  
 $0.5 + D_{BK}/2 = 0.5 + W_{BK}/2T_s$   
 $= 0.75 + W_{BB1}/2T_s = 0.75 + D_{BB}$

- BB ↔ BT  
 $0.75 + D_{BB} = 0.75 + W_{BB2}/2T_s$   
 $= 1 + W_{BT}/2T_s = 1 + D_{BT}/2$

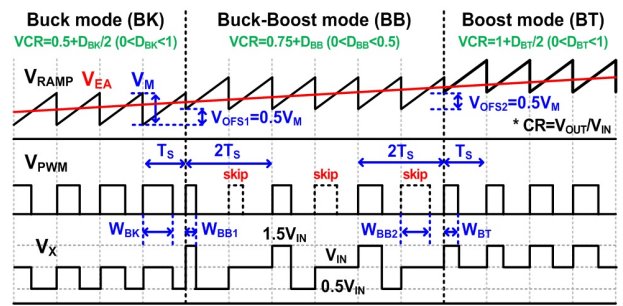
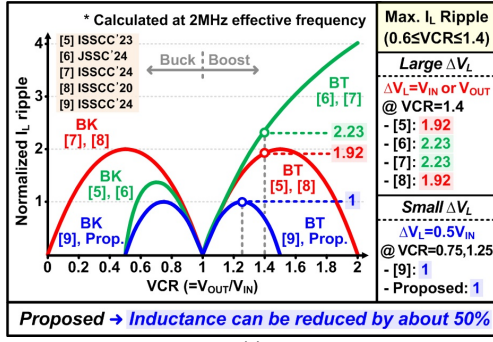


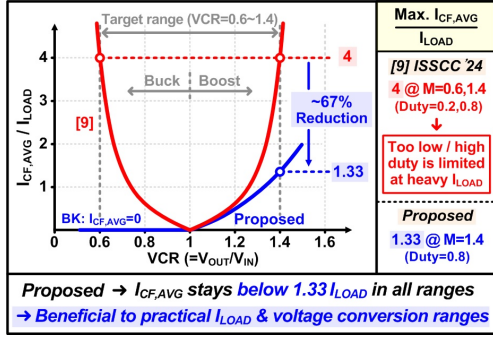
Fig. 6. Dynamic ramp offset control for seamless mode transition.

distribute the current from  $V_{IN}$  to  $V_X$  node, which helps maintain low capacitive inrush current even when the duty cycle approaches 0 or 1. During the all operation modes, both  $V_{CA}$  and  $V_{CB}$  are at  $0.5V_{IN}$  while  $V_{CF}$  is at  $V_{IN}$ .

Fig. 4 shows the operation principle of the proposed converter.  $\Phi_1$ ,  $\Phi_2$ , and  $\Phi_3$  represent switch operation where the  $V_X$  node is at  $0.5V_{IN}$ ,  $V_{IN}$ , and  $1.5V_{IN}$ , respectively. Depending on charging and discharging of flying capacitors ( $C_A$  and  $C_B$ ) during  $\Phi_1$  and  $\Phi_3$ , these operations are categorized into  $\Phi_A$ ,  $\Phi_B$ ,  $\Phi_C$ , and  $\Phi_D$ , resulting in a total of 12 switch operations. The converter alternates between  $\Phi_{1(A,B,C,D)}$  and  $\Phi_{2C}$  in buck (BK) mode, while operating between  $\Phi_{3(A,B,C,D)}$ ,  $\Phi_{2D}$ , and  $\Phi_{2D}^*$  in boost (BT) mode where  $\Phi_{2D}^*$  is the operation with switches  $S_1$ ,  $S_3$  off and switch  $S_2$  on to reduce switching losses. In buck-boost (BB) mode, all 12 operations are performed sequentially in the order of  $\Phi_2$ ,  $\Phi_1$ , and  $\Phi_3$  with  $\Phi_2$  having a fixed duty cycle that occupies half of each period. Across all operating modes, the capacitive inrush current, which varies in its average value with  $D$ , occurs only in  $C_F$ , as  $C_A$  and  $C_B$  are always soft-charged or soft-discharged by the inductor. Additionally, the sizes of switches ( $S_{A1-5}$  and  $S_{B1-5}$ ) can be reduced by half due to current distribution



(a)



(b)

Fig. 7. Comparison of (a) inductor current ripple and (b) capacitive inrush current for the proposed converter with prior arts.

through the dual-channel configuration, mitigating the area penalty. Meanwhile, the switching frequency of each switch is lower than the effective switching frequency relative to the  $V_X$  node, as shown in Table I, leading to reduced switching losses.

### B. System Architecture and Seamless Mode Transition

Fig. 5 illustrates the overall system architecture of the proposed converter, including both the power and control stages. The dual-channel configuration with  $C_A$  and  $C_B$  alternates between series and parallel connections, enabling self-balancing operation to correct small voltage mismatch generated during series connection when they are later connected in parallel. In the control stage, an adaptive ramp generator facilitates seamless mode transitions through a dynamic offset control, as shown in Fig. 6. When the ramp signal ( $V_{RAMP}$ ) reaches a height of  $V_M$ , an offset of  $0.5V_M$  is added or subtracted during mode transition, resulting in a VCR offset of 0.25 between BB and other modes. This offset adjustment ensures that the VCR remains continuous across different operating modes, preventing abrupt change in  $V_{OUT}$ .

### C. Comparison with Prior Arts

Fig. 7(a) compares the normalized inductor current ripple ( $\Delta I_L$ ) between previous works and the proposed converter, assuming identical inductance and frequency.  $\Delta I_L$  of converters with large  $\Delta V_L$  ( $V_{IN}$  or  $V_{OUT}$ ) in [5-8] are normalized to the maximum  $\Delta I_L$  value of the proposed converter operating with small  $\Delta V_L$  ( $0.5V_{IN}$ ). Within the target VCR range ( $0.6 \leq VCR \leq 1.4$ ), the normalized maximum  $\Delta I_L$  values are 1.92 for  $\Delta V_L = V_{IN}$  and 2.23 for  $\Delta V_L = V_{OUT}$ . These results indicate that the required inductance can be approximately halved while maintaining the same  $\Delta I_L$  if the converter operates with  $\Delta V_L$  of  $0.5V_{IN}$ . Fig. 7(b) compares the average capacitive inrush current ( $I_{CF,AVG}$ ) normalized to  $I_{LOAD}$  between the converter in [9] and the proposed

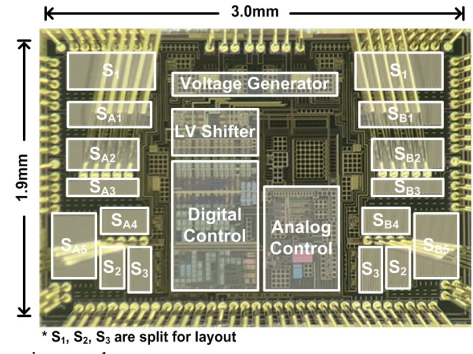


Fig. 8. Die micrograph.

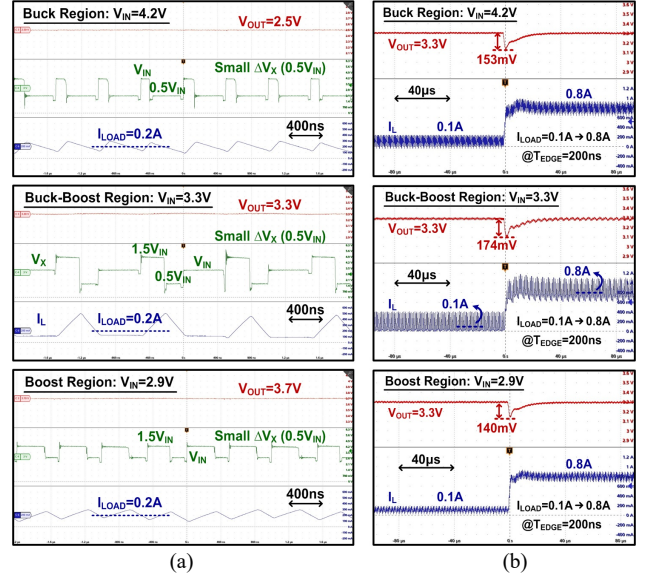


Fig. 9. Measured (a) steady-state and (b) load transient waveforms at different operation modes.

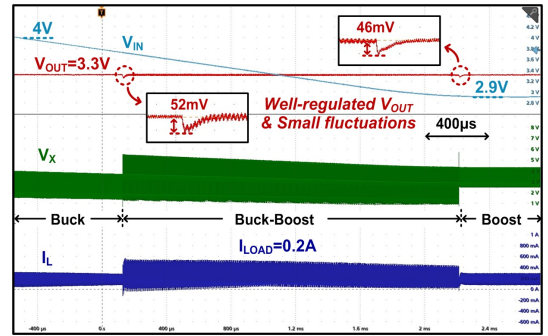


Fig. 10. Seamless mode transition waveform.

converter, both operating with small  $\Delta V_L$  of  $0.5V_{IN}$ . It is observed that the difference in  $I_{CF,AVG}$  between the converters sharply increases toward the edges of the target VCR range. For instance, the converter in [9] exhibits  $I_{CF,AVG}$  up to 4 times  $I_{LOAD}$  at VCR=0.6 and VCR=1.4, but the proposed converter has zero  $I_{CF,AVG}$  when VCR<1 and low  $I_{CF,AVG}$  up to 1.33 times  $I_{LOAD}$  at VCR=1.4. Since the proposed converter has lower  $I_{CF,AVG}$  across the entire VCR range, the practical operating range of both VCR and  $I_{LOAD}$  can be effectively extended, making it suitable for applications that require wide VCR and high  $I_{LOAD}$ .

## III. MEASUREMENTS RESULTS

Fig. 8 shows the die micrograph of the proposed buck-boost converter, fabricated in a  $0.25\mu\text{m}$  CMOS process,

TABLE II. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS

	[5] ISSCC'23 Jin	[6] JSSC'24 Zhao	[7] ISSCC'24 Ruan	[8] ISSCC'20 Baek	[9] ISSCC'24 Zhao	This Work			
Process	0.18 $\mu$ m BCD	0.18 $\mu$ m CMOS	0.18 $\mu$ m BCD	0.18 $\mu$ m CMOS	0.18 $\mu$ m CMOS	0.25 $\mu$ m CMOS			
Topology	Hybrid BB	Hybrid BB	Hybrid BB (Dual-channel)	3-Level BB (Dual-channel)	3-Level BB	3-Level BB (Dual-channel)			
Input Voltage [V]	2.7 - 4.2	2.7 - 4.2	2.7 - 4.2	2.5 - 5	2.8 - 4.2	2.9 - 4.2			
Output Voltage [V]	3.4	3.3	Sub1 - 6	0.4 - 9	3.3	2.5 - 3.7			
Load Current [A]	0.1 - 1	0.1 - 2.5	0.1 - 0.8	0.05 - 1	0 - 2	0.05 - 1	0.1 - 1.5		
Inductor	L [ $\mu$ H]	2.2	2.2	1.2	1	2.2	1		
	DCR [m $\Omega$ ]	170	8	110	N/A	N/A	110	8.5	70
	Thickness [mm]	1.2	5	0.9 <sup>A</sup>	N/A	N/A	0.9	4	0.65
	Volume [mm <sup>3</sup> ]	3	575	4.5	N/A	N/A	4.5	272	2.08
C <sub>OUT</sub> [ $\mu$ F] / C <sub>FLY</sub> [ $\mu$ F]	10 / 4.7	10 / 10	1 / 4.7x2	10 / 10x2	10 / 10x2	10 / 10, 4.7x2			
Effective Frequency [MHz]	1	2	2	0.8 - 3	2	2 (1 @ BB)			
Continuous I <sub>OUT</sub>	No	No	Yes <sup>B</sup>	Yes	Yes	Yes			
Seamless mode transition technique	Not reported	Dynamic ramp offset control	Dual ramp control	Not reported	Not used	Dynamic ramp offset control			
Peak Efficiency (%)	97.3	98.6	97.6	97.3	96.7	97.2	98.2	97.0	
Inductor Voltage Swing Level ( $\Delta V_L$ )	$V_{OUT}$ or $V_{IN}$	$V_{OUT}$	$V_{IN}$ or $V_{OUT}$	$V_{IN}$	$0.5 V_{IN}$	$0.5 V_{IN}$			
Normalized Max. I <sub>L</sub> -Ripple*	1.92	2.23	2.23	1.92	1	1			
Max. Average Inrush Current (I <sub>CF,AVG</sub> )**	1.2 I <sub>LOAD</sub> (VCR=0.6)	2 I <sub>LOAD</sub> (VCR=0.6)	0.175 I <sub>LOAD</sub> (VCR=1.4)	0.67 I <sub>LOAD</sub> (VCR=1.4)	4 I <sub>LOAD</sub> (VCR=0.6, 1.4)	1.33 I <sub>LOAD</sub> (VCR=1.4)			
Low $\Delta V_L$ & Max. I <sub>CF,AVG</sub> (Simultaneously)	No	No	No	No	No	No	Yes		

\* Normalized by maximum ripple value of the proposed converter  
 \*\* In the voltage conversion ratio (VCR) range from 0.6 to 1.4

<sup>A</sup> Calculated by the reported data  
<sup>B</sup> Except when D>0.5 in boost operation

operating with a 0.65mm-T 0806-sized inductor. Fig. 9(a) presents the measured steady-state waveforms for each operating region (BK, BB, BT). In the BK region, the  $V_X$  node swings between  $0.5V_{IN}$  and  $V_{IN}$ , while in the BB region,  $V_X$  alternates among  $0.5V_{IN}$ ,  $V_{IN}$ , and  $1.5V_{IN}$ . Similarly, in the BT region,  $V_X$  swings between  $V_{IN}$  and  $1.5V_{IN}$ . Fig. 9(b) shows the load transient response with a fixed  $V_{OUT}$  of 3.3V, where  $I_{LOAD}$  increases by 0.7A within 200ns edge time, demonstrating stable operation in all operating regions (BK, BB, BT) for  $V_{IN}$  of 2.9V, 3.3V, and 4.2V, respectively. Fig. 10 shows the seamless mode transition when  $V_{IN}$  is swept from 4V to 2.9V.  $V_{OUT}$  remains well-regulated across the entire  $V_{IN}$  range with small undershoots of 52mV and 46mV observed during the BK-to-BB and BB-to-BK mode transitions, respectively. Fig. 11 presents the measured power efficiencies according to  $I_{LOAD}$  under various  $V_{IN}$  and  $V_{OUT}$  conditions, achieving a peak efficiency of 97% at 0.2A and 93.7% at 1A. Table II summarizes and compares the performance of the proposed dual-channel 3-fine-level buck-boost converter with the state-of-the-art converters. The proposed converter exhibits a low inrush current up to 1.33 times  $I_{LOAD}$  with small  $\Delta V_L$  of  $0.5V_{IN}$ , while handling the high  $I_{LOAD}$  of 1.5A across a wide output voltage range from 2.5V to 3.7V. Additionally, the converter achieves a peak efficiency of 97%, which is comparable to that of the prior works, despite utilizing a low-L inductor with a minimal thickness of 0.65mm and a compact volume of 2.08mm<sup>3</sup>.

#### IV. CONCLUSION

The proposed converter leverages 3-level topology to achieve a low  $\Delta V_L$ , an increased effective switching frequency, the elimination of the RHP zero, and continuous output current delivery. Additionally, the soft-charging-based dual-channel architecture efficiently distributes current from  $V_{IN}$  to  $V_{OUT}$ , maintaining low inrush current across the entire VCR range. The design enables the use of a low-L inductor with low DCR and minimal thickness ( $\leq 0.65$ mm), which is essential for slim form-factor devices, while ensuring stable performance under heavy  $I_{LOAD}$  conditions. Furthermore, dynamic ramp offset control enables seamless mode

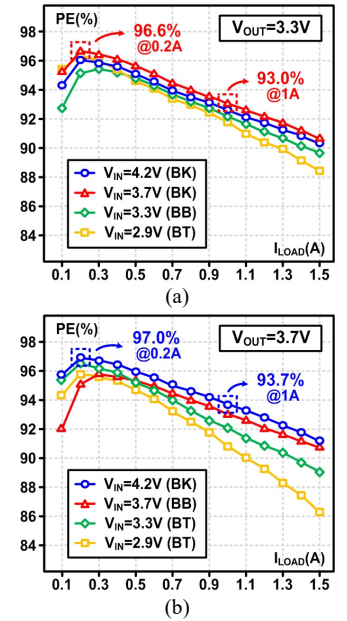


Fig. 11. Measured power efficiencies at various  $V_{IN}$  for (a)  $V_{OUT} = 3.3V$  and (b)  $V_{OUT} = 3.7V$ .

transitions, minimizing  $V_{OUT}$  fluctuations. The prototype chip operates over a wide VCR range ( $V_{IN}=2.9$  to 4.2V,  $V_{OUT}=2.5$  to 3.7V), delivering up to 1.5A of  $I_{LOAD}$  with a peak efficiency of 97%.

#### ACKNOWLEDGMENT

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