A 20-56 Gb/s Inductor-Less Optical Receiver with Passive Hybrid S2D and Octave-Rate Look-Ahead DFE in 28-nm CMOS

Xuxu Cheng*,[1], Hongzhi Wu*,[1], Liping Zhong[1], Weitao Wu[1], Yangyi Zhang[1], Zhenghao Li[1], Zhijian Chen[2], Quan Pan#,[1]
(*Equally contributed authors)
[1]School of Microelectronics, Southern University of Science and Technology, Shenzhen 518055, China
[2]School of Microelectronics, South China University of Technology, Guangzhou 511442, China
#Email: panq@sustech.edu.cn

***Abstract*—This paper presents a 56 Gb/s inductor-less optical receiver (RX) in 28-nm CMOS technology, featuring a passive hybrid single-ended to differential converter (S2D) and an octave-rate look-ahead decision feedback equalizer (DFE). The proposed passive hybrid S2D suppresses the group delay and gain mismatch by 85% and 78%, respectively. Benefiting from the octave-rate architecture and the proposed look-ahead DFE, this optical RX achieves data rates of 20-56 Gb/s (optical) and 20-72 Gb/s (electrical), and an optical energy efficiency of 1.9 pJ/b at 56 Gb/s with a compact area of 0.019 mm^2, which compares favorably with the state-of-the-art.**

Keywords—decision feedback equalizer (DFE), inductor-less optical receiver, octave-rate architecture, single-ended to differential converter (S2D).

I. Introduction

The rapid development of AI and machine learning has continuously increased the demand on the computing capability of data centers. In this scenario, optical interconnects using non-return-to-zero (NRZ) signaling are favorable due to the advantages of low bit error ratio (BER), low latency, and high bandwidth density [1-2]. To increase data rate to 50 Gb/s+, inductors are extensively used in previous works [2-5]. However, inductors enlarge the chip area, thereby limiting the number of I/Os and the overall data throughput of the optical interconnects. Besides, it complicates the routing of peripheral power supplies in flip-chip or advanced packaging. In contrast, the optical receiver (RX) without inductors improves the bandwidth density and area efficiency [6-7] by minimizing the data path area and placing a dense number of channels with a small pitch. Though the inductor-less optical RX has limited bandwidth extension capability, equalization techniques like feed-forward equalization (FFE) and decision feedback equalizer (DFE) help to broaden the bandwidth. Compared to FFE, DFE eliminates post-cursors without boosting high-frequency noise [8-9]. Among DFE topologies, the look-ahead DFE is popular since it has less stringent feedback timing constraints at higher data rates, which is realized by aligning all look-ahead signals before feedback operation. The look-ahead DFE typically adopts half-rate or quarter-rate architectures. As the data rate increases, clock generation and distribution for half-rate and quarter-rate architecture become more challenging at higher frequencies. As a result, the complex clock path design leads to a stringent power budget and large area.

This paper presents an inductor-less optical RX featuring a passive hybrid S2D and an octave-rate look-ahead DFE, aiming for high speed and high bandwidth density. To enhance the signal integrity at the slicer input, a passive hybrid S2D is proposed, which significantly suppresses group delay and gain mismatch. The octave-rate architecture allows for a halving of the clock frequency, alleviating the design burdens for generation and distribution in the clock path.

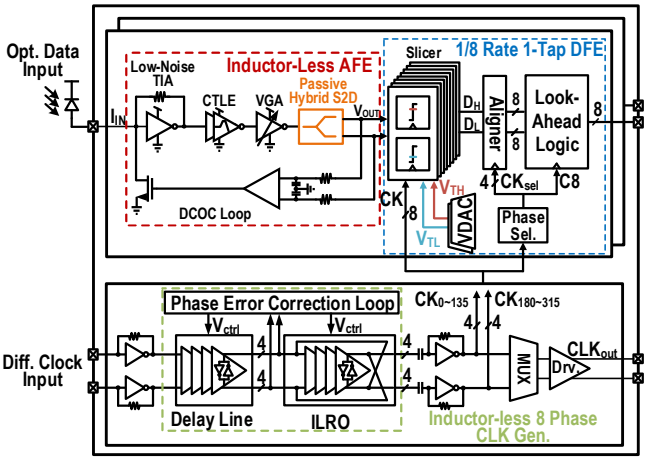

Fig. 1. Block diagram of the proposed inductor-less octave-rate optical RX.

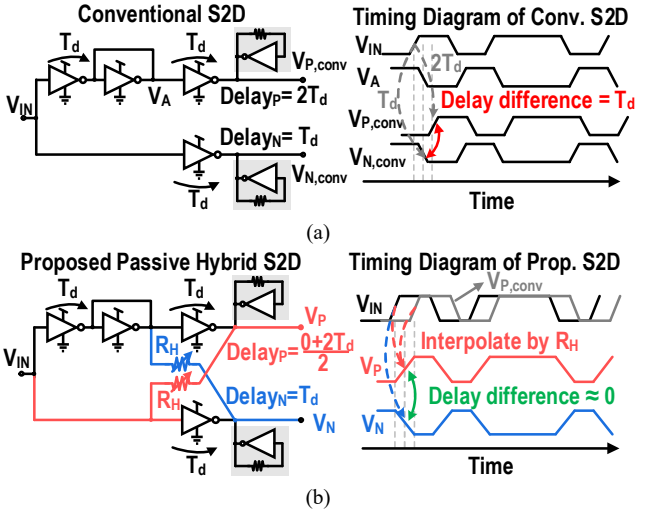

Fig. 2. Block diagram and timing diagram of (a) conventional S2D and (b) proposed passive hybrid S2D.

II. Inductor-less Optical RX

The overall architecture of the inductor-less octave-rate optical RX is illustrated in Fig. 1. Both the data path and clock path are inductor-less designs for compact area. The low noise trans-impedance amplifier (TIA) converts the photocurrent generated by the photodetector (PD) into an electrical signal. The continuous-time liner equalizer (CTLE) and variable gain amplifier (VGA) equalize and amplify the electrical signal

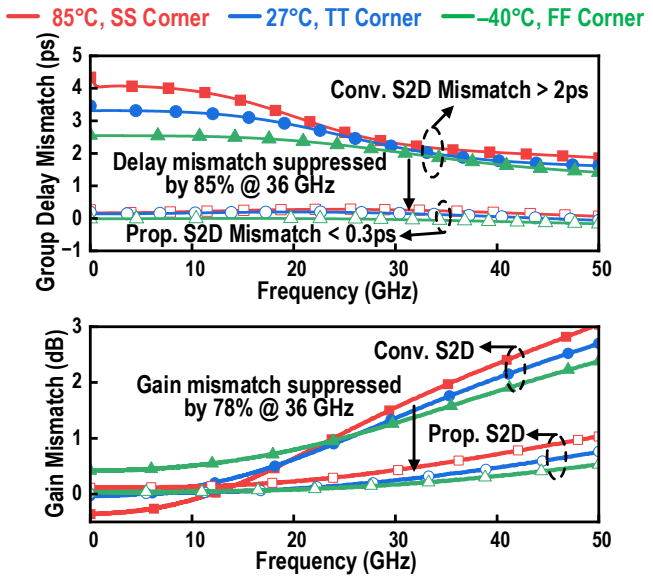

Fig. 3. Simulated group delay mismatch (top) and gain mismatch (bottom) of conventional S2D and proposed S2D.

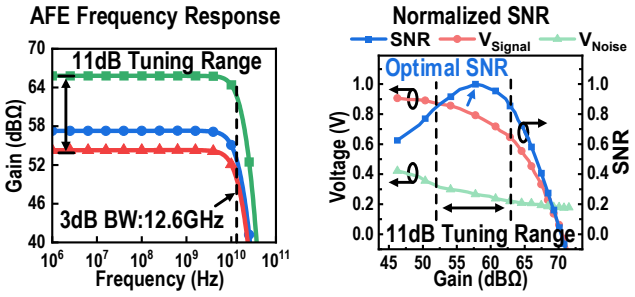

Fig. 4. Simulation results of (a) inductor-less AFE frequency response, and (b) system normalized SNR.

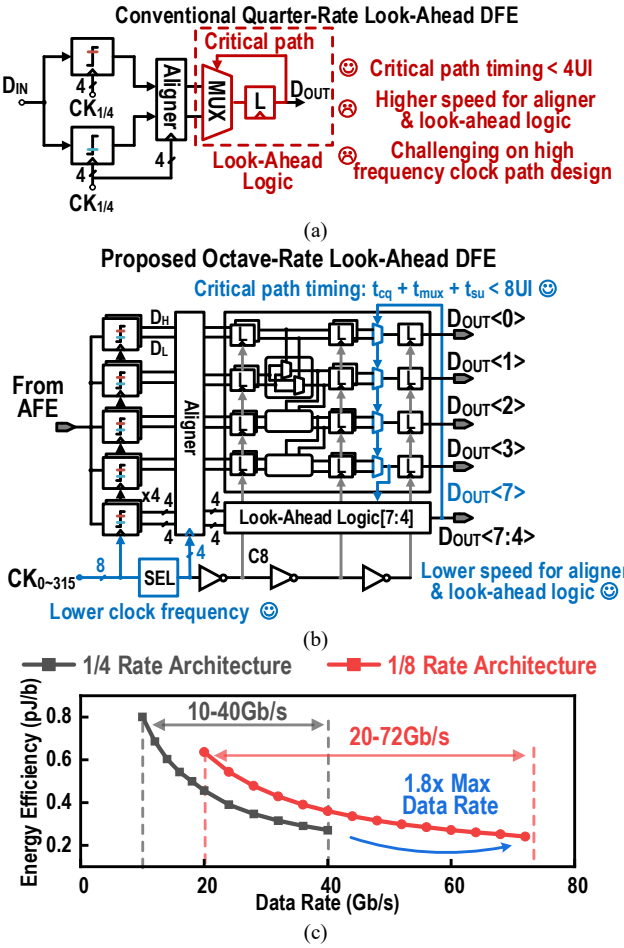

Fig. 5. (a) Conventional quarter-rate look-ahead DFE, (b) proposed octave-rate look-ahead DFE, and (c) comparison of quarter-rate and octave-rate architecture on energy efficiency and operation range.

from the TIA, and their bandwidth are further extended by active inductors. The passive hybrid S2D converts the VGA output into pseudo-differential signals V_{OUT}. The DC offset cancellation (DCOC) loop detects the common-mode voltage of V_{OUT} and feeds it back to the input of TIA to ensure proper DC operation points in the analog front-end (AFE). The octave-rate look-ahead DFE samples V_{OUT} and eliminates post-cursor in the following look-ahead logic. The clock path receives the differential clock signal and generates 8-phase clock signals using the voltage-controlled delay line (VCDL) and injection-locked ring oscillator (ILRO), providing wide-band and low-jitter clock signals for the data path.

To ensure the best eye-opening for the look-ahead DFE, it is necessary to minimize the delay and amplitude errors of the pseudo-differential signals generated by the S2D. The conventional inverter-based S2D suffers from delay and gain mismatch due to different signal paths for the pseudo-differential signals $V_{P,conv}$ and $V_{N,conv}$, as Fig. 2(a) indicates. Compared to the conventional S2D, the proposed passive hybrid S2D incorporates a passive hybrid resistor R_H, which feeds forward the phase-leading input signal V_{IN} to the output, as illustrated in Fig. 2(b). The output signal V_P is interpolated between V_{IN} and $V_{P,conv}$, so the delay of the output signal V_P is reduced from $2T_d$ to T_d; therefore, the delay is matched for pseudo-differential signals V_P and V_N. Simulated group delay mismatch and gain mismatch are shown at the top and bottom of Fig. 3, respectively. The results show that the proposed passive hybrid S2D reduces group delay mismatch by 85% and gain mismatch by 78% at 36 GHz. The proposed S2D also shows superior performance across PVT corners compared with conventional S2D. Combined with CTLE and VGA, the overall frequency response of the inductor-less AFE is shown in Fig. 4(a), achieving bandwidth of 12.6 GHz and trans-impedance gain ranging from 54 to 65 dBΩ, offering 11 dB tuning range. Fig. 4(b) indicates that the frequency response of the inductor-less AFE covers the optimal SNR point to achieve the best eye-opening for the system when the gain is 57 dBΩ.

Conventional direct-feedback DFE faces challenges in meeting the 1 UI feedback timing constraint at data rate above 50 GBaud [3]. To address this limitation, look-ahead DFE relaxes the timing constraint by aligning the slicer outputs before look-ahead logic. As shown in Fig. 5(a), the conventional quarter-rate look-ahead DFE employs the aligner using 4-phase quarter-rate clocks to align the 1 UI staggered output signals from the slicers, thereby extending the feedback timing of the critical path to 4 UI. However, as the data rate further increases, the quarter-rate architecture requires the DFE logic to operate at higher speeds, leading to degraded energy efficiency. Meanwhile, generating high-frequency and high-performance multi-phase clocks is also challenging for the clock path. To address the above issues in quarter-rate architecture, this work adopts octave-rate architecture with minimized hardware costs. Fig. 5(b) shows the circuit implementations of the proposed octave-rate 1-tap look-ahead DFE. The 8-way octave-rate slicers sample the AFE output signal V_{OUT} and then generate the 8-way look-ahead signals. These look-ahead signals are aligned prior to

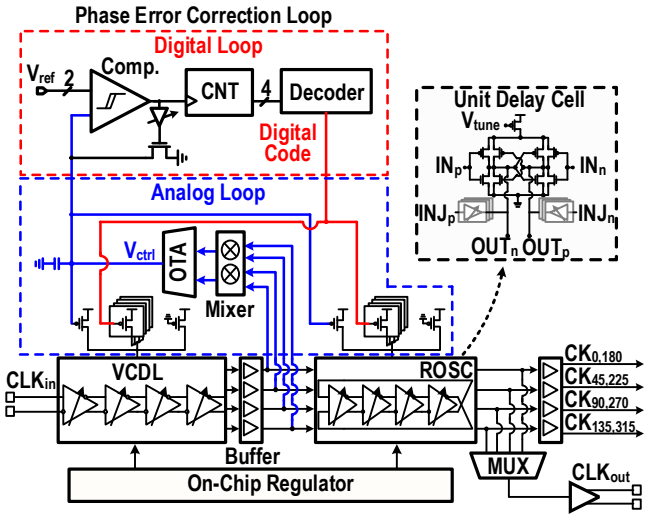

Fig. 6. Block diagram of the wideband inductor-less clock path.

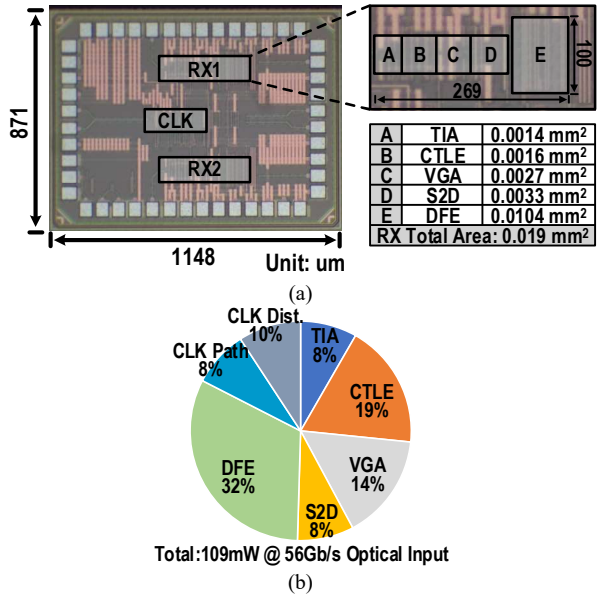

Fig. 7. (a) Chip micrograph and (b) power breakdown.

the DFE logic and finally selected by the output signal D_{OUT}<7>. Instead of using all 8-phase clocks for the aligner, the clock phase selector (SEL) is adopted to choose 4 octave-rate clocks out of the 8-phase octave-rate clocks to perform the alignment operation, reducing the hardware overhead and power consumption. Fig. 5(c) shows the curve of energy efficiency versus data rate. Considering a clock path with limited operating range from 2.5 to 10 GHz, the proposed octave-rate look-ahead DFE achieves an operation range from 20 to 72 Gb/s. Its maximum data rate is limited by the bandwidth of the data path itself. In contrast, the quarter-rate architecture operates within a range of 10 to 40 Gb/s, with its maximum speed constrained by the clock path. This architectural difference results in a 1.8× improvement in the maximum achievable data rate for the octave-rate design.

Fig. 6 shows the detailed clock path design. Since octave-rate architecture requires 8-phase clocks, the generation and calibration of the 8-phase clocks are the key challenge. The clock path adopts multi-stage VCDL to generate 8-phase clocks and inject them into the ILRO to correct phase error and perform jitter filtering. Both VCDL and ILRO share the same unit delay cell and have 5-bit fine and 1-bit coarse frequency tuning switches to cover a wide frequency band.

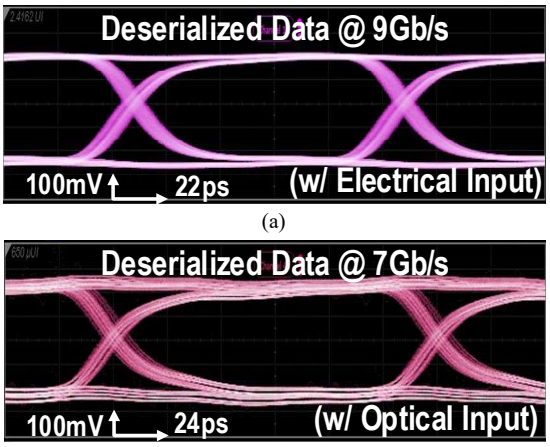

Fig. 8. (a) Measured deserialized data with 72 Gb/s electrical input; (b) measured deserialized data with 56 Gb/s optical input.

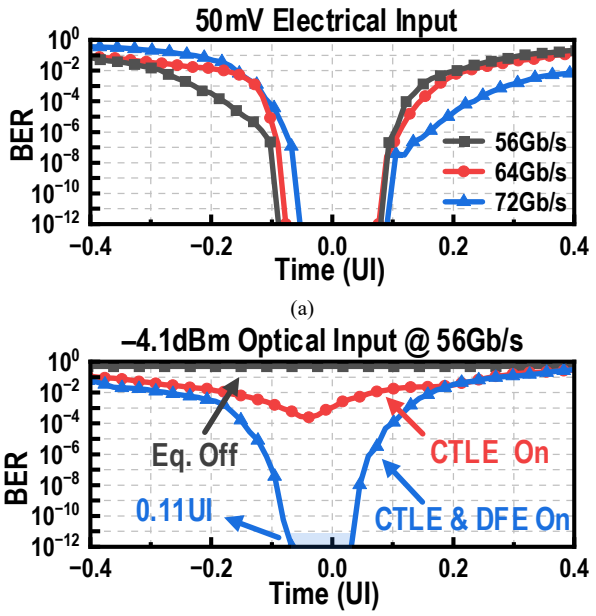

Fig. 9. (a) Measured electrical bathtub curve; (b) measured optical bathtub curve.

The phase error correction loop consists of a digital frequency tracking loop and an analog phase error detection loop to guarantee that the natural frequency of VCDL and ILRO matches the input clock frequency. Thus, it provides high-performance 8-phase clocks with minimized phase error and jitter. The clock path is capable of working from 2.5 to 10 GHz, which is able to support wide-band operation for the octave-rate RX.

III. Measurement Results

The optical RX is fabricated in 28-nm CMOS as shown in Fig. 7(a). The optical RX realizes a compact active area of 0.019 mm^2 with a vertical dimension of 100 um, making it possible to place a large number of channels within the limited area, thus enhancing the bandwidth density. The power breakdown of optical RX is shown in Fig. 7(b), which consumes 109 mW at 56 Gb/s optical input, achieving 1.9 pJ/b energy efficiency (output stages excluded). The RX is verified by both electrical and optical measurements. Fig. 8(a) shows the measured 9 Gb/s deserialized data signal with 72 Gb/s electrical input and Fig. 8(b) shows the measured 7 Gb/s

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH RECENTLY PUBLISHED OPTICAL RXS

	FinFET Process			Planar Process		
	JSSC'20[4]	ISSCC'23[2]	VLSI'24[5]	JSSC'22[3]	RFIC'23[10]	This work
Process	16nm	7nm	22nm	28nm	28nm	28nm
Data Rate (GBaud)	50	50	40-50	50-56	42.7	Optical: 20-56 / Electrical: 20-72
Operation Range (GBaud)	NA	NA	10	6	NA	36 / 52
Energy Efficiency (pJ/b)	1.7	0.96	1.5	3.9	3.4	1.9 / 1.7
Inductor-less Design	No	No	No	No	No	Yes
Clock Rate	1/4 (12.5GHz)	1/4 (12.5GHz)	1/4 (10-12.5GHz)	1/4 (12.5-14GHz)	1/4 (10-12.5GHz)	1/8 (2.5-10GHz)
RX Equalization	Inductor-Based CTLE	Passive Inductor	Inductor-Based CTLE + 2-tap FFE	Passive Inductor + 2-tap FFE + 2-tap DFE	Passive Inductor + CTLE	Inductor-less CTLE + 1-tap DFE
PD Cap. (fF)	90	60	100	70	NA	68
PD Responsivity (A/W)	1	0.96	0.48	1	0.8	0.7
Optical Sensitivity* (dBm) @ BER 1e-12	NA	–11.4	–6	–11.1	–3.6	–4.1
RX Area** (mm^2)	0.27	0.031	0.32	0.45	0.043	0.019
FoM***	2179	33602	2083	570	6840	27700

*Measured at the highest NRZ data rate. **Clock path area is excluded. ***FoM = Data Rate [Gb/s] / (Power [W] • Area [mm^2]).

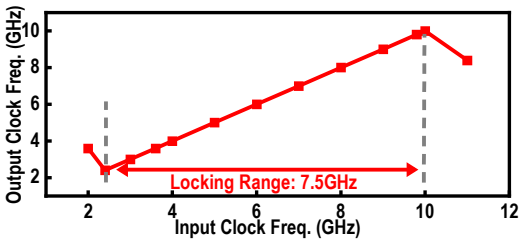

Fig. 10. Measured clock path operation range.

deserialized data signal with 56 Gb/s optical input. These deserialized output signals are fed to the error detector for the BER measurements. Fig. 9(a) shows the measured electrical BER bathtub curves at multiple data rates. The optical RX achieves 0.19 UI eye-opening at 56 Gb/s, 0.16 UI eye-opening at 64 Gb/s, and 0.14 UI eye-opening at 72 Gb/s for 1e-12 BER. Moreover, the RX is validated using an optical reference transmitter with an extinction ratio of 3.1 dB and a limited electro-optical modulation bandwidth of 22 GHz. Higher optical data rate is expected with better optical transmitter equipment. Fig. 9(b) shows the BER measurement results at 56 Gb/s. When all the equalization is turned off, the BER is about 5e-1. With CTLE enabled, the BER improves to approximately 3e-4. When DFE is further enabled, a BER of 1e-12 is achieved, with an error-free margin of 0.11 UI. The optical RX's sensitivity is –8.5 dBm at 20 Gb/s and –4.1 dBm at 56 Gb/s. Fig. 10 shows that the measured output clock successfully tracks the input clock frequency from 2.5 to 10 GHz.

Table I compares this work with other recently published optical RXs. Thanks to the octave-rate architecture and the inductor-less design, the proposed optical RX supports wideband operation from 20 to 56 Gb/s (optical) and 20 to 72 Gb/s (electrical), achieving the minimum RX area and the highest FoM using the planar process, which compares favorably with the state-of-the-art.

IV. CONCLUSION

This paper reports an inductor-less optical RX with an octave-rate look ahead DFE, achieving wideband operation ranges from 20 to 56 Gb/s (optical) and 20 to 72 Gb/s (electrical). To improve the signal integrity, the proposed passive hybrid S2D suppresses the group delay and gain mismatch by 85% and 78%, respectively. The optical RX achieves a compact area of 0.019 mm^2 using 28-nm CMOS technology, demonstrating its potential application for high-speed and high-bandwidth density optical interconnects.

ACKNOWLEDGMENT

This work was supported in part by the NKRDP under Grant 2024YFB2807602, in part by the SSTMP under Grant 20231023100159002 and Grant 20240903100208012, and in part by Grant HC-CN-ZXIC20240528002.

REFERENCES

[1] M. Wade et al., "Monolithic Microring-based WDM Optical I/O for Heterogeneous Computing," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2021, pp. 1–2.

[2] M. Raj et al., "A 0.96pJ/b 7 × 50Gb/s-per-Fiber WDM Receiver with Stacked 7nm CMOS and 45nm Silicon Photonic Dies," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 11–13.

[3] H. Li, C. -M. Hsu, J. Sharma, J. Jaussi and G. Balamurugan, "A 100-Gb/s PAM-4 Optical Receiver With 2-Tap FFE and 2-Tap Direct-Feedback DFE in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 44–53, Jan. 2022.

[4] M. Raj et al., "Design of a 50-Gb/s Hybrid Integrated Si-Photonic Optical Link in 16-nm FinFET," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1086–1095, Apr. 2020.

[5] S. Krishnamurthy et al., "A 4×50Gb/s NRZ 1.5pJ/b Co-Packaged and Fiber-Terminated 4-Channel Optical RX," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2024, pp. 1–2.

[6] H. Morita et al., "8.2 A 12×5 two-dimensional optical I/O array for 600Gb/s chip-to-chip interconnect in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 140–141.

[7] M. Moayedi Pour Fard et al., "1.23-pJ/bit 25-Gb/s Inductor-Less Optical Receiver With Low-Voltage Silicon Photodetector," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1793–1805, Jun. 2018.

[8] M. G. Ahmed et al., "A 12-Gb/s -16.8-dBm OMA Sensitivity 23-mW Optical Receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 445–457, Feb. 2018.

[9] J. E. Proesel et al., "A 32 Gb/s, 4.7 pJ/bit Optical Link With −11.7 dBm Sensitivity in 14-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1214–1226, Apr. 2018.

[10] H. Kang et al., "A 42.7Gb/s Optical Receiver with Digital CDR in 28nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Feb. 2023, pp. 9–12.