A 100Gb/s 1.32pJ/b PAM4 Optical Receiver with Digital CDR in 28nm CMOS

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***Abstract*—This paper presents a PAM4 broadband optical receiver (RX) with an LC-oscillator based quarter-rate digital clock and data recovery (CDR). A transimpedance amplifier (TIA) with sub-Nyquist bandwidth is designed for low input-referred noise and followed by an inverter-based continuous-time linear equalizer (CTLE) and variable-gain amplifier (VGA) stages for bandwidth recovery. Implemented in 28nm CMOS process and co-packaged with a commerical photodetector (PD) via wirebonding, the proposed RX achieves 100Gb/s PAM4 operation with -6.4dBm sensitivity at 1.4 × 10^{-4} BER and 1.32pJ/bit energy efficiency.**

***Index Terms*—Clock and data recovery (CDR), optical RX, PAM4, quarter-rate, receiver, silicon photonics.**

I. Introduction

The increasing demand for AI, big data analytics, and edge computing has led to the rapid growth of data centers and computing systems. As these technologies evolve, the need for high-speed, low-latency, and energy-efficient data transmission has been continuously growing. In this context, optical communication systems and interconnects have become essential as they enable scalable, high-bandwidth, and low-power data transfer across vast distances. Fig. 1(a) shows an example of a conventional optical receiver module, which consists of a discrete photodetector, an analog front-end (AFE) in BiCMOS process, and a clock and data recovery (CDR) and host SERDES designed in CMOS. While designing the AFE in BiCMOS offers several advantages, such as low noise and wide bandwidth, CDR and SERDES host are typically implemented in CMOS due to its superior power efficiency, scalability, and lower cost. However, this heterogeneous integration of an AFE in BiCMOS with subsequent circuitry in CMOS increases the number of electrical interfaces and overall cost, becoming more challenging as data rates continue to rise rapidly.

To address the challenges of heterogeneous integration, several attempts have been made to implement the AFE in CMOS [1]– [3] along with the CDR and host SERDES, as shown in Fig. 1. To overcome inherent higher noise characteristics of CMOS, direct feedback DFE (DF-DFE) and lookahead DFE are employed in [1] and [2] to improve OMA sensitivity by mitigating residual inter-symbol interference (ISI) penalties. However, DFE also increases hardware complexity and power consumption, as it requires a current-integrating summer (DF-DFE) or additional samplers (lookahead DFE).

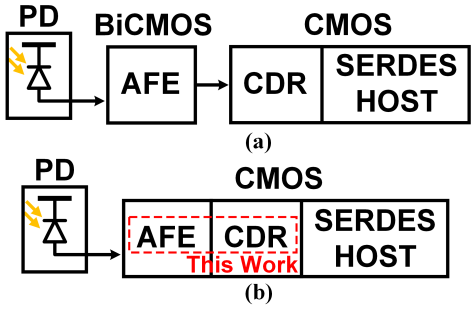


Fig. 1. (a) Conventional optical RX block diagram and (b) proposed optical RX block diagram.

Clocking architecture is a crucial component of optical links. While some previous studies [3] have used an external clock without implementing CDR, this approach requires careful phase control between the incoming data and the clock, which becomes even more challenging as data rates continue to increase. Although phase interpolator (PI)-based CDR can be a viable solution [4], it also requires external clock distribution networks, leading to increased power consumption and hardware complexity.

This work presents a PAM4 optical receiver (ORX) with digital CDR. A power-efficient inverter-based continuous-time linear equalizer (CTLE) is implemented for receiver equalization. An LC-oscillator-based digital CDR generates a quadrature clock for the PAM4 slicers, eliminating the need for an external clock signal. Measurement results demonstrate that the CTLE improves RX power efficiency while maintaining OMA sensitivity comparable to that of DFE techniques.

II. Receiver Architeture

Fig. 2 shows the block diagram of the proposed PAM4 ORX. A discrete commercial PD is integrated with the CMOS RX through wire-bond. Two main building blocks of the CMOS RX are AFE and CDR. AFE consists of transimpedance amplifier (TIA), CTLE, variable gain amplifier (VGA), and DC offset cancellation (DCOC). At the AFE output, quarter-rate PAM4 samplers and PLL-based CDR follow. The quarter-rate PAM4 samplers consist of twelve data samplers for PAM4 symbol detection and four edge samplers for 2× over-sampling CDR architecture. The outputs of the samplers are deserialized by demultiplexers (DMUX)

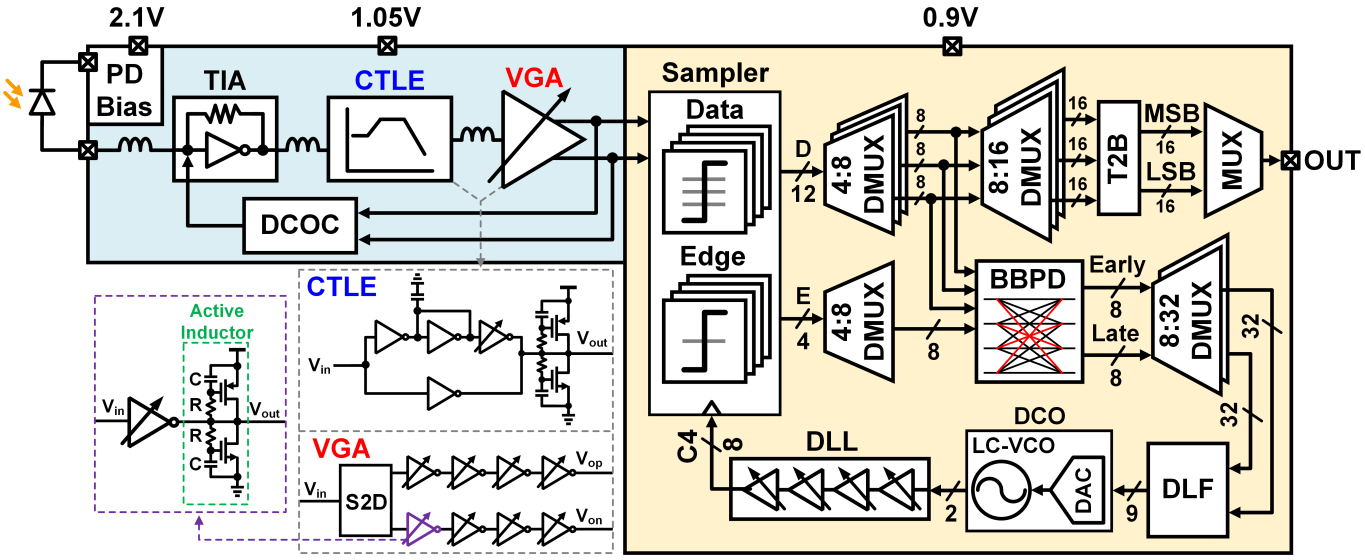


Fig. 2. Proposed optical RX block diagram. Insets show the schematics for the active inductor, CTLE and VGA stages.

and are either probed out for BER measurement (MSB/LSB) or fed into bang-bang phase detector (BBPD) to generate phase information (early/late) for the digital loop filter (DLF) to drive the LC-DCO. Since LC-DCO generates differential clock signals at quarter rate, delay-locked loop (DLL) is implemented for the generation of 8-phase clock signals that the samplers require. With RX equalization implemented in the AFE using CTLE, CDR achieves power efficient operation by not having FFE/DFE, which will be demonstrated by power consumption measurement in section V.

III. Analog Front-end Design

The block diagram of the AFE and schematic of the CTLE and VGA are shown in Fig. 2. The PD is wire-bonded to the CMOS RX, and its photocurrent is fed into the TIA that converts and amplifies the current into a voltage signal. The average photocurrent is subtracted by the DCOC to maximize the dynamic range of the AFE for a given supply voltage. A low-bandwidth TIA is designed to improve the input-referred noise of the AFE by having larger feedback resistance as TIA is usually a key factor in determining the RX sensitivity. However, low-bandwidth design exacerbates the residual ISI, requiring an equalization technique to prevent this ISI penalty from degrading RX sensitivity. This work utilizes CTLE since it enables power efficient operation while also minimizing the hardware overhead compared to FFE/DFE techniques in [1], [2]. Moreover, meeting the feedback latency required in DFE technique becomes increasingly challenging as data rates continue to rise. The CTLE compensates for the reduced TIA bandwidth by employing an adjustable peaking mechanism (Fig. 3(a)). An inverter-based VGA then amplifies the signal to a level suitable for the subsequent PAM4 slicers. Both CTLE and VGA incorporate the active inductors, as shown in Fig. 2, which provide frequency peaking and achieve bandwidth extension. Between the main building blocks of the AFE,

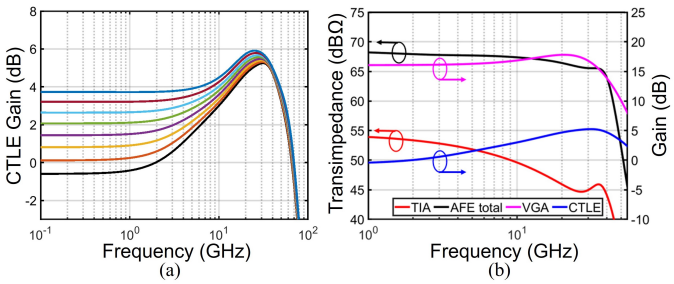


Fig. 3. Simulated frequency response of (a) CTLE and (b) overall AFE.

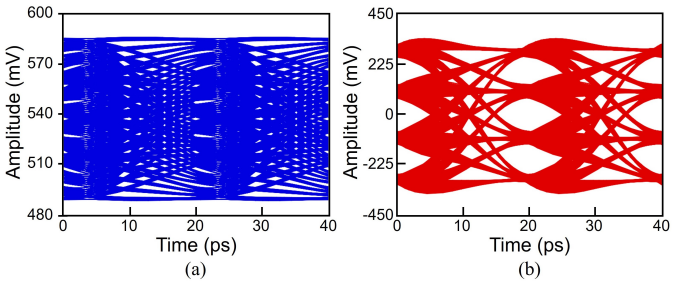


Fig. 4. Simulated 100Gb/s PAM4 eye diagrams at the (a) TIA output and (b) AFE output.

series passive inductors are also added to further extend the AFE bandwidth along with the active inductors.

The overall AFE frequency response is illustrated in Fig. 3(b), showing a 3-dB bandwidth of approximately 38 GHz, while the TIA bandwidth is only around 7 GHz. Fig. 4 compares layout-extracted simulated 100Gb/s PAM4 eye diagrams measured at the TIA and AFE outputs. Due to the sub-Nyquist bandwidth design, the TIA produces a closed eye diagram (Fig. 4(a)). However, the following CTLE and VGA stages provide equalization, opening the eye diagram as shown in Fig. 4(b).

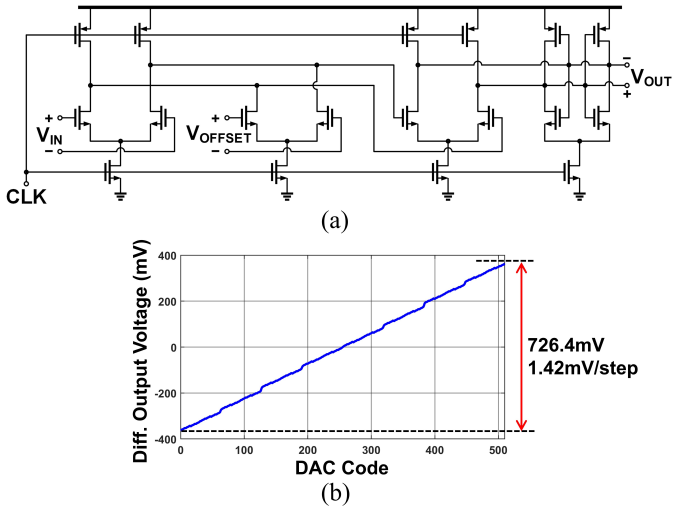


Fig. 5. (a) Schematic of the PAM4 sampler unit. (b) Simulated differential output voltage of the DAC for sampler offset/ PAM4 threshold control.

IV. PAM4 PLL-BASED CDR

At the output of the AFE, quarter-rate PAM4 samplers are implemented, as shown in Fig. 2. A schematic of the sampler is shown in Fig. 5(a). The proposed sampler, designed with a two-stage dynamic amplifier in parallel with the regeneration stage, operates with a single clock phase and achieves no static power consumption, short aperture time, and CMOS-level outputs [5]. For offset correction/threshold control, an additional differential stage is connected in parallel to the first stage, controlled by the two 8-bit DACs in a differential manner. The DAC generates differential output voltage over a ±363mV range (Fig. 5(b)), which is wide enough for a nominal threshold control requirement of ±225mV based on simulated eye-diagrams in Fig. 4(b). The outputs of the samplers are time-aligned and further deserialized to either 1/16 (data) or 1/32 (BBPD output) symbol rate by the subsequent DMUXs. For the external BER measurement, thermos-to-binary (T2B) encoders are implemented and then either MSB or LSB bit is probed out.

A PLL-based digital CDR consists of a BBPD, DLF, LC-DCO, and DLL. A BBPD receives all the data and edge bits at 1/8 symbol rate to generate early/late decision only for the symmetric transitions, as highlighted in red in Fig. 2, to avoid asymmetric transition pattern induced jitter. A DLF processes the BBPD output and digitally controls the subsequent DCO, achieving better power and area efficiency as well as robustness to PVT variations compared to analog CDR, primarily by not having a power-hungry charge pump and passive RC filter. The DLF has programmability of the proportional gain (K_p) and integral gain (K_i). The LC-DCO generates differential clocks at quarter-rate. An LC oscillator is chosen for its lower phase noise and reduced power consumption compared to ring oscillators. The LC-DCO incorporates a 9-bit DAC for conversion of the DLF's digital output into an analog voltage, which in turn drives a varactor. To achieve a linear frequency tuning characteristic, the DAC and varactor are co-optimized

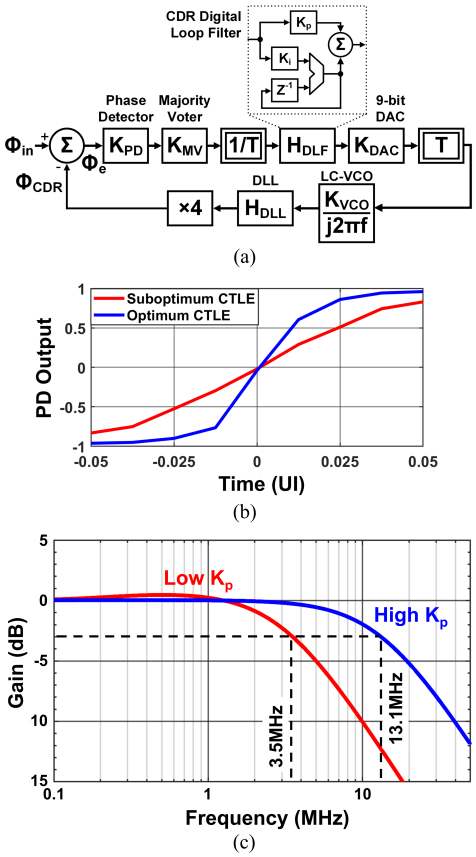


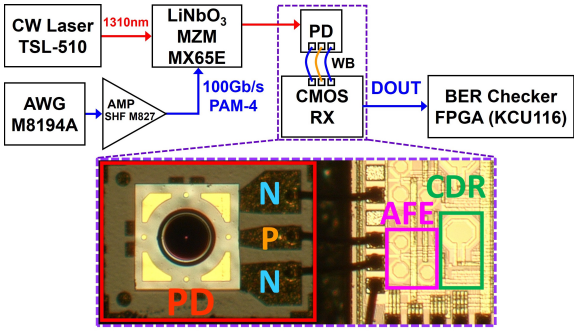
Fig. 6. (a) Linearized CDR phase model. (b) Simulated BBPD transfer function after majority voter. (c) Simulated jitter transfer function of the CDR.

such that resulting frequency curve is linear with respect to the DAC input code. Following the DCO, a DLL generates eight-phase clocks required for the 2× oversampling architecture. The DLL consists of inverter-based delay cells with tunable delays and a negative feedback loop that includes a quadrature phase detector and an operational transconductance amplifier to ensure equal eight-phase spacing. Since the DLL's negative feedback loop is embedded within the CDR loop, the DLL loop bandwidth is set significantly higher than that of the CDR to prevent interference with the CDR loop dynamics.

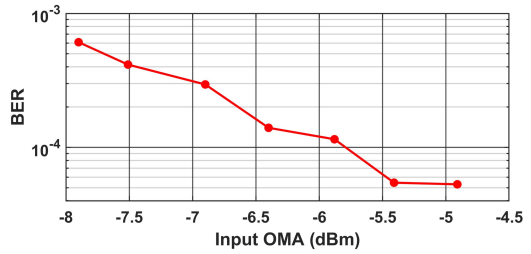
A linearized phase domain model of the CDR is given in Fig. 6(a), and the BBPD transfer function after the majority voter is presented in Fig. 6(b). As CTLE setting deviates from the optimum, increased ISI at the AFE output leads to a reduction in BBPD gain. Based on the phase domain model and BBPD gain obtained, overall CDR transfer function curve is plotted in Fig. 6(c) for different K_p values. Fig. 6(c) demonstrates that the programmability of the DLF enables optimization of the CDR loop bandwidth and stability.

V. EXPERIMENTAL RESULTS

Fig. 7(a) shows the optical test setup, consisting of an O-band laser source, a high-speed $LiNbO_3$ MZM, a Keysight M8194A arbitrary waveform generator (AWG) generating the 100Gb/s PAM4 pattern, and an FPGA performing BER testing on the demultiplexed outputs at 1/16 symbol rate. A



(a)



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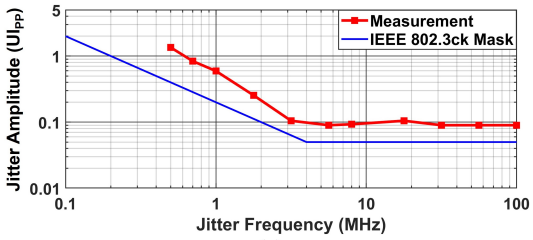
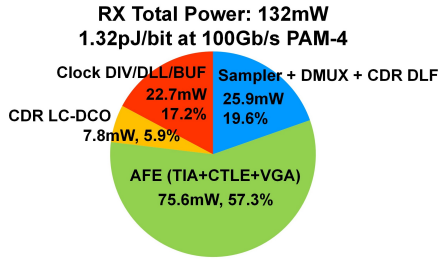


(c)



(d)

Fig. 7. (a) Measurement setup for the hybrid-integrated PAM4 RX. Inset shows the micrograph image of the hybrid integration. (b) Measured input OMA sensitivity at 100Gb/s PAM4. (c) Jitter tolerance measurement at 100Gb/s PAM4. (d) RX power breakdown at 100Gb/s PAM4.

commercial PD and CMOS RX, fabricated in a 28nm process, are wire-bonded and mounted on a PCB (Fig. 7(a)). The PD cathode is biased through the CMOS RX, which helps to reduce noise thanks to decoupling capacitors and minimize wire-bond inductance. The extinction ratio (ER) of the optical signal coupled to the PD was measured to be 3.68 dB. Fig. 7(b) presents the measured BER curves across different input OMA with 100Gb/s PAM4 PRBS15 inputs. The measured sensitivity was -6.4 dBm with the BER of 1.4×10^{-4}. Fig. 7(c) is jitter tolerance measurement, with the input OMA of -5.4 dBm and target BER of 1.4×10^{-4}. It shows that the CDR bandwidth is around 4 MHz with 0.09 UI high-frequency JTOL, satisfying the IEEE 802.3ck mask. Due to the equipment jitter generation limit, JTOL curve below 500 kHz cannot be measured. The power consumption of the RX is 1.32 pJ/bit at 100Gb/s PAM4. As shown in Fig. 7(d) the majority of the power is consumed in the AFE. Compared to [1], CTLE-based RX equalization and on-chip CDR enable significant power saving by eliminating FFE/DFE and external clock distribution network. Table I compares this work with state-of-the-art slicer-based ORXs, demonstrating the best energy efficiency at the highest data rate.

TABLE I. OPTICAL RECEIVER PERFORMANCE COMPARISON

	ISSCC'20 [6]	JSSC'18 [4]	JSSC'22 [1]	This Work
Technology	55nm BiCMOS	14nm FinFET	28nm CMOS	28nm CMOS
Data Rate (Gb/s)	53.125	60	100	100
Modulation	PAM-4	PAM-2	PAM-4	PAM-4
On-Chip CDR?	Yes	Yes	No	Yes
OMA Sensitivity (dBm)	-9.5	-8.2*	-8.9	-6.4
BER	2.4×10^{-4}	1×10^{-12}	2.4×10^{-4}	1.4×10^{-4}
PD Responsivity (A/W)	0.945	0.52*	1	0.65
RX Equalization	N/A	Lookahead DFE	FFE + DFE	CTLE
RX Energy Eff. (pJ/bit)	4.4	1.9	3.9	1.32

* Estimated from [2]

VI. CONCLUSION

This paper presented a CMOS RX hybrid-integrated with a photodetector, featuring an energy-efficient inverter-based AFE and a digital CDR. An LC oscillator generates quarter-rate clocks, eliminating the need for external clock source and distribution network. The RX achieves an OMA sensitivity of -6.4 dBm at 100Gb/s PAM4 operation and energy efficiency of 1.32pJ/bit. To the best of our knowledge, this work achieves the best energy efficiency among slicer-based optical RX.

ACKNOWLEDGMENT

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