A Buck-Boost Photovoltaic Energy Harvester Employing Adaptive Power-Scalable MPPT Control Achieving >98% MPPT Efficiency and >82% Power Conversion Efficiency Across a 100,000× Dynamic Range

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***Abstract*—This paper presents a photovoltaic energy harvesting (PVEH) system achieving both high Maximum Power Point Tracking (MPPT) efficiency (η_{MPPT}) and power conversion efficiency (η_{CONV}) across a wide input power dynamic range (DR), employing a direct input power-to-digital converter (PDC) and an adaptive power-scalable MPPT scheme. The proposed PVEH achieves >98% (with a peak of 99.9%) η_{MPPT} across a 100,000× DR (10μW to 1W), representing a 10× improvement over the state-of-the-art, as well as a competitive η_{CONV} of >82% (with a peak of 92%) across the same DR.**

I. Introduction

PVEH is widely used for outdoor IoT applications. To maximally extract the energy from the PV cells, achieving both high η_{MPPT} and high η_{CONV} across a wide DR is crucial.

Some PVEHs employ Fractional Open-Circuit Voltage (FOCV) MPPT method for simplicity [1] [2]. However, FOCV interrupts the energy harvesting process and requires a look-up table (LUT) to calculate the MPPT voltage $\mathrm{V_{MPP}}$. Perturb and Observe (P&O) is another widely used MPPT method. However, it requires the measurement of the input power, and previous methods such as pulse-integration power detectors [1], analog multipliers followed by analog-to-digital converters (ADCs) [3], and pulse-based multipliers [4] either consume excessive power that degrades η_{CONV} in low-irradiation (LI) conditions; or only offer a high η_{MPPT} over a limited DR.

Expanding DR while maintaining high efficiency presents significant challenges due to inherent trade-offs in PVEH systems. While voltage and current sensing circuits enhance MPPT accuracy, they also introduce additional circuit complexity and power overhead. High-precision MPPT techniques with sufficient tracking speeds are essential, as implemented in [4], [5], they improve the tracking accuracy at specific input power ($\mathrm{P_{in}}$) but introduce energy overhead at lower $\mathrm{P_{in}}$, limiting the DR for >85% η_{CONV} to only ~6×. Moreover, as $\mathrm{P_{in}}$ increases, the limited bandwidth of MPPT further constrains the DR for >98% η_{MPPT} to only 9× and 5×. Many studies have explored minimizing the power consumption of MPPT controller by using LUTs [1], [2], [6]. Notably, [2] achieves an impressive 1,000× DR for >85% η_{CONV} and 10,000× DR for >98% η_{MPPT}. However, LUT-based approaches are sensitive to environmental and PVT variations. These trade-offs make it inherently difficult to develop a PVEH system that is both highly efficient and robust across a wide DR.

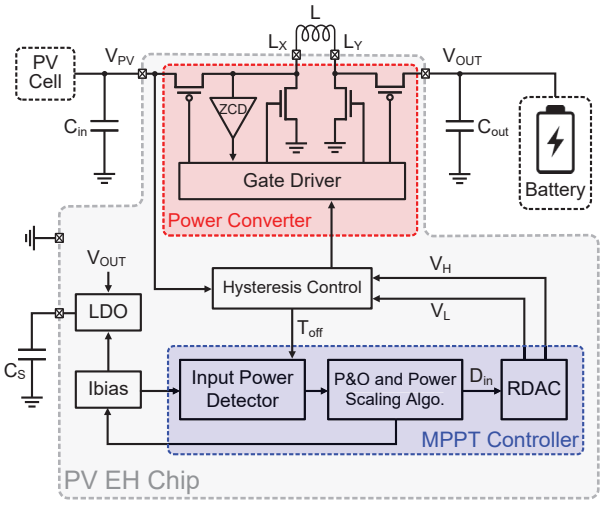


Fig. 1. Overall architecture of the proposed PVEH with adaptive power-scalable MPPT controller.

To address these challenges and achieve a wide input DR of PVEH, this work proposes a power-scalable MPPT scheme that employs a direct PDC-based P&O MPPT without the need for voltage/current sensing circuits, multipliers, LUTs, or ADCs. To achieve both high η_{MPPT} and η_{CONV}, the power of the MPPT circuit is automatically scaled with respect to $\mathrm{P_{in}}$ while maintaining the proper accuracy and speed required in both LI and high-irradiation (HI) conditions.

II. Proposed PVEH System

A. System Design

As shown in Fig. 1, the proposed PVEH system consists of a buck-boost converter, a hysteresis controller, an MPPT controller, an LDO, and a bias generator. The MPPT controller consists of a PDC, a P&O and power scaling algorithm, and an RDAC. The buck-boost converter operates in discontinuous conduction mode (DCM), facilitated by a zero current detection (ZCD) circuit, and adapts a pulse frequency modulation (PFM) technique with input hysteresis control that regulates the photovoltaic voltage $\mathrm{V_{PV}}$ within a hysteresis window ($\mathrm{V_H}$ and $\mathrm{V_L}$). The MPPT controller compares the input power in two adjacent cycles, during which two $\mathrm{V_{PV}}$s are chosen. Based

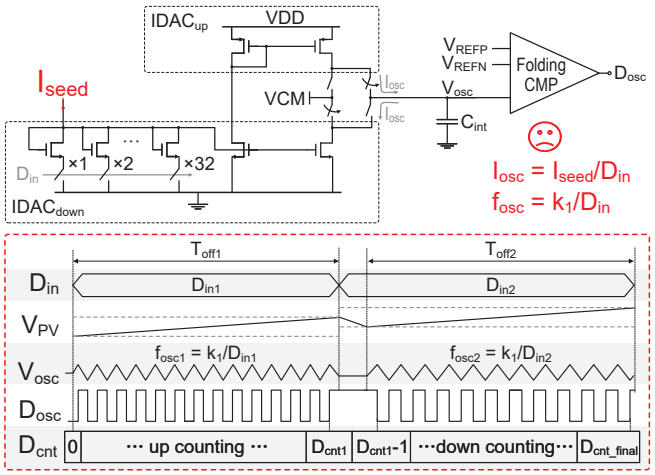


Fig. 2. The working principle of the proposed PDC; DCO with a current divider IDAC.

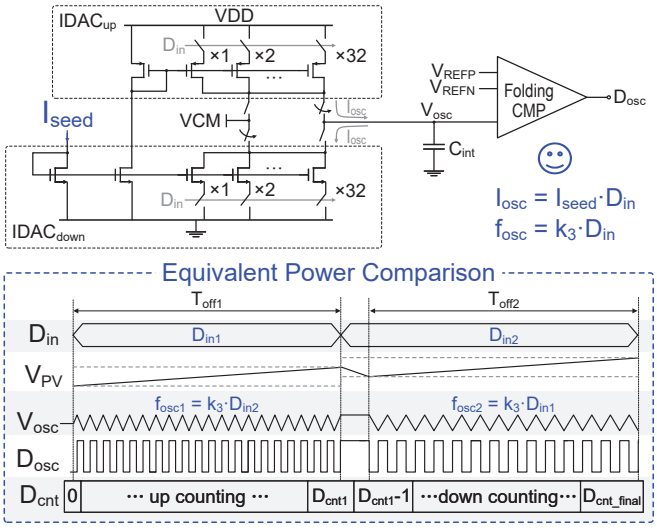


Fig. 3. Proposed PDC with the equivalent power comparison technique.

on the result, the MPPT controller adjusts V_H/V_L around a new V_{PV} by changing RDAC code D_{in}, which is then fed to the hysteresis controller.

B. Power-to-Digital Converter

As illustrated in Fig. 2, the PDC consists of an integration capacitor Cint, two current DACs $IDAC_{up}$ and $IDAC_{down}$, and a folding comparator that compares V_{osc} to $V_{REFP,N}$ generated by RDAC. The oscillation frequency f_{osc} is determined by the digital code of $IDAC_{up/down}$.

During the off-time (T_{off}) of the buck-boost converter, the inductor is disconnected from the PV cell, and the input capacitor C_{in} gets charged. T_{off} is given by

$$T_{off} = V_{HYS} \cdot C_{in}/I_{PV} \tag{1}$$

where $V_{HYS} = V_H - V_L$, and I_{PV} is the average input current from the PV cell during T_{off}.

Since V_{PV} is known as D_{in}, it can be used to control $IDAC_{up/down}$, so that f_{osc} is proportional to $k_1/D_{in} = k_2/V_{PV}$, where k_1 and k_2 are constants. Define D_{cnt} as the number of oscillations within one T_{off}, which is given by

$$\begin{aligned} D_{cnt} &= T_{off} \cdot k_2/V_{PV} = V_{HYS} \cdot C_{in} \cdot k_2/(I_{PV} \cdot V_{PV}) \\ &= V_{HYS} \cdot C_{in} \cdot k_2/P_{in} \end{aligned} \tag{2}$$

thus, D_{cnt} is directly inversely proportional to P_{in}.

To obtain V_{MPP}, P_{in} is measured during $T_{off1,2}$ with $V_{PV1,2}$ and $D_{in1,2}$ and then compared in the digital domain by an up/down counter. A net positive count means the power P_{in} is higher during T_{off2} and vice versa. However, the above-mentioned IDACup/down is power consuming since I_{osc} is inversely proportional to D_{in} (Fig. 2) and so is generated by dividing a large seed current I_{seed}, which consumes excessive power in LI conditions.

To reduce I_{seed}, an equivalent power comparison technique is proposed. As shown in Fig. 3, instead of setting f_{osc} to k_1/D_{in}, it is set to $k_3 \cdot D_{in2}$ during T_{off1} and set to $k_3 \cdot D_{in1}$ during T_{off2}. This is feasible since at the beginning of a new comparison cycle, $D_{in1,2}$ and $V_{PV1,2}$ are known based on the power comparison result from the previous cycle. From Fig. 3, D_{cnt_final} is given by

$$\begin{aligned} D_{cnt\_final} &= D_{cnt1} - D_{cnt2} \\ &= k_3 \cdot D_{in2} \cdot T_{off1} - k_3 \cdot D_{in1} \cdot T_{off2} \\ &= \alpha \cdot (V_{PV2}/I_{PV1} - V_{PV1}/I_{PV2}) \end{aligned} \tag{3}$$

where α is constant. The polarity of (3) is equivalent to the polarity of $\beta \cdot (V_{PV2} \cdot I_{PV2} - V_{PV1} \cdot I_{PV1})$, where β is constant. Therefore, (3) represents the same power comparison result. The equivalent power comparison technique effectively reduces the PDC's power consumption by ~30×.

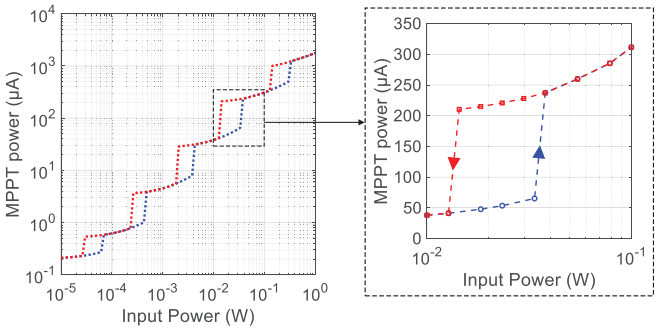


Fig. 4. Simulated MPPT power vs. input power.

C. Power-Scalable MPPT

To obtain high η_{CONV} over a 100,000× DR, where the system switching frequency (f_{sw}) varies between 10Hz and 600kHz from LI to HI, the power of MPPT circuits must be scaled. In LI conditions, its power consumption must be minimized for high η_{CONV}, while in HI conditions, the speed and noise of some blocks, e.g., the comparators, become crucial to achieve high η_{MPPT}, demanding increasing power.

Thanks to the PDC, such power scaling can be done autonomously, and the entire DR has been divided into six power regions logarithmically to ensure optimal η_{CONV} and

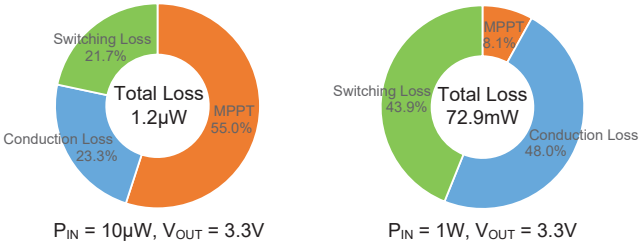


Fig. 5. Simulated power consumption of the power-scalable MPPT circuit vs. input power.

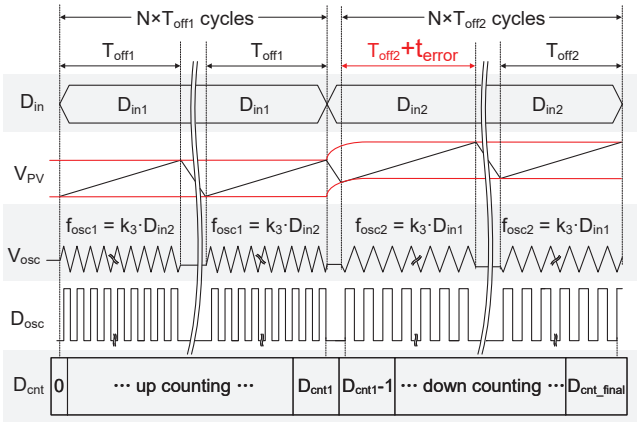


Fig. 6. Proposed multiple counting technique.

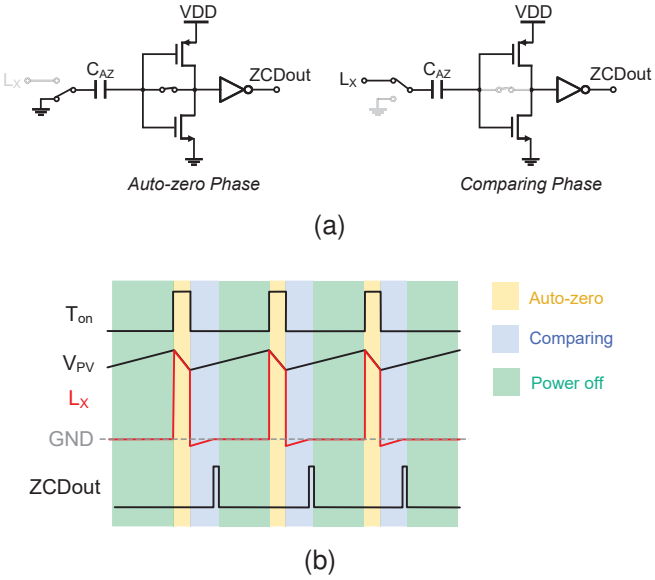
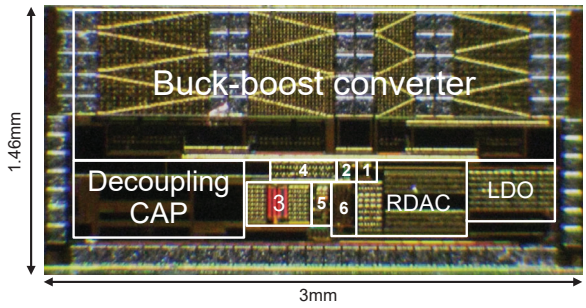


Fig. 7. Auto-zero inverter-based ZCD, (a) simplified schematic, and (b) timing diagram.

η_{MPPT} in each region. According to D_{cnt1} from the previous comparison cycle, the bias current of most MPPT circuitry automatically scales in the next comparison cycle.

Fig. 4 shows the simulated power consumption of the power-scalable MPPT circuit vs. P_{in}, where hysteresis is applied to prevent a dead loop due to circuit settling errors



1. ZCD
2. Hysteresis control
3. DCO
4. Input voltage divider
5. Ibias generator
6. Synthesized digital block (MPPT algorithm)

Fig. 8. Die micrograph.

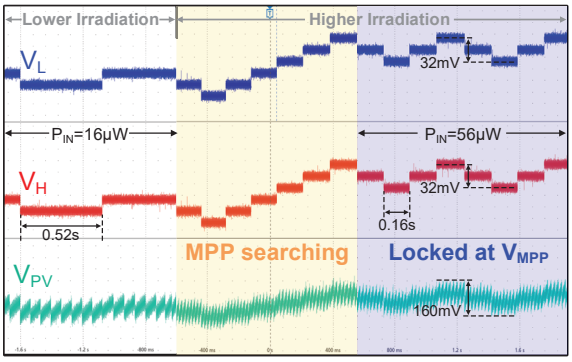


Fig. 9. Measured transient waveform with irradiation changing.

during bias current switching.

Naturally, the power of dynamic blocks such as comparators also increases as f_{sw} within each power region. Fig. 5 shows that MPPT power dominates the system power loss at low P_{in} and increases considerably but stays negligible at high P_{in}.

To achieve >98% η_{MPPT}, the $IDAC_{up/down}$ is implemented as 6-bit to minimize quantization errors. This is complemented by a 6-bit RDAC that sets the hysteresis window. To accommodate the hysteresis controller input voltage range ($\leq$1V), V_{PV} is divided by a 3:1 divider. To reduce the effect of comparator noise, 4× $T_{off1,2}$ are counted in a power comparison cycle. In HI conditions, not only the comparator noise but also the settling time associated with switching $V_{H,L}$ from one state to another becomes comparable to short T_{off}, and thus can introduce noticeable error in the T_{off} duration, as shown in Fig. 6, and hence degrade η_{MPPT}. To mitigate this, 16× $T_{off1,2}$ is used at these power levels (>0.1W).

To ensure good η_{CONV} in LI, ZCD is implemented using a duty-cycled auto-zero inverter-based comparator [7] that also minimizes offset and flicker noise (Fig. 7). It is first auto-zeroed during T_{on}, and once triggered by the voltage of L_X (Fig. 1) during T_{off}, it is automatically powered off until next T_{on}, resulting in an average power of only 8nW in the lowest irradiation condition.

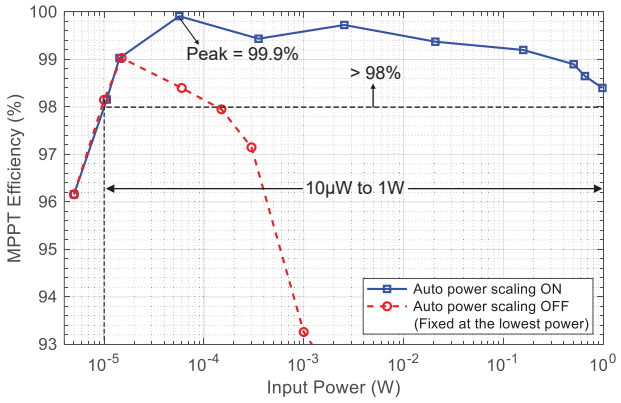


Fig. 10. Measured transient waveform with irradiation changing.

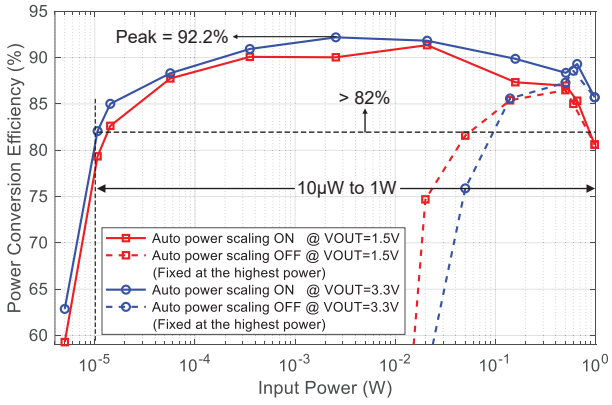


Fig. 11. Measured transient waveform with irradiation changing.

TABLE I
COMPARISON WITH STATE-OF-THE-ARTS

	[4]	[1]	[6]	[8]	[2]	[5]	This Work
Process	180nm	350nm	180nm	180nm	180nm	180nm	180nm
Power Stage	Boost	Boost	Boost	Buck-Boost	Buck-Boost	Boost	Buck-Boost
C_{IN}	–	10μF	20μF	–	10μF	10μF	10μF
L	47μF	10μH	82μH	10μH	10μH	–	10μH
MPPT Type	P&O	FOCV + P&O	P&O	P&O	FOCV	P&O	P&O
Using LUT	No	Yes	Yes	No	Yes	No	No
Continous MPPT	Yes	No	Yes	Yes	No	No	Yes
V_{IN} (V)	0.6–1.15	0.5– 2.4	0.2–1.5	0.2–1.5	1– 5.2	0.15–1.8	1–3
V_{OUT} (V)	1.2–1.8	3.5	3.3	0.6–1.8	3.5	2.2, 3	1.5–3.3
Peak η_{MPPT}	99.3%	99.9%	–	95%	99%	99.5%	99.9%
Peak η_{CONV}	94.7%	92.6%	93.6%	87%	96.5%	88%	92%
P_{IN} Range for η_{MPPT} > 98%	0.6mW–5.4mW* **(9×)**	4mW–0.9W* **(225×)**	–	N.A.	150μW–1.5W* **(10,000×)**	2mW–10mW* **(5×)**	10μW–1W **(100,000×)**
P_{IN} Range for η_{CONV} > 85%	0.85mW–5.4mW* **(6×)**	40mW–835mW* **(21×)**	0.5μW–50mW* **(100,000×)**	4mW–10mW* **(2.5×)**	1.5mW–1.5W* **(1,000×)**	9mW–50mW* **(5.6×)**	14μW–1W **(71,400×)** @V_{OUT}=3.3V

* Estimated from data/graph

III. MEASUREMENTS RESULTS

The proposed PVEH IC was fabricated in a 0.18μm CMOS (Fig. 8). Fig. 9 shows the measured waveforms of $V_{H,L}$ and V_{PV}. It can be seen that f_{sw} changes according to irradiation, and the EH begins to search and settle around a new V_{MPP}, as expected. The "oscillation" is normal and intrinsic to P&O operation.

Fig. 10 and Fig. 11 show the measured η_{MPPT} and η_{CONV} vs. input power. Across the power range from 10μW to 1W, >98% η_{MPPT} is measured with a peak of 99.9%, regardless of V_{OUT}, and >82% η_{CONV} with a peak of 92% is measured when V_{OUT}=3.3V. When the auto power-scaling algorithm is disabled and the MPPT power is fixed at the lowest level, η_{MPPT} rapidly decreases as P_{in} increases beyond ~150μW due to the low speed and high noise of the MPPT circuit. Conversely, when the MPPT power is fixed at the highest level, the high power of the MPPT circuit limits η_{CONV} when P_{in} is below 50mW. As shown in Table I, the proposed PVEH achieves 10× wider DR with >98% η_{MPPT} compared to all other state-of-the-art EHs and 444× wider DR compared to other EHs employing P&O. It also achieves a competitive >82% η_{CONV} over the same DR.

IV. CONCLUSION

This paper presents a PVEH system that achieves both high η_{MPPT} and η_{CONV} across a wide input power DR, employing a direct input PDC and an adaptive power-scalable MPPT scheme. To reduce the power consumption of PDC and mitigate the comparator noise and RDAC settling error, equivalent power comparison technique and multiple counting technique are applied. The proposed PVEH achieves >98% (with a peak of 99.9%) η_{MPPT} across a 100,000× DR (10μW to 1W), as well as a competitive η_{CONV} of >82% (with a peak of 92%) across the same DR. The wide DR makes it suitable for various outdoor IoT applications.

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