A 68.5 dB SNDR, 50 MHz Bandwidth, 800 MS/s Bandpass CT-Pipeline ADC in 65 nm CMOS

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***Abstract*—We present a continuous-time bandpass pipeline ADC that is equivalent to a sixth-order, 50 MHz bandwidth bandpass filter (center frequency 200 MHz) followed by an 800 MS/s 12 bit ADC. The converter is not only easy to drive, but also achieves a bandpass STF that cuts off sharply outside the signal band. Thanks to the open-loop nature of the architecture, much wider bandwidths are possible when compared to bandpass CT-ΔΣ converters. The prototype converter, designed in a 65 nm CMOS process, achieves a peak SNDR of 68.5 dB while consuming 75 mW from a 1.2 V supply.**

I. Introduction

Continuous-time (CT) bandpass analog-to-digital converters are useful in RF receivers as they enable radio architectures that avoid problems like flicker noise, local oscillator reradiation, and I-Q mismatch [1]–[4]. Furthermore, they simplify system design since they are easy to drive. At this time, CT-bandpass ADCs have all been realized using bandpass ΔΣ modulation. Achieving wide bandwidths in such converters has been a challenge due to complexities associated with closing the ΔΣ loop. This work presents a CT bandpass *pipeline* ADC that avoids the problem of closing a mixed-signal feedback loop, thereby enabling wideband operation. In addition, unlike in a ΔΣ modulator, the STF and NTF of a bandpass CTP can be independently designed. This enables the realization of a sharp bandpass STF.

This work presents a three-stage bandpass CTP that achieves 68.5 dB SNDR in a 50 MHz band centered at 200 MHz. Designed in a 65 nm CMOS process, it is equivalent to a sixth-order bandpass filter followed by a 12 bit ADC operating at 800 MS/s, and is the first bandpass CTP reported in the literature. The architecture and design details form the subject of the rest of this paper, which is organized as follows. Section II describes the top-level architecture. Design details of the pipeline stages are given in Section III. Section IV gives measurement results and compares our work with the state-of-the-art. Section V concludes the paper.

II. Architecture Details

Fig. 1(a) shows the block diagram of our bandpass CTP. It consists of three stages followed by an 8-bit, 4× time-interleaved SAR ADC. ADC_1-DAC_1 in stage 1, which operate at f_s, form a 17-level quantizer and create a digital approximation to $u(t)$. This coarse version of $u(t)$ is subtracted from a $u(t-t_d)$ to yield a continuous-time residue. This is filtered and amplified by a "bandpass-like" transfer function $H_f(s)H_1(s)$. Stages 2 and 3 operate similarly, except that they do not use a prefilter before the residue-amplifying

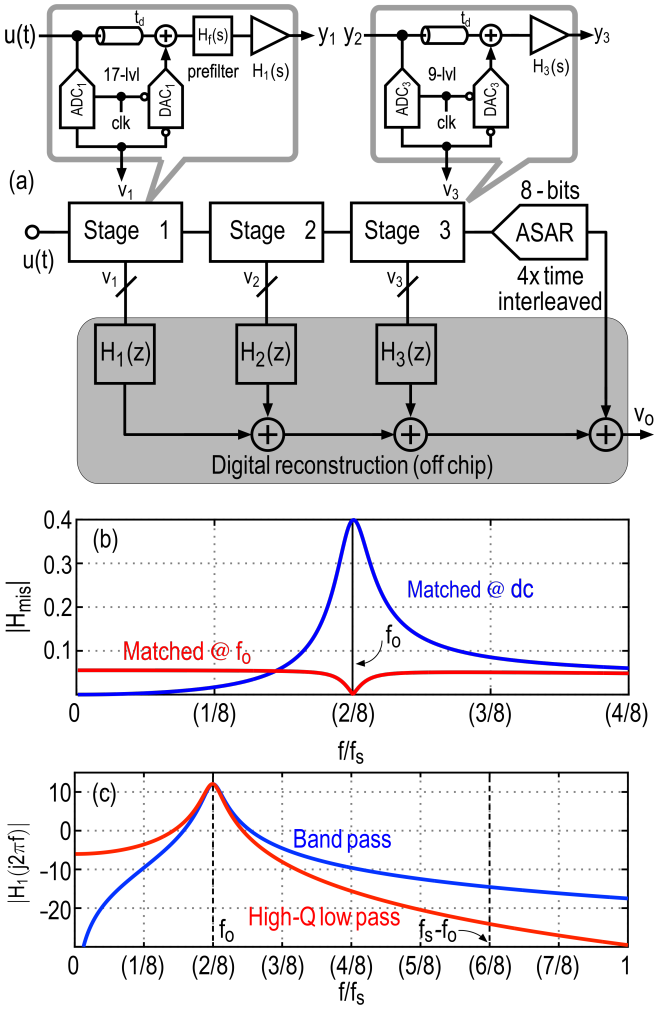


Fig. 1. (a) Three-stage bandpass CTP architecture. The call out shows the details of each stage. (b) Mismatch transfer function when gain and delay of the quantizer path and delay line are matched at dc (blue), and f_o (red). (c) $|H_1(j2\pi f)|$ for two choices of residue amplifying filter transfer function i.e. bandpass and lowpass.

filter. The sub-ADC and DAC in each stage are clocked half-cycle apart to give the ADCs enough time to make a decision. The effective magnitude response of the CTP's STF is $|H_f(s)H_1(s)H_2(s)H_3(s)|$. Since H_1, H_2, H_3 peak around the center frequency (denoted by f_o), the CTP is equivalent to a bandpass filter at f_o followed by an ADC. As in bandpass ΔΣ converters [2]–[4], f_o/f_s is chosen as 1/4 to simplify demodulation of the digitized signal.

Unlike in a lowpass CTP [5], [6], where gain/delay of the input and quantizer paths are matched at dc, a bandpass CTP should match paths at f_o [7]. Fig. 1(b) compares the magnitude of the leakage transfer function for matching at dc and at f_o.

The obvious choice for $H_1(s)$ in Fig. 1(a) is a bandpass transfer function. However, a similar response around f_o can also be achieved with a high-Q lowpass filter. The advantage of using a low-pass $H_1(s)$ is that it exhibits a sharper roll-off at high frequencies as seen in Fig. 1(c). Consequently, DAC images at $(f_s - f_o)$ experience a higher attenuation. As a result, a higher-gain residue-amplifying filter can be used.

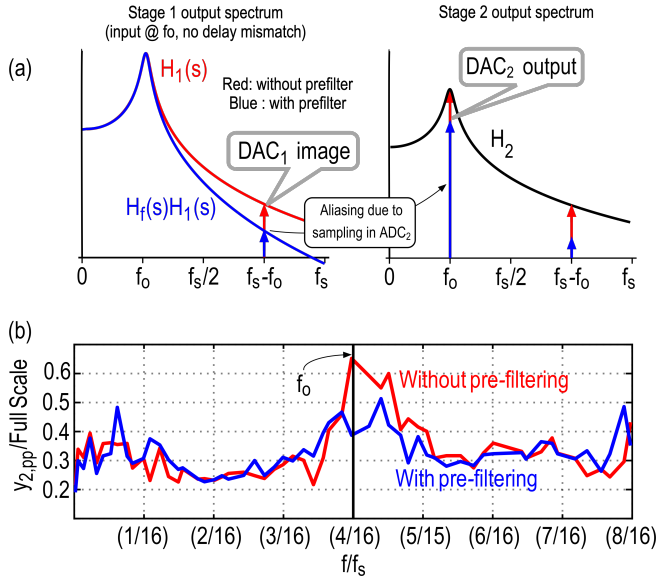
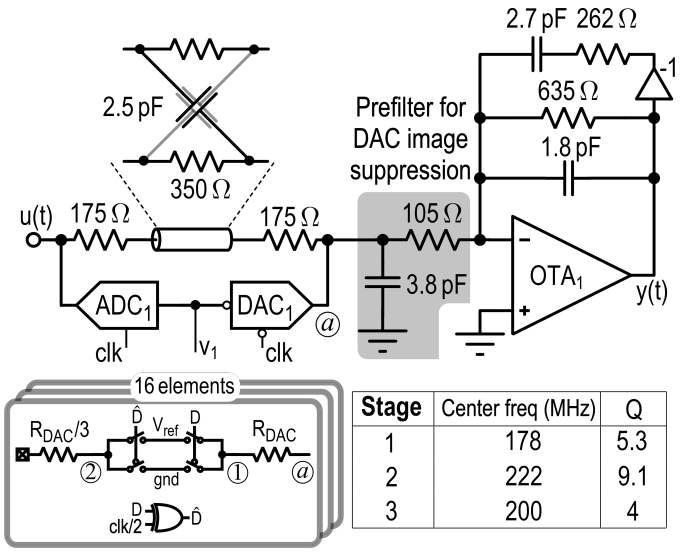


Fig. 2. (a) Prefiltering in stage-1 suppresses DAC_1's images, reducing peak-to-peak swing at the second-stage output. (b) Simulated (normalized) peak-to-peak swing of the second-stage output with/without prefiltering.

DAC images contribute significantly to the residue in a bandpass CTP since the ratio of input to image frequencies is large. Apart from increasing the peak-to-peak residue of the first stage, images impact the pipeline in another way, as explained using Fig. 2(a). For an input at f_o, the unsuppressed image of DAC_1 at $(f_s - f_o)$ at stage-1's output y_1 is aliased back to f_o by the sub-ADC of stage 2. Since this aliased component at f_0 is injected into the residue-amplifying filter of stage 2 by DAC_2, the peak-to-peak value of stage-2's output (namely y_2) increases. Using a lowpass prefilter ($H_f(s)$) with corner frequency of $f_s/2$ in stage-1 addresses this problem by suppressing DAC_1's image. The result of using prefiltering on the peak-to-peak value of the stage-2 output is shown in Fig. 2(b). Notice the increase in $y_{2,pp}$ around f_o. Since the bandwidth of the lowpass prefilter is much higher than the passband frequency, it does not impact the the inband magnitude response.

III. Stage Architecture and Circuit Design

Fig. 3 shows the simplified single-ended schematic of the CTP's first stage. The 17-level coarse quantizer formed by



Stage	Center freq (MHz)	Q
1	178	5.3
2	222	9.1
3	200	4

Fig. 3. Simplified single-ended schematic of the first stage. The table shows the gain, center frequency and Q of the stages.

ADC_1-DAC_1 creates approximation to the input $u(t)$. DAC_1 is clocked half clock cycle after ADC_1 to give the latter enough time to make a decision. To minimize the residue current, the input is delayed using a single-section RC lattice. The residue current is processed by a passive prefilter (in the gray box in Fig. 3). As described earlier, the purpose of the prefilter is to attenuate the images created by DAC_1. The prefiltered residue is then processed by a high-Q lowpass resonator with a center frequency f_o.

The resonator is formed by OTA_1 and the feedback network around it. Positive feedback through the 2.7 pF+262Ω creates a high quality factor resonator [3]. The second and third stages of the CTP do not need prefiltering since they process largely noise-like waveforms, and DAC images are not problematic. They use the same resonator and OTA structures, except that they are impedance scaled to save power. The center-frequencies and quality factors of the filters in the pipeline stages are given in the table in Fig. 3. The overall gain of the stages in the passband is about 15.

Fig.4(a) shows the single-ended block diagram of the four-stage feedforward-compensated OTA used in this work. The frequency-dependent gain of the OTA is shown in Fig. 4(b). The unity-gain bandwidth is about 1.7 GHz, and the nominal gain at 200 MHz is ≈47 dB.

ADC_1 is a flash ADC that employs the low-kickback comparators similar to those used in [8], [9]. The coarse ADCs in the second and third stages are StrongArm latch based structures. All DACs are resistive. DAC_1 is a 16-element reference-switched design, as shown in the callout of Fig. 3. R_{DAC} is switched between V_{ref} and ground depending on the bit D. To prevent distortion caused by data-dependent switching current drawn from the reference by parasitic capacitance at node ①, an open-circuit dummy element ($R_{dac}/3$) is switched by a sequence $\hat{D}$ which makes a transition when D does not and vice versa [8].

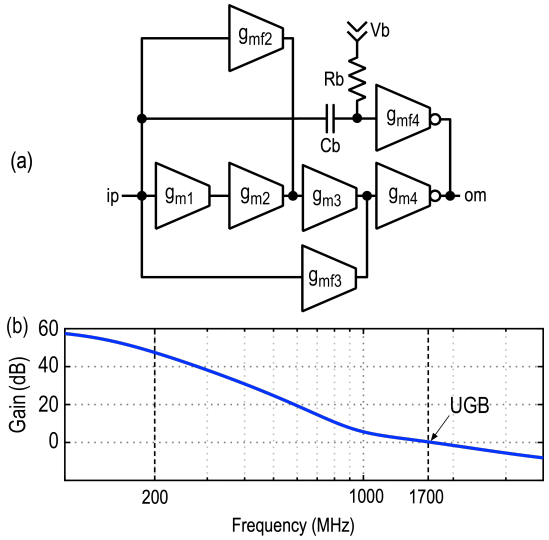


Fig. 4. (a) Simplified single-ended schematic of the 4-stage OTA used in stage 1. (b) Magnitude response of the layout-extracted opamp.

The second and third stages of the CTP are impedance scaled to save power. They do not need prefiltering, use 9-level quantizers, and employ the OTA architecture of Fig. 4.

IV. Measurement Results

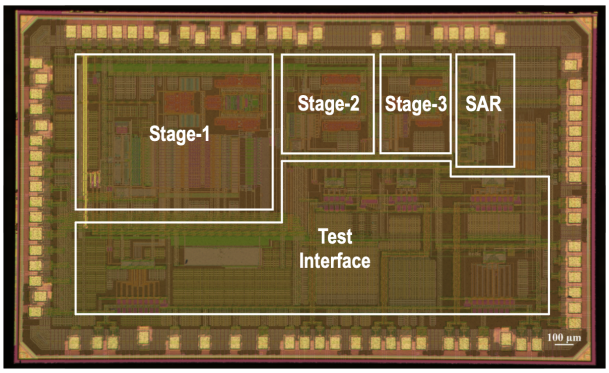


Fig. 5. Chip micrograph.

A prototype chip was fabricated in a 65 nm GP CMOS process. Fig. 5 shows the chip micrograph, with the layout superimposed on it. The active area of bandpass CTP is about 2.55mm^2. The chip was mounted in a QFN package for testing.

The digital outputs of the three stages and the back-end ADC were brought off chip, and appropriately combined in MATLAB. The transfer functions of the reconstruction filters are IIR, but are approximated by sufficiently long FIR filters. System-level simulations indicate that each reconstruction FIR filter needs 80 taps. The coefficients are obtained using the foreground frequency-domain technique described in [10].

Fig. 6(a) shows the output PSD of the converter for a full-scale input at f_{in}=201 MHz. A -78 dBFS aliased third harmonic, which lies in-band, is seen. The SNDR is 68.5 dB.

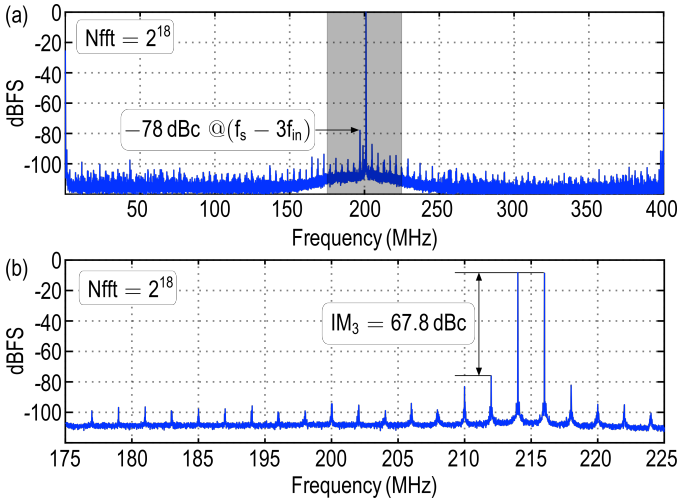


Fig. 6. (a) Output PSD for a single-tone 0 dBFS input at 200 MHz. (b) Measured IM_3 tones for two -6 dBFS input tones at 214 MHz and 216 MHz.

Fig. 6(b) shows the results of an in-band IM_3 test for -6 dBFS tones at 214 MHz and 216 MHz. The third-order intermodulation distortion is seen to be -67.8 dBc.

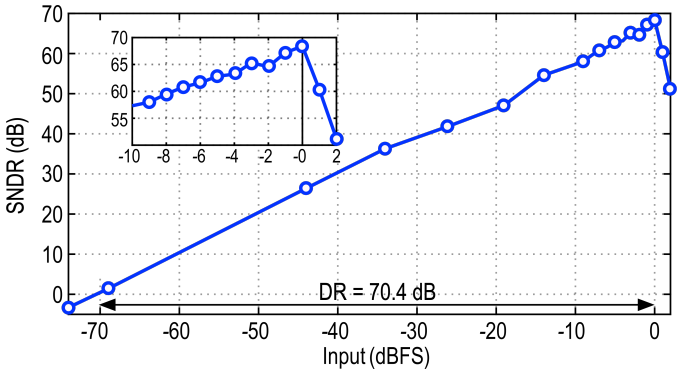


Fig. 7. Measured SNDR with respect to the amplitude of tone at 200 MHz. The dynamic range is estimated to be 70.4 dB.

The measured dynamic-range plot is given in Fig. 7. The converter achieves a dynamic range of 70.4 dB.

The STF of the converter is shown Fig.8(a). As expected, it is a bandpass response with a sharp roll-off beyond the signal band. The STF in the first Nyquist band (575−625 MHz), measured with a -25 dBFS tone is shown in Fig. 8(b). A minimum alias rejection of 60 dB is seen.

The bandpass CTP consumes 75 mW from a 1.2 V supply. Of this, 45 mW is dissipated in the opamps, 18 mW in the coarse quantizers, and 12 mW in the back-end SAR ADC. The Schreier Figure-of-Merit(FoM) of our converter is 157 dB. A few observations are in order.

a. Thanks to the pipeline architecture, the CT-bandpass ADC is stable up to 0 dBFS (and more). Contrast this with a bandpass CT$\Delta\Sigma$M, whose maximum stable amplitude is about -3 dBFS.

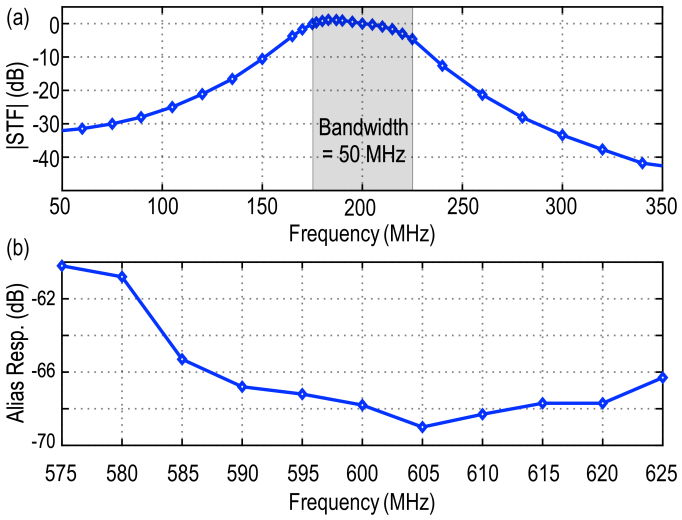


Fig. 8. (a) Measured STF from 50-350 MHz. (b) Alias response ($\equiv |STF(f)/STF(f-f_s)|$) in the first Nyquist band (575−625 MHz).

b. The in-band noise spectral density (see Fig. 6(a)), which is largely due to thermal noise is about 12 dB higher than the NSD at out-of-band frequencies (which is mostly due to the quantization noise of the back-end ADC).
c. The in-band NSD is largely flat. Contrast this with the thermal noise spectral density that would be obtained from a sixth-order stand-alone active bandpass filter, which would exhibit significant peaks at the band-edge frequencies.
d. The out-of-band NSD of the CT-bandpass ADC is also flat, unlike in a bandpass CTΔΣM whose NSD increases by several orders of magnitude outside the signal band.
e. The STF of the bandpass CTP begins to roll off sharply outside the signal band. Contrast this with that of a bandpass CTΔΣM , whose STF cannot be narrow band due to the constraints imposed by the noise transfer function.

Table I summarizes the performance of our design, and compares it with prior art bandpass ADCs. Thanks to the open-loop nature of the architecture, our design not only achieves a significantly higher bandwidth in the same process technology but also an STF that rolls off sharply outside the signal band. Furthermore, the Schreier FoM is comparable to that of [3] while achieving 2× the bandwidth, and significantly higher than those of [2] and [4].

V. Conclusion

We presented a bandpass continuous-time pipeline ADC that is equivalent to a 50 MHz bandwidth sixth-order bandpass filter with a 200 MHz center frequency followed by a 12-bit 800 MS/s ADC. When compared to prior-art bandpass CTΔΣMs realized in the same process technology, our design achieves significantly higher bandwidth and a sharply selective STF. The promising results from this first prototype shows that the bandpass CTP is a compelling alternative to continuous-time bandpass CTΔΣMs.

TABLE I
Comparison of performance of the CTP with prior-art bandpass ADCs.

Parameter	This Work	Chae JSSC 2013 [2]	Chae JSSC 2016 [3]	Lu JSSC 2010 [4]	Schreier JSSC 2006 [1]
Architecture	**BP CTP**	BP CTDSM	BP CTDSM	BP CTDSM	Quadrature BPCTDSM
Process (nm)	**65**	65	65	180	180
Order	**Sixth**	Fourth	Sixth	Sixth	Sixth
f_o (MHz)	**200**	200	200	200	44
BW (MHz)	**50**	24	25	10	8.5
f_s (MHz)	**800**	800	800	800	264
SNDR (dB)	**68.5**	58	69	68.4	77
DR (dB)	**70.4**	60	70	70	90†
IIP_3 (dBFS)	**27.9**	22.4	27	28.8	30
Max. Input (dBFS)	**0**	-4	-4	-2	0
Power (mW)	**75**	12	35	160	375
Min. AR (dB)	**60**				65
Area (mm^2)	**2.55**	0.2	0.25	2.5	2.5
FoM (dB)‡	**157**	151	158	146	151

† Implements gain scaling to improve dynamic range.
‡ FoM = SNDR(dB) + $10\log_{10}$(BW/Power)

References

[1] R. Schreier, N. Abaskharoun, H. Shibata, D. Paterson, S. Rose, I. Mehr, and Q. Luu, "A 375-mW quadrature bandpass ΔΣ ADC With 8.5-MHz BW and 90-dB DR at 44 MHz," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2632–2640, 2006.

[2] H. Chae, J. Jeong, G. Manganaro, and M. P. Flynn, "A 12 mW low power continuous-time bandpass ΔΣ modulator with 58 dB SNDR and 24 MHz bandwidth at 200 MHz IF," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 405–415, 2014.

[3] H. Chae and M. P. Flynn, "A 69 dB SNDR, 25 MHz BW, 800 MS/s continuous-time bandpass ΔΣ modulator using a duty-cycle-controlled DAC for low power and reconfigurability," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 649–659, 2016.

[4] C.-Y. Lu, J. F. Silva-Rivas, P. Kode, J. Silva-Martinez, and S. Hoyos, "A sixth-Order 200 MHz IF bandpass sigma-delta modulator with over 68 dB SNDR in 10 MHz bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1122–1136, 2010.

[5] H. Shibata, V. Kozlov, Z. Ji, A. Ganesan, H. Zhu, D. Paterson, J. Zhao, S. Patil, and S. Pavan, "A 9 GS/s 1.125-GHz BW oversampling continuous-time pipeline ADC achieving -164-dBFS/Hz NSD," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3219–3234, 2017.

[6] D. O'Hare, A. G. Scanlan, E. Thompson, and B. Mullane, "Bandwidth enhancement to continuous-time input pipeline ADCs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 2, pp. 404–415, 2017.

[7] M. W. Ismail, X. Liu, and T. C. Carusone, "Inductorless bandpass noise-shaping continuous-time pipelined ADC architectures," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–5.

[8] S. Manivannan and S. Pavan, "A 65-nm CMOS continuous-time pipeline ADC achieving 70-dB SNDR in 100-MHz bandwidth," *IEEE Solid-State Circuits Letters*, vol. 4, pp. 92–95, 2021.

[9] S. Pavan, S. Manivannan, and N. Basavaraj, "Analysis and design of wideband filtering ADCs using continuous-time pipelining," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 1, pp. 268–281, 2024.

[10] N. Basavaraj, S. Manivannan, and S. Pavan, "Simplified simulation and measurement of the signal transfer function of a continuous-time pipelined analog-to-digital converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 10, pp. 3993–3997, 2022.