

# An 8.65-GHz 8<sup>th</sup>-Order-Polynomial DPD FMCW PLL Achieving 10-GHz/ $\mu$ s Chirp Slope with 0.039% rms Frequency Error and 3-GHz Chirp Bandwidth

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**Abstract**—This paper presents a FMCW PLL with fast chirp slope and wide chirp bandwidth. An 8<sup>th</sup>-order polynomial digital predistortion (8OP-DPD) is proposed to achieve low root-mean-square (rms) frequency error at high chirp slopes. An overlap correction circuit is implemented to eliminate the non-monotonicity in the tuning curve of the digitally controlled oscillator (DCO), enabling accurate polynomial curve fitting. The proposed FMCW PLL is fabricated in a 65-nm CMOS process and occupies a core area of 0.432 mm<sup>2</sup>. Measurement results show an output frequency range from 7.15 to 10.15 GHz. The PLL achieves a chirp slope of 10 GHz/ $\mu$ s at a center frequency of 8.65 GHz and a 3-GHz chirp bandwidth, corresponding to a normalized chirp slope of 115.6%/ $\mu$ s with 0.039% rms frequency error, while consuming 20.16 mW.

**Index Terms**—Digitally controlled oscillator (DCO), FMCW PLL, fast chirp slope, higher-order polynomial digital predistortion (DPD), wide chirp bandwidth.

## I. INTRODUCTION

The FMCW radars have been widely used in fields like autonomous driving and healthcare. For applications requiring a maximum unambiguous velocity >340 km/h and range resolution down to sub-centimeter levels, the chirp generator in FMCW radars must be capable of producing chirps with a period <10  $\mu$ s and a bandwidth (BW) >15 GHz, requiring a chirp slope >1.5 GHz/ $\mu$ s [1]. Moreover, a faster chirp enables faster target identification and improves the sensitivity for separating multiple targets [1]. To achieve a fast chirp slope, phase-locked loops (PLLs) utilizing a two-point modulation (TPM) technique [Fig.1(a)] are widely employed as chirp generators in FMCW radars, as this approach overcomes the PLL's loop bandwidth limitation [1–6]. However, the inherent square-root relationship between frequency and capacitance in the digitally-controlled-oscillator (DCO) results in significant chirp nonlinearity and large frequency error which limits the radar's detection accuracy [Fig.1(b)]. DPD techniques have been proposed to linearize the DCO's tuning curve, thereby reducing frequency error [1–6]. However, existing DPD methods struggle to achieve rms frequency errors below 0.05% with ultra-wide chirp BWs >2.5 GHz and ultra-fast chirp slopes >5 GHz/ $\mu$ s. To address these challenges, this paper presents an 8.65 GHz DTC-based sampling PLL by

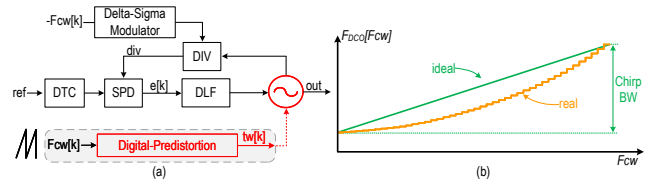


Fig. 1. The difficulties in high-linearity and low rms frequency error FMCW PLL.

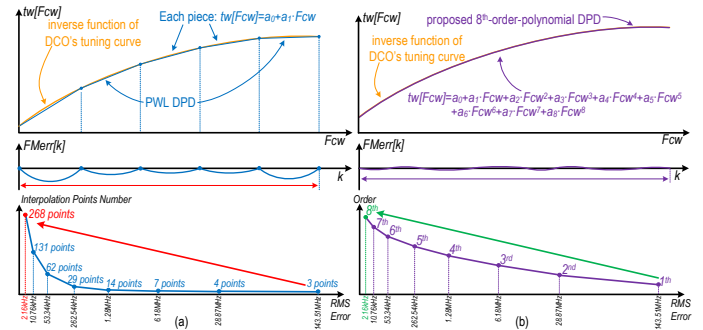


Fig. 2. The comparison between (a) uniform PWL-DPD FMCW PLL and (b) proposed 8OP-DPD FMCW PLL.

employing a proposed 8OP-DPD technique and a DCO with fast-charging switched-capacitors, achieving a chirp slope of 10 GHz/ $\mu$ s and a chirp bandwidth of 3 GHz with a rms frequency error < 0.039% for both triangular and sawtooth chirps.

Fig.2(a) illustrates the piecewise linear DPD (PWL-DPD) technique [5]. PWL-DPD approximates the ideal inverse function of DCO's tuning curve through piecewise interpolation, partially mitigating the nonlinearity induced by the DCO. However, with a limited number of interpolation points, the approximation is inadequate, offering limited improvement in chirp linearity and frequency error. To meet stringent frequency error requirements, PWL-DPD necessitates many interpolation points. For instance, reducing the rms frequency error requirement to <100 kHz demands over 45 interpolation points, while achieving 2.16 kHz requires as many as 268 points, significantly increasing the hardware resources needed to store the weights for each segment. However, using high-order polynomial DPD for



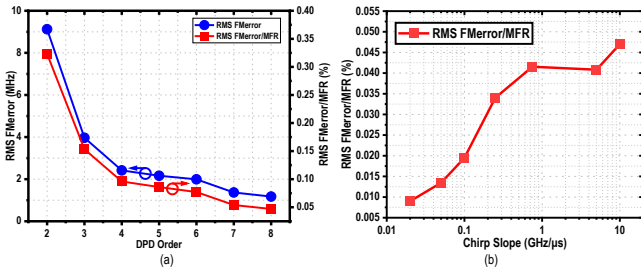


Fig. 5. Measured triangle chirp average rms  $FM_{error}$  (a) versus different DPD orders at the maximum chirp slope and (b) versus different chirp slopes.

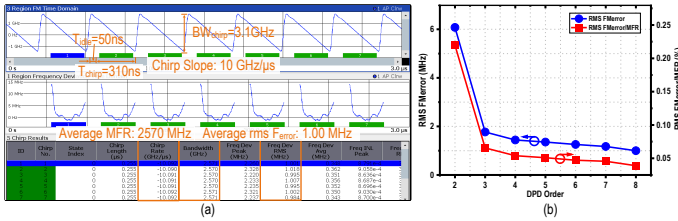


Fig. 6. (a) Sawtooth chirp and  $FM_{error}$  and (b) comparison of measured rms  $FM_{error}$  with different DPD orders at the maximum chirp slope.

overlap correction circuit, which uses a delta-sigma modulator (DSM) [5, 6], requires the tuning range of the finer switched-capacitor bank to be at least twice the step size of the coarse switched-capacitor bank. Besides, if all of the coarse switched-capacitors use the same weights for overlap correction, the capacitor mismatches can cause discontinuities in DCO's tuning curve, increasing frequency error. To avoid these issues,  $tw$  is first quantized by a flash quantizer [7] to obtain the thermometer-coded DCO control word  $D_{CTRLT}[31:1]$  and the quantization output  $D_M$ . The quantization error  $RES[1]$  is further quantized by a cascaded quantizer to generate the binary-weighted DCO control word  $D_{CTRLB}[15:0]$ . This cascaded quantizer progressively quantizes  $RES[1]$  using eleven 1-bit quantizers to produce  $D_{CTRLB}[15:5]$ . The quantization error from the final stage quantizer is used to control the last five bits of the switched-capacitor bank,  $D_{CTRLB}[4:0]$ . In the overlap correction circuit,  $BIN[5]$  to  $BIN[15]$  represent the weights of the binary-weighted fine switched-capacitor bank, while  $TH[1]$  to  $TH[31]$  are the cumulative weights of the thermometer-coded coarse switched-capacitor bank, which are derived through a binary-search-based foreground calibration.

After overlap calibration, a foreground calibration is performed to determine the polynomial coefficients for the inverse function of the DCO's tuning curve. This inverse function is obtained by sweeping  $tw$  and measuring the corresponding  $f_{DCO}$ . Here,  $f_{DCO}$  serves as the input to the inverse function, while  $tw$  acts as the output. To avoid overfitting, the measured frequency points must cover the entire frequency range of the chirps and it requires at least 9 evenly distributed measurement points to solve for the 9 polynomial coefficients. The foreground calibrations are implemented using software programming on an off-chip processor, which is an essential component for radar signal processing in a radar system, without extra hardware. Further background calibrations can be implemented by using

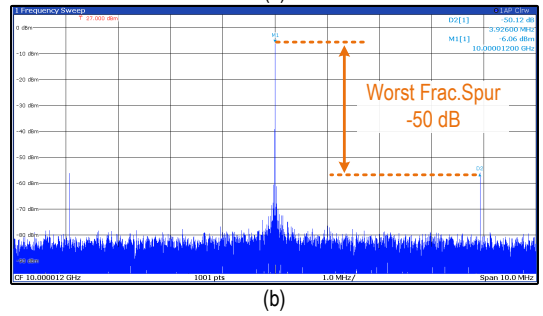
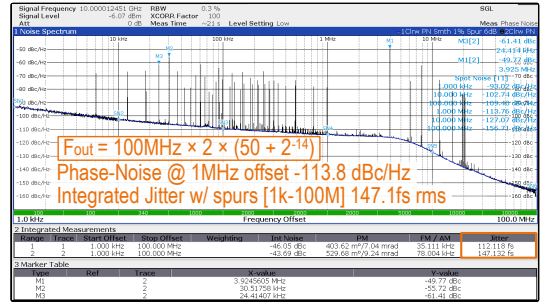


Fig. 7. Measured PLL's jitter and worst-case fractional spur in fractional-N mode.

least-mean-square (LMS) algorithm [5, 9], which requires a locked PLL and becomes slow with a slow chirp slope and a narrow calibration loop bandwidth for low calibration error. The foreground calibration can provide the initial conditions for the background calibrations to avoid an unlocked PLL due to large initial frequency error and assist background calibration convergence.

### B. Proposed DCO with Fast-charging Switched Capacitors

Fig.3(b) illustrates the proposed DCO with a fast-charging switched-capacitor bank. The DCO is designed with a 5-bit thermometer-coded coarse switched-capacitor bank and a 16-bit binary-weighted fine switched-capacitor bank with capacitor dividers applied to the last 10 bits to achieve high resolution. In conventional switched-capacitors, when transistors transition from the on-state to the off-state, the bias resistors slow down the capacitor charging and prevent the rapid pull-up of drain and source voltages to  $V_B$ . Consequently, the DCO would have large frequency settling error, limiting FMCW PLL's frequency error. To achieve fast switching, a pre-charge delay line generates a pulse signal  $SW_1$  immediately after the  $SW$  signal transitions from high to low, turning on transistors  $M_1$  and  $M_2$ . This action increases the charging current, rapidly raising the voltages at nodes X and Y close to  $V_B$ . The fast-charging switched capacitor technique is applied to both the coarse switched-capacitor bank and the first 6 bits of the fine switched-capacitor bank.

## III. MEASUREMENT RESULTS

The proposed FMCW PLL is implemented in a 65 nm CMOS process, with a chip micrograph shown in Fig.8. The core area is around 0.432 mm<sup>2</sup>. At a maximum chirp slope of 10 GHz/μs, the measured power consumption is 20.16 mW. Fig.4(a) and Fig.4(b) shows the measured

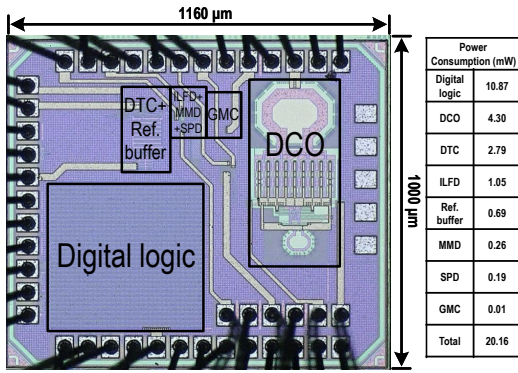


Fig. 8. Chip micrograph and power breakdown.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS.

	This Work	T. Francesco ISSCC'24	W. Xuan ISSCC'24	P.T. Renukaswamy ISSCC'23	Z. Shen ISSCC'21	P.T. Renukaswamy ISSCC'20	
Technology	65nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	40nm CMOS	28nm CMOS	
Architecture	TPM SPPLL	TPM DPPLL	TPM SSPLL	TPM CP-PLL + QDAC	TPM ADPLL	TPM SSPLL + QDAC	
DPD method	8 <sup>th</sup> -order-polynomial DPD	Non-uniform PWP DPD	2 <sup>nd</sup> -order curve fitting DPD	Uniform PWL DPD	Overlap compensation LUT	0 <sup>th</sup> -order LUT	
Chirp waveform	Saw & Tri	Saw & Tri	Saw & Tri	Saw	Saw & Tri	Saw	
Ref. Frequency [MHz]	100	250	100	80	200	80	
Frequency Range [GHz]	7.15 to 10.15	9.25 to 10.5	9.6 to 12.4	15 to 18.5	21.8 to 25.4	8.3 to 11.7	
MFR @ Max Slope [MHz]	2499	647	2160	1430	N/A	1140	
Max. chirp BW [MHz]	3000	680	2350	1500	3200	1210	
Max. chirp BW/Center freq. [%]	34.68	6.8	21.4	8.95	13.3	11.95	
Max Slope [GHz/μs]	10	0.68	2.3	0.11	0.32	0.095	
Max Slope/Center freq. [100%/μs]	1.156	0.069	0.209	0.007	0.014	0.010	
Sawtooth FM error at max chirp slope	RMS [kHz]	1000.3	151	1176	137.6	309	168
	RMS / Chirp BW [%]	0.032	**0.022	0.051	0.009	0.01	0.014
Triangular FM error at max chirp slope	RMS [kHz]	1174.1	131	1198.4	N/A	397	N/A
	RMS / Chirp BW [%]	0.039	**0.019	0.052	N/A	0.012	N/A
	RMS / MFR[%]	0.047	0.023	**0.055	N/A	N/A	N/A
*PN@1MHz offset (dBc/Hz)	-113.8	-116.5	-116	-109.1	-101.5	-108.7	
Jitter w/ spurs (fs rms) Integration BW [Hz]	147.1 [1k to 100M]	87.1 [1k to 100M]	148.7 [1k to 100M]	156 [10k to 100M]	N/A	313.4 [10k to 81M]	
Power (mW)	20.16	21	50.8	16.5	28	11.7	
Core Area (mm <sup>2</sup> )	0.432	0.34	1.2	0.6	0.26	0.9	

\*Normalized to 10 GHz \*\*Estimated from measured figure

frequency-modulation (FM) errors for both 2<sup>nd</sup>-order and 8<sup>th</sup>-order polynomial DPD at a chirp slope of 10 GHz/μs. The measured frequency range (MFR) is 2827 MHz and 2499 MHz, with average rms FM errors of 9.12 MHz and 1.17 MHz, respectively. Fig.4(c) shows the measured FMCW PLL spectrum, achieving a chirp BW of 3 GHz, covering frequencies from 7.15 GHz to 10.15 GHz. Fig.5(a) shows the average rms FM error of triangular chirps at the maximum chirp slope 10 GHz/μs using different polynomial DPD orders. Increasing the polynomial DPD order from 2<sup>nd</sup> to 8<sup>th</sup> improves rms FM error/MFR performance by around 7 times, which demonstrates the effectiveness of the proposed 8OP-DPD technique. Fig.5(b) shows the FM error performance of triangular chirps at different chirp slopes with the 8OP-DPD.

Fig.6(a) shows the measured sawtooth chirp at the maximum chirp slope of 10 GHz/μs, with an average rms FM error of 1.00 MHz, an MFR of 2570 MHz, and an idle time of 50 ns. The large peak error occurs only at the chirp turning points, while for most of the time, the FM<sub>error</sub>

remains very small. Fig.6(b) reports the average rms FM errors of sawtooth chirps at the maximum chirp slope with different polynomial DPD orders. Increasing the polynomial DPD order from 2<sup>nd</sup> to 8<sup>th</sup> improves the rms FM<sub>error</sub>/MFR performance by approximately 5.6 times. Fig.7 reports the PLL performance at a near integer-N setting of around 10 GHz, showing a rms jitter of 147.1 fs (integrated from 1 kHz to 100 MHz, including spurs) and a worst-case fractional spur of -50 dBc. Table I summarizes the performance of this work and compares it with prior arts. With a comparable normalized frequency error, power consumption, area, and a wider normalized chirp bandwidth, the proposed FMCW PLL achieves the largest normalized chirp slope (chirp slope/center frequency) of 115.6%/μs.

#### IV. CONCLUSION

This work proposes a FMCW PLL with a normalized chirp slope of 115.6%/μs that is >5 times faster than that of prior arts. It employs an 8OP-DPD technique and an overlap correction circuit. The polynomial-DPD technique allows achieving low frequency error with only a few polynomial orders. Compared with DSM-based overlap correction, the flash-quantizer-based overlap correction circuit halves the tuning range requirements of finer switched-capacitor bank. Each coarse switched-capacitor bank use different weights for overlap correction to avoid mismatch-induced discontinuities in DCO's tuning curve.

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