A Wideband Class-E Wi-Fi Power Amplifier using Scalable Transformer-Based Output Network

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***Abstract*—In this paper, a novel scalable transformer-based output matching network (OMN) for differential Class-E power amplifier (PA) is developed and used to elaborate a comprehensive design methodology that maximizes the operating bandwidth. The proposed methodology is used to design a wideband fully-integrated WiFi-6 PA, in 130 nm SOI-CMOS process, achieving more than 27.8dBm of saturated output power (P_{sat}) with 32-39.5% of peak PAE over the 5.1 to 6.6GHz frequency band. The proposed PA achieves state-of-the-art performance with higher than 18.7dBm of linear output power with -42dB of EVM using 80MHz 1024-QAM WiFi-6 signal from 5.1 to 6.6GHz.**

Keywords— CMOS, Wi-Fi, Power Amplifier, Class-E.

I. Introduction

The demand for wideband, high-efficiency, and compact RF power amplifiers is rapidly increasing, driven by the growing number of frequency bands used in cellular and Wi-Fi applications. To address these challenges, Class-E PAs have been widely investigated due to their strong potential for achieving efficient, wideband and compact implementation [1]. In particular, the single-ended Class-E OMN with finite dc-feed inductor is used due to its simplicity and straightforward parameters calculation [2]. In [3], a single-ended Class-E OMN is implemented using a scalable bondwire-based transformer to achieve compact and wideband performance. However, the proposed approach requires additional LC-ladder matching to achieve the desired behavior. Moreover, differential Class-E PAs with transformer-based [4] and transmission-line [5] baluns have been proposed for cellular applications to achieve higher output power and improved harmonic rejection. However, these later require additional drain supply inductors.

In this work, a scalable transformer-based output matching network (OMN) synthesis approach for differential Class-E PA is proposed. The OMN network elements are directly calculated to achieve ideal Class-E waveform shaping for any load resistance R_L, without requiring any additional matching stages or drain supply inductors as opposed to [3], [4]. The scalable OMN model is used to elaborate a new design methodology that maximizes the operating bandwidth of the PA by allowing the use of lower loaded Q benefiting from the inherent common-mode rejection of the differential topology compared to the single-ended one. The proposed methodology is employed to design a wideband fully-integrated differential Class-E PA in a 130nm SOI-CMOS process. Under 3.8V supply voltage, the PA achieves a measured P_{sat} and PAE higher than 27.8dBm and 32% respectively over the 5.1-6.6GHz frequency band. Moreover, it achieves higher than 18.7dBm of linear output power with -42dB of EVM using 80MHz MCS11 (1024-QAM) 802.11ax signal from 5.1 to 6.6GHz.

II. Wideband Transformer-based Class-E PA

A. Conventional Single-ended Class-E PA

The generalized form of the single-ended Class-E PA output matching network, Fig. 1, includes a series inductance L_b and a finite DC-feed inductor L_{dc} [6]. The inductor L_{dc} provides the DC current to the device during the on-state and contributes along with the shunt capacitance C_{sh} to ensure the AC current flow to the output during the off-state. The series reactance X_s adjusts the initial phase-shift of the output current to avoid current and voltage overlap at the device drain. Finally, the $L_{f_0} - C_{f_0}$ resonator is used to filter-out the harmonics and to achieve a pure sinusoidal output current through the load R_E.

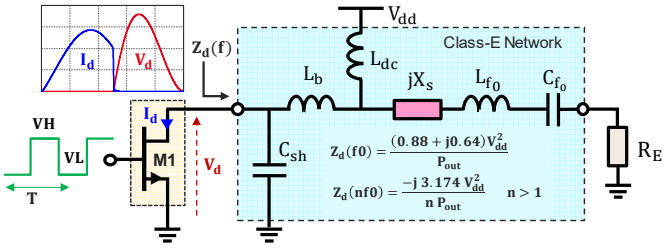

Fig. 1. Single-ended Class-E PA with generalized load network [6].

The analytical solution of the generalized Class-E network is given in [6] considering a square input drive signal with 50% duty cycle. The class-E output-matching network elements $\{C_{sh}, L_b, L_{dc}, X_s, L_{f_0}, C_{f_0}, R_E\}$ are expressed in terms of the target output power P_{out}, the supply voltage V_{dd}, the angular design frequency ω_0, the loaded quality-factor Q_L of the harmonic filter $L_{f_0} - C_{f_0}$ and the so-called K-set coefficients $\{K_P, K_L, K_C, K_X\}$, TABLE I. The K-set coefficients depend on the free parameters $\{\alpha, \chi\}$, where $\alpha = L_b/L_{dc}$ and $\chi = \omega_0\sqrt{L_{dc}C_{sh}}$. It is important to mention that, for $\{Q_L \gg 1,\ \alpha \geq 0, \chi > 0.5\}$, the Class-E network presents the same drain plane impedance Z_d at fundamental and harmonic frequencies. Also, the presence of the on-state resistance r_{on} does not change the equations of Table. 1 but it impacts the K-set coefficients values as discussed in [2], [7].

TABLE I. Network elements [6].

$R_E = \frac{K_P(\alpha,\chi)\, V_{dd}^2}{P_{out}}$	$C_{sh} = \frac{K_C(\alpha,\chi)}{\omega_0\, R_E(\alpha,\chi)}$
$X_s = K_X(\alpha,\chi)\, R_E(\alpha,\chi)$	$L_{dc} = \frac{K_L(\alpha,\chi)\, R_E(\alpha,\chi)}{\omega_0}$
$L_{f_0} = \frac{Q_L R_E(\alpha,\chi)}{\omega_0}$	$C_{f_0} = \frac{1}{L_{f_0}(\alpha,\chi)\, \omega_0^2}$

B. *Proposed Transformer-based Differential Class-E OMN*

The proposed transformer-based differential Class-E OMN is depicted in Fig. 2. It is composed of a transformer (XFMR) connected to a parallel input capacitor C_i and a series output capacitor C_o connected to an arbitrary load R_L.

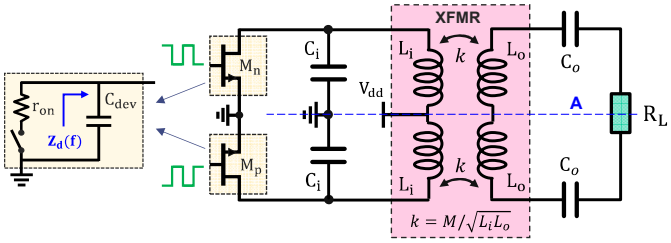

Fig. 2. Schematic of the proposed transformer-based differential Class-E PA.

Considering the plane of symmetry A , Fig. 2, and replacing the RF transformer by its equivalent circuit model, the half OMN can be represented using the equivalent network shown in Fig. 3-a. Then, the inductor $L_o - T_i\,M$ and the capacitor C_o can be transferred to the primary side leading to the network depicted in Fig. 3-b, which corresponds to a cascade of a Class-E network followed by an ideal $1:\mathrm{T_i}$ transformer. The intermediary transformation ratio (T_i) is calculated to transform $R_L/2$ into the optimum Class-E network load R_E:

$$T_i = \sqrt{\frac{R_L}{2\,R_E}} = \sqrt{\frac{R_L P_{out}}{4\,K_P\,V_{dd}^2}} \qquad (1)$$

with P_{out} being the overall output power of the differential PA. As discussed in [6], for $K_X(\alpha,\chi) \geq 0$ the reactance jX_s (Fig. 1) acts as an inductor and can be merged with L_{f_0}, while for $K_X(\alpha,\chi) < 0$ it acts as a capacitor and can be merged with C_{f_0}. Hence, by equating the network elements between Fig. 1 and Fig. 3-b, the parameters L_o and C_o can be expressed as follow:

$$L_o = \frac{R_L}{2\omega_0}[Q_L + K_L + \beta\,K_X] \qquad (2)$$

$$C_o = \frac{2}{R_L\omega_0}\left[\frac{1}{Q_L + K_X\,(\beta - 1)}\right] \qquad (3)$$

where β is a binary parameter introduced to switch between the two cases (i.e. $\beta = 1$ for $K_X \geq 0$ and $\beta = 0$ for $K_X < 0$). Similarly, using the Class-E network relationships $L_b = \alpha L_{dc}$, and identifying $L_{dc} = M/T_i$ and $L_b = L_i - M/T_i$, the primary side inductor L_i can be expressed as follow:

$$L_i = 2K_L K_P\,V_{dd}^2(1+\alpha)/(\omega_0 P_{out}) \qquad (4)$$

Moreover, using (2) and (4) and the relationship $M = T_i \cdot L_{dc}$, the required coupling coefficient k can be written as:

$$k = \frac{M}{\sqrt{L_i L_o}} = \sqrt{\frac{K_L}{(1+\alpha)\,(K_L + Q_L + \beta\,K_X)}} \qquad (5)$$

Finally, the input capacitor C_i is given by:

$$C_i = \mathrm{K_C P_{out}}/(2\mathrm{K_P} V_{dd}^2 \omega_0) - C_{dev} \qquad (6)$$

Note that the device's output capacitance C_{dev} should smaller than or equal to C_{sh} to ensure $C_i \geq 0$.

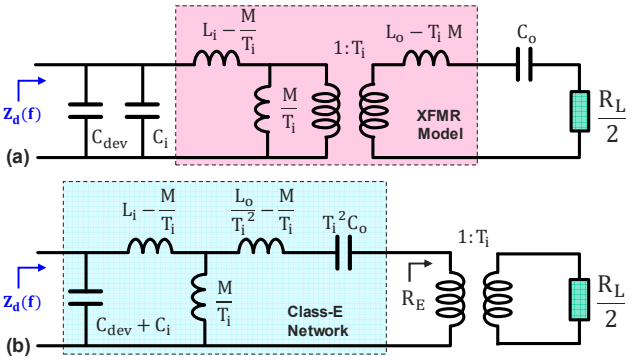

Fig. 3. Equivalent circuit model used to analyze the proposed PA.

Equations (1) to (6) along with the K-set coefficients form a scalable model allowing to calculate the transformer-based differential Class-E OMN parameters $\{C_i, C_o, L_i, L_o, k\}$ as a function of the input design parameters $\{f_0,\ P_{out}, V_{dd}, R_L\}$and the free design parameters $\{\alpha, \chi, Q_L\}$. In the next section, the scalable OMN model is used to elaborate a new design methodology allowing to select the optimum set $\{\alpha, \chi, Q_L\}$ that maximizes the operating bandwidth of the PA.

C. *OMN Optimization for Wideband Operation*

The proposed design methodology is illustrated on a practical design example targeting the 5-7 GHz Wi-Fi bands. The PA is required to deliver 28.5dBm of overall output power P_{out} to the load $R_L = 50\Omega$ under $V_{dd} = 3.8\mathrm{V}$. A high-performance LDMOS device with >13.5V of breakdown voltage is used to ensure PA reliability under the high voltage swing of Class-E operation. The device has a normalized on-state resistance $R_{onW} = 1.8\ \Omega.\mathrm{mm}$, and normalized output capacitance $\mathrm{C_u} = 0.25\ \mathrm{pF/mm}$, with an output power density $\mathrm{P_d} = 0.35\ \mathrm{W/mm}$. Note that to account for the OMN losses (estimated to 1dB), and the conduction losses causes by r_{on} (estimated to 0.8dB based on [7]), the total target P_{out} at the devices drain plane should be 30.3dBm (i.e. 27.3dBm per device). Hence, the required device size, and the corresponding on-resistance and output capacitance can be calculated as $W_{n,p} = 0.5\,P_{out}/P_d = 1.5mm$, $r_{on} = R_{onW}/W_{n,p} = 1.17\Omega$ and $C_{dev} = W_{n,p} \cdot \mathrm{C_u} = 380fF$.

To achieve wideband operation, we first focus on the choice of the loaded Q_L of the harmonic filter. As discussed in [3], the choice of Q_L is a trade-off between efficiency and bandwidth for single-ended Class-E PAs. Selecting high Q_L leads to an efficient but narrowband PA, while selecting low Q_L leads to wider operating bandwidth but with lower efficiency due to the imperfect harmonic termination and waveform shaping. In contrast, the proposed differential Class-E PA benefits from its inherent common-mode rejection property allowing to reduce Q_L with minimal degradation of the P_{out} and efficiency and resulting in a wider operating bandwidth compared to single-ended Class-E, as can be seen in Fig. 4. In fact, since the even harmonics are naturally rejected by the output transformer, the harmonic filter is only required to reject the odd harmonics which are 10 times lower than the even harmonics in the drain-plane Class-E waveform and hence have low impact on the PA performance.

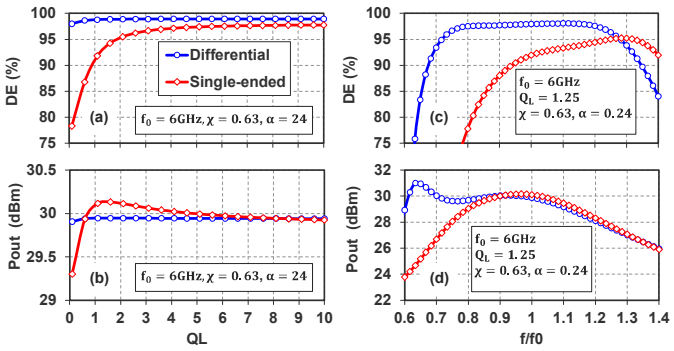

Fig. 4. (a) DE, (b) P_{out} versus Q_L, and (c) DE, (d) P_{out} versus normalized frequency for differential and single-ended Class-E PAs.

Next, to select the optimum set $\{\alpha, \chi\}$ that reduces the OMN size and facilitates the implementation, we plot the OMN parameters $\{C_i, C_o, L_i, k\}$ and the turns ratio $n_t = L_o/L_i$ versus $\chi = [0.55:0.95]$ and $\alpha = [0:1]$ for $Q_L = 1.25$ and $f_0 = 6GHz$. In addition, we plot the theoretical maximum class-E operating frequency $f_{0,max}$ for the used process (i.e. P_d/C_u) [8]:

$$f_{0,max} = \frac{P_{out,dev}}{2\pi\, V_{dd}^2 C_{dev}} \frac{K_c}{K_p} = \frac{P_d}{2\pi\, V_{dd}^2 C_u} \frac{K_c}{K_p} \qquad (7)$$

As shown in Fig. 5-(a), increasing χ and α reduces $f_{0,max}$. Hence, for our case ($f_{0,max} \geq 7$ GHz), the choice of χ and α must be within the region below the dashed trend line. Moreover, reducing χ and α simultaneously leads to smaller L_i (Fig. 5-b) and higher $f_{0,max}$ but also higher n_t (Fig. 5-c) and coupling factor k (Fig. 5-d).

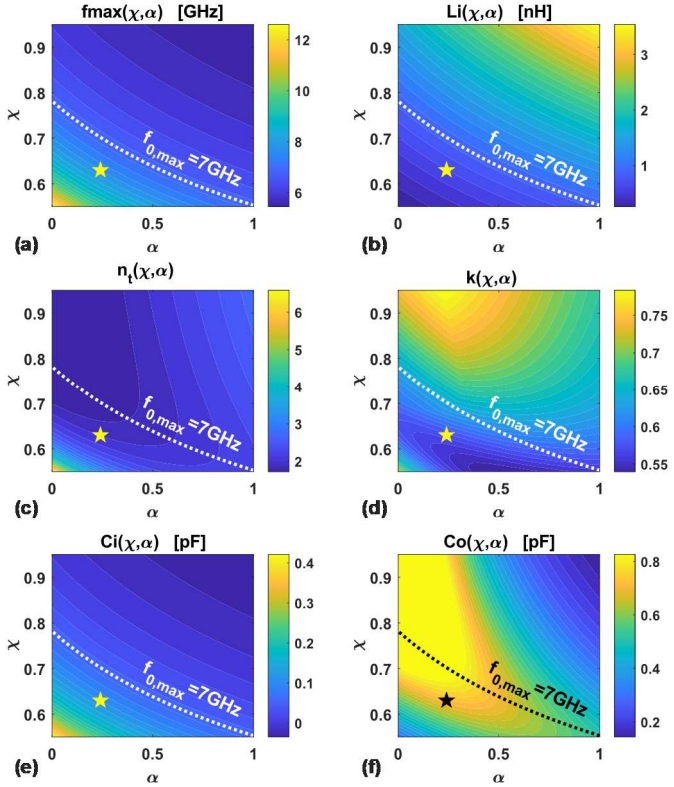

Fig. 5. Contours of the differential Class-E output network parameters versus χ and α for $Q_L = 1.25$, $P_{out} = 30.3dBm$, $V_{dd} = 3.8V$ and $f_0 = 6\ GHz$.

According to (2), selecting a lower Q_L reduces L_o (i.e. n_t) since L_i (i.e. (4)) does not depend on Q_L. However, according to (5), the use of low Q_L increases the required coupling factor k which can be difficult to achieve. Consequently, we choose $Q_L = 1.25$, $\chi = 0.63$ and $\alpha = 0.24$ which leads to $L_i = 0.7$nH, $n_t \approx 2$, $k = 0.62$, $C_i = 0.11$pF and $C_o = 0.72$pF. Note that higher k values could be achieved but requires the use of broad-side coupled transformer. In our case, we use an edge-coupled transformer in order to limit the capacitive coupling between the primary and the secondary windings and ensure the validity of the proposed theory in which the capacitive coupling has been ignored.

III. Implementation and Measurement

Based on the previous analysis, a fully-integrated differential Class-E PA, Fig. 6, is designed in a 130nm SOI-CMOS process to address the 5/6 GHz Wi-Fi frequency bands. The OMN is implemented based on the proposed methodology and optimized using electromagnetic simulation. The output-stage uses a cross-coupling neutralization capacitances pair (C_n) to improve its stability and gain. Note that C_n capacitance is tuned in presence of the input second-harmonic resonator ($L_Y - C_Y$) to optimize the AMAM and AMPM of the output stage. Moreover, a linear class-B driver stage is designed using a cascode transistor made of a common-source body-contact NMOS device and a common-gate LDMOS device each with a gate width of 0.45mm. A wideband inter-stage matching-network is designed to transform the input impedance of the output stage into the optimum load impedance of the driver stage. The RC network (R_x, C_x) is added to ensure the overall PA stability. Finally, a wideband input matching-network is designed to match the driver input to 50Ω.

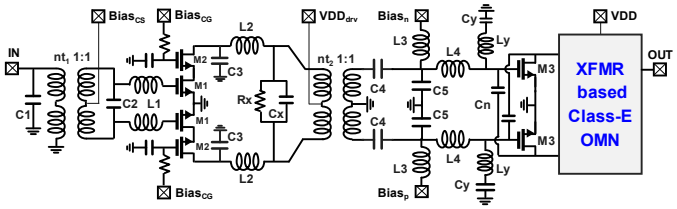

Fig. 6. Simplified schematic of the differential Class-E PA prototype.

The proposed differential Class-E PA is integrated as part of a fully-integrated Front-End Module (FEM) including a low-noise amplifier and an antenna switch, Fig. 7. The SOI chip is mounted using flip-chip assembly on a 4-Layer organic LGA package. The PA is measured on-board under $V_{dd} = 3.8$V and a quiescent current $I_{dq} = 70$mA. The measured performances are extracted at the package reference plane.

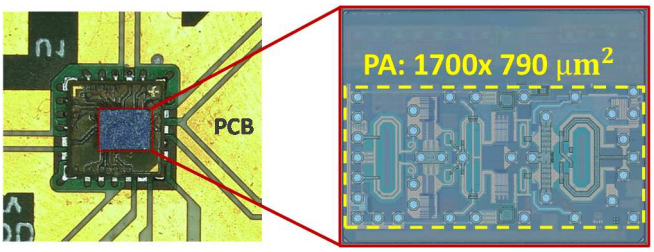

Fig. 7. Die and micrograph of the proposed differential Class-E PA.

The measured S-parameters and large-signal characteristics are shown in Fig. 8. The PA exhibits a small-signal power gain S_{21} higher than 21.5dB with less than -

10dB of input return loss S_{11} from 5.1 to 6.6GHz, Fig. 8-(a). Moreover, it achieves an output-referred 1dB-compression power (OP_{1dB}) higher than 26.5dBm, a saturated output power (P_{sat}) higher than 27.8dBm with a peak PAE ranging from 32% to 39.5% across the 5.1-6.6GHz band, Fig. 8- (b) and (c). In addition, the third-order intermodulation distortion (IMD3) measured with 1MHz two-tone spacing is lower than -35dB up to 21dBm, Fig. 8-(d).

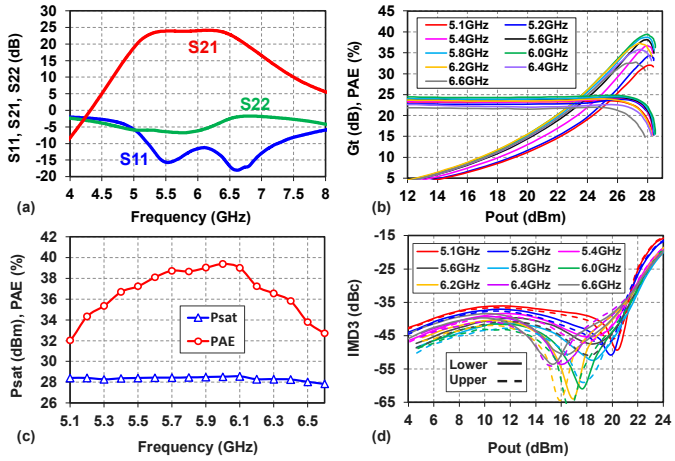

Fig. 8. Measured, (a) S-Parameters, (b) CW G_t and PAE versus P_{out}, (d) peak PAE and P_{sat}, (d) IMD3 from 5.1 to 6.6GHz.

The PA was also measured using 80MHz MCS11 1024QAM 802.11ax signal with digital pre-distortion (DPD). As shown in Fig. 9 (a) and (b), the PA delivers 18.75-19.7dBm of linear output power with an EVM of −42dB with 140-184mA of I_{dd} over the 5.1 to 6.6GHz frequency band. The output spectrum and I/Q constellation are measured at 5.6GHz for P_{out} = 19.5dBm and depicted in Fig. 9 (c) and (d).

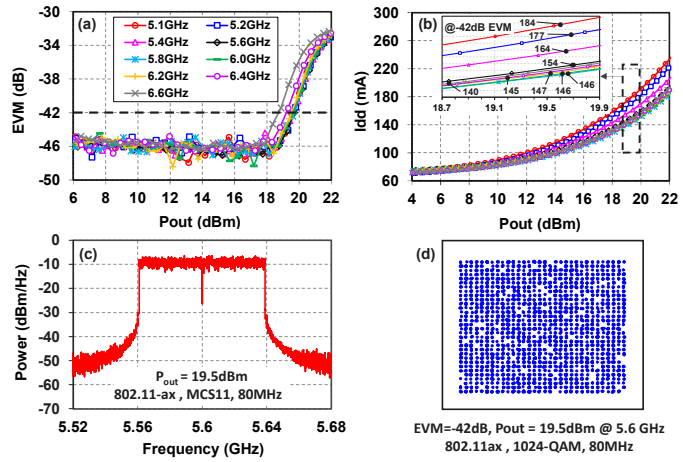

Fig. 9. Performances measured using 80MHz MCS11 802.11ax signal, (a) EVM, (b) I_{dd} versus P_{out} from 5.1 to 6.6GHz, (c) output spectrum and (d) I/Q constellation at 5.6GHz for P_{out} = 19.5dBm.

TABLE II shows a performance comparison with state-of-the-art CMOS [9]-[10], SiGe [11] and GaAs [12] PAs for 5/6GHz Wi-Fi applications. The proposed PA achieves wider operating band with lower power consumption and competitive size. Further optimization of the output and interstage matching is required to achieve the 5-7GHz.

TABLE II. PERFORMANCE COMPARISON.

	MWCL23 [9]	ISSCC17 [10]	JSSC20 [11]	MWTL23 [12]	This Work
PA Architecture	Differential w. Linearizer	Two-chip Doherty	Differential w. 2nd HT	Differential CM Class-F	**Differential Class-E**
Technology	CMOS 180nm	CMOS 55nm + SOI 180nm	SiGe 350nm	GaAs	**CMOS-SOI 130nm**
Freq. (GHz)	5.1 – 6.1	5.1 – 5.9	5.2 – 5.9	5.15 – 6.425	**5.1 – 6.6**
Supply (V)	3.3	3.3	5.0	5.0	**3.8**
Psat (dBm)	30.1	28.5	33	29	**27.8 – 28.5**
Peak PAE (%)	18	*NA*	35.5	35	**32 – 39.5**
MCS /BW(MHz)	MCS9 / 80	MCS9 / 160	MCS7 / 80	MCS11 / 80	**MCS11 / 80**
EVM (dB)	-32	-38	-38 **	-40 **	**-42**
Pout (dBm)	18.8 @5.3GHz	18 @5.8GHz	17 – 21.5 * @5.2-5.85GHz	18 – 20 @5.1-6.4GHz	**18.8 – 19.7 @5.1-6.6GHz**
Idd (mA)	384	191	286 – 353 *	204 – 221	**140 – 184**
Chip size (mm)	2.3x1.3	2.0x0.58 + 1.9x0.76	1.45 x 1.4	1.6x0.8	**1.7x0.79**

*Graphically estimated **Without DPD

CONCLUSION

We presented a design methodology utilizing a novel scalable transformer-based OMN synthesis approach to realize a wideband, fully-integrated differential Class-E PA. The design methodology was demonstrated on a fully-integrated 130nm CMOS-SOI PA addressing the Wi-Fi 6 bands. From 5.1 to 6.6GHz, the proposed PA delivers up to 19.7dBm of average output power with an EVM of -42dB using 80MHz 1024-QAM 802.11ax signal with DPD.

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