Including Package-Induced Mechanical Stress in Bandgap Reference Circuit Design

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Abstract— **Package-induced mechanical stress on the silicon die causes piezoelectric changes in the performances of integrated circuits, leading to significant inaccuracy in high-precision analog circuits. This work presents a design flow for predicting the package-related stress drift using the example of a bandgap voltage reference (BGR). Stress measurements in plastic QFN packages are combined with the piezoresistive sensitivity of semiconductor devices in the circuit. The data is used for a blind trim at wafer-level to compensate for package stress after chip and PCB assembly and its relative temperature change during chip operation. The developed stress models were implemented in Verilog-A and can easily be included in the circuit simulator to consider package stress in the design phase.**

I. Introduction

Die encapsulation materials in packaging typically consist of plastics or ceramics with thermal expansion coefficients and elastic properties different from silicon, the copper lead frame, and the epoxy die-attach (Fig. 1). This results in material strain when cooling down after the chip assembly and soldering process [1]. Additionally, mechanical stress in the package changes under varying temperature and humidity conditions due to mold expansion, moisture absorption, and mechanical aging of the chip package [2], [3]. Package-induced stress impacts the performance of integrated circuits. E.g., stress effects in bandgap references (BGRs) have been proven to be the predominant reference voltage error (several mV's) [4], [5], which is more than the statistical errors in trimmed state-of-the-art BGRs. In [4], the stress drift of a BGR has been measured based on three-point bending, not including out-of-plane normal stress σ'_{zz}. A BGR with an internal stress sensor and digital compensation has been proposed in [5], leading to a precise but large and complex system. Therefore, a typical BGR has been designed in this work to demonstrate the new capabilities of the stress models: stress drifts in a package compared to wafer-level measurements can be predicted by the model, and no additional silicon area is required for trimming. Further, the proposed methodology can be transferred to all kinds of analog stress-sensitive circuits. Fig. 2 shows the mathematical description of the anisotropic silicon resistivity $\vec{\rho}$ in dependence of the isotropic resistivity ρ_0, the piezoresistive coefficients π, and mechanical stress $\vec{\sigma}$. Combining the measurements of package stress in [3] with the stress sensitivity of the integrated circuit components of the PDK enables reliable prediction of stress-dependent electrical performances during schematic and layout design.

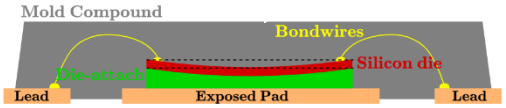

Fig. 1. Conceptional view of the chip package with different thermal coefficients of die, die-attach, and mold compound causing die stress.

II. Circuit Implementation

The circuit topology of the BGR designed for demonstration purposes is similar to state-of-the-art high-precision references and shows comparable performance as in [6]. Fig. 3(a) shows the simplified schematic: two vertical bipolar transistors (BJTs) generate PTAT and CTAT components. The voltage V_{BE1} is buffered and can be measured externally for stress and temperature monitoring. The OTA in Fig. 3(b) provides switches to swap the input differential pair, the current sources, and the current mirror load (mainly causing the offset). After swapping, the offset is inverted, calculated at the BGR output V_{BG} and trimmed at the input differential pair (coarse trim) and the degeneration resistor R_{SRC} (fine), followed by a blind trim of $R_{1,trim}$ for temperature effects (derived once from characterization values avoiding two temperature tests). Finally, V_{BG} is set ($R_{3,trim}$) to 1.24 V. Fig. 4 shows the chip view. The accuracy of 5 samples is depicted in Figs. 5(a) and 5(b).

III. Package Stress and Stress Sensitivity

To model the stress drift of V_{BG}, first, the piezoelectric characteristic (the stress sensitivity) of the individual semiconductor devices has to be known. It strongly depends on doping concentration [7], which is typically non-disclosed by foundries. Thus, the p-type resistors and BJTs used in the BGR core have been characterized in a three-point bending setup as in [8]. Fig. 6(a) shows the test rig, Fig. 6(b) the sili-

$$\begin{bmatrix}\rho_{xx}\\ \rho_{yy}\\ \rho_{zz}\\ \rho_{yz}\\ \rho_{xz}\\ \rho_{xy}\end{bmatrix} = \begin{bmatrix}\rho_0\\ \rho_0\\ \rho_0\\ 0\\ 0\\ 0\end{bmatrix} + \boldsymbol{\rho_0} \begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix} \begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{xz}\\ \sigma_{xy}\end{bmatrix}$$

Fig. 2. Tensor describing the change of isotropic silicon resistivity ρ_0 in dependence of the piezoresistive coefficients π and mechanical stress $\vec{\sigma}$.

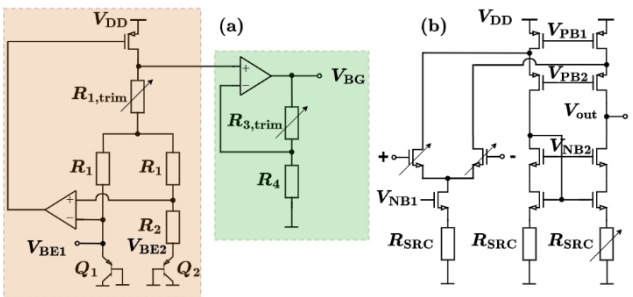

Fig. 3. (a) Simplified schematic view of the bandgap reference, and (b) transistor-level implementation of the OTA for temperature regulation.

con stripe with stress test structures, and Fig. 6(c) the bond wires between silicon and PCB for electrical connection. Figs. 6(d) and 6(e) depict the measured stress sensitivities. The piezo-junction effect shows slight dependence on the bias current, as reported in [4]. Second, the package-related stress on the die at the circuit position is required. Spatial information on mechanical stress has been measured in a prior publication [3]. To be able to precisely map the stress patterns, the BGR chip has the same edge length (1.4 mm) and thickness (300 μm) as the stress-sensing IC in [3]. The QFN packages used in [3] and this work are identical and from the same supplier. The normal stresses σ'_{xx}, σ'_{yy} and σ'_{zz} close to Q_1, Q_2, R_1, and R_2 (Fig. 3(a)) over temperature can be seen in Fig. 7(c). Figs. 7(d) and 7(e) show the spatial distribution of in-plane normal stress. Shear stress (particularly in the chip center) is small [3] and neglected in this work.

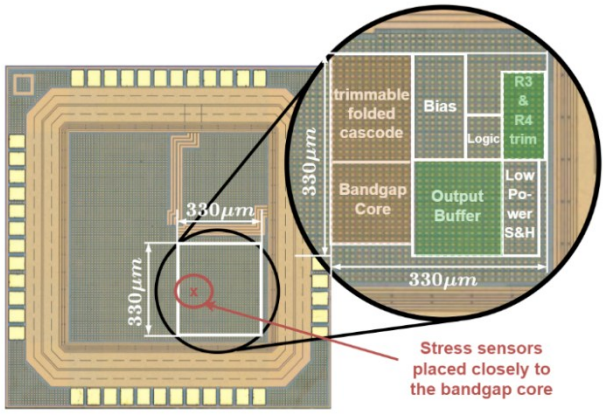

Fig. 4. Chip view of the silicon die before packaging and location of the BGR circuit blocks. The point marked by x (red) shows the location of the closest stress sensor (mapped from the stress-sensing chip in [3]) to the BJTs.

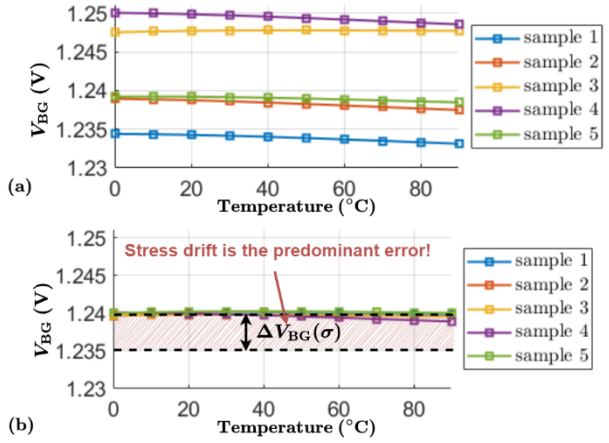

Fig. 5. Accuracy of the reference voltage V_{BG} over temperature (5 samples) (a) before and (b) after trimming. The typical range of package stress drift is also highlighted for reference.

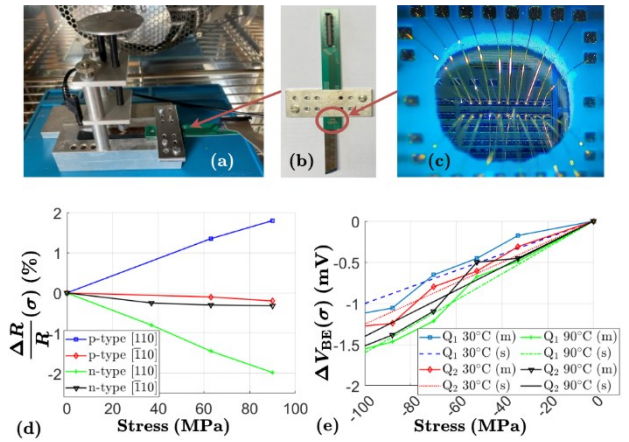

Fig. 6. (a) Test rig for stress characterization of circuit devices, (b) metal clamp with PCB and silicon stripe used as a cantilever, (c) bond wires between the die and the PCB. Stress drift w.r.t σ'_{xx} for (d) p-poly and n-diffusion resistors, and (e) BJTs in same operating point as in the bandgap core (m = measurement, s = simulation).

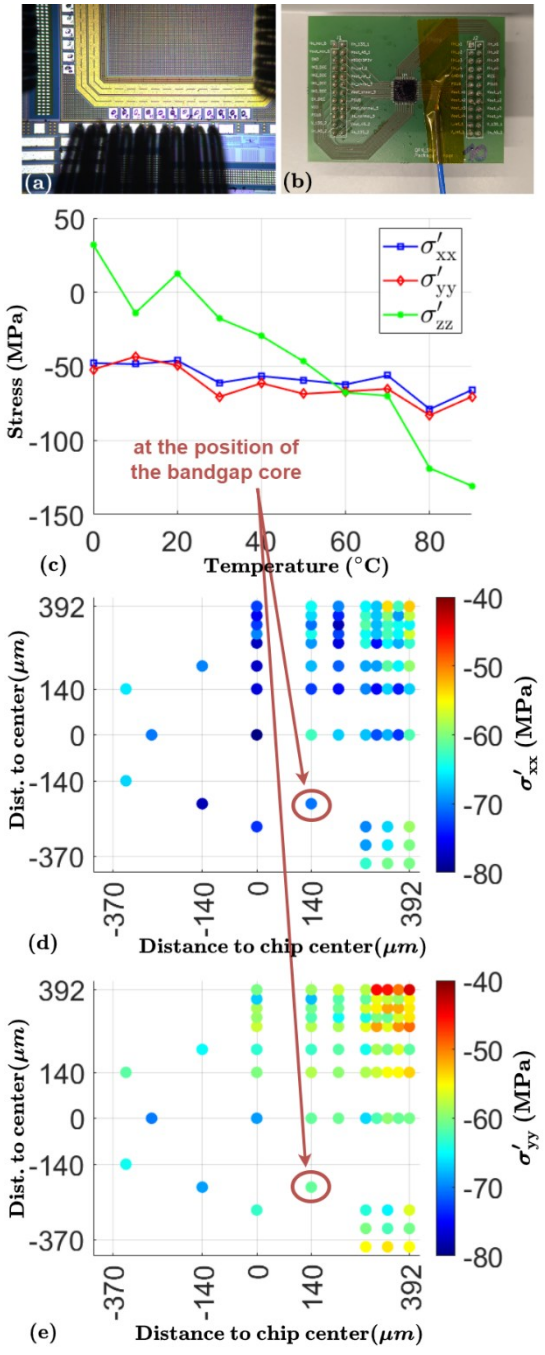

Fig. 7. (a) Wafer-level characterization of BGR at T = 30 °C and T = 90 °C with probe card needles serving as stress-free reference measurement, (b) QFN package containing the bandgap reference on PCB shield, (c) measured normal stresses σ'_{xx}, σ'_{yy} and σ'_{zz} at the position of the bandgap core after soldering on the PCB, (d) spatial distribution of σ'_{xx}, and (e) σ'_{yy} over the stress-sensing chip after soldering on the PCB [3].

IV. MODELING PACKAGE-INDUCED BGR DRIFT

First, the BGRs were measured at wafer-level on a probe station (stress-free reference), as can be seen in Fig. 7(a). Afterward, the ICs were packaged (QFN) while being traced for identification and soldered on PCB shields. The packaged ICs were then measured again in a climate chamber at precisely controlled temperature and humidity. Temperature gradients between the probe station and the climate chamber were compensated with an external temperature sensor (Fig. 7(b)). Figs. 8(a) and 8(c) show a constant stress-induced offset of V_{BG} for T=30 °C and its temperature drift at T=90 °C, which can be included as blind trim in wafer-level trim routines. Note that the stress drift was obtained from untrimmed BGRs and can be superimposed on the circuit since it is independent of trim values. The measurement of V_{BE1} in Figs. 8(b) and 8(d) not only serves for temperature monitoring but is also required for modeling: whereas common bending setups are able to apply in-plane normal stresses σ'_{xx} and σ'_{yy}, they can not adjust σ'_{zz}. This is sufficient to fully characterize the 3D stress sensitivity of lateral devices with direction of current flow in the wafer plane since stress can be applied in parallel and perpendicular to the current during bending. For BJTs with vertical current flow, however, out-of-plane normal stress σ'_{zz} (parallel to the direction of current) has to be considered for complete characterization as in-plane normal stresses are all perpendicular to the current. Thus, σ'_{zz} known from the chip package measurements in [3] is used for calibration of the piezo-junction model via V_{BE1}. The stress-related device characterizations have been implemented in Verilog-A models and can be used to simulate the overall circuit's stress drift during circuit design. Although the piezoresistive and piezo-junction effects are reported with (weak) second-order effects in [4], Figs. 6(d) and 6(e) indicate a linear characteristic up to +/-100 MPa. Fig. 9(a) shows the coordinate system including silicon crystal alignment and normal stresses, Fig. 9(b) illustrates the concept of the Verilog-A models used to simulate the stress dependencies of Q_1, Q_2, R_1, and R_2. Their impact on the overall stress drift of V_{BG} is listed in TABLE I. The OTA regulates stress effects on the PMOS current source in the core. The loop gain of the amplifier is set by resistors. They are arranged in cross-coupled pairs to average out stress gradients. Therefore, the resistor ratio is stress-independent. Stress effects on the MOSFETs have the same impact on both amplifier current branches and slightly change the open loop gain, leading to a negligible stress-dependent finite gain error. Fig. 10(a) illustrates the predicted stress drift of V_{BG} matching the measurement with a maximum error of 1.4 mV. This corresponds to a 0.1% error on V_{BG} and a 3x reduction of the package-induced stress drift, which is a dominant reference voltage error. Stress drifts resulting from material aging have been evaluated after 300 thermal cycles between T = -40 °C and T = 145 °C with an exposure time of 30 min each as specified in IEC 60068-2-14 Test Na. According to [3] package aging saturates after ~100 thermal cycles and the package stress can be considered static. Fig. 10(b) shows the difference of V_{BG} of 6 BGR samples before and after package aging measured at T=30 °C and T=90 °C. The deviation between new and aged packages is almost constant over temperature. Slight temperature dependence might result from material fatigue after the aging tests. The simulated aging drift was obtained with package aging stress drifts from [3]. Aging drifts barely depend on the position on the chip but are mainly statistically distributed. Therefore, the overall chip stress change was averaged to obtain the simulated data in Fig. 10(b), which explains the deviation of 2 aged BGR package samples. Stress effects caused by package aging can be accurately simulated for most samples with a maximum remaining error of 0.5 mV and can be included in wafer-level trim routines. TABLE II summarizes the performance

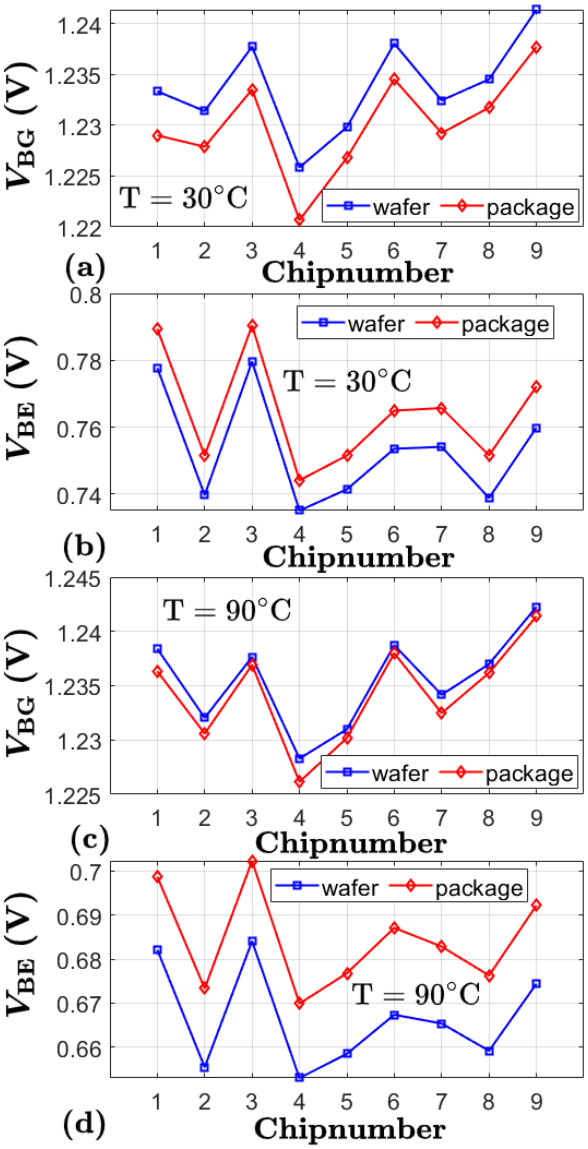

Fig. 8. (a) V_{BG} (untrimmed) and (b) V_{BE1} before and after packaging (9 samples) at T = 30 °C, and (c) and (d) at T = 90 °C.

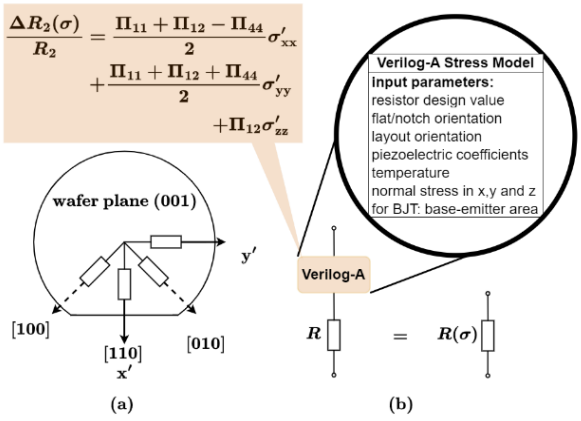

Fig. 9. (a) Wafer alignment and direction of normal stresses with respect to the silicon crystal axes, and (b) the concept behind Verilog-A modeling of the stress drift of the circuit components. The Verilog-A models add a stress-dependent voltage to the foundry model of resistors and BJTs.

improvements achieved in a BGR design using the proposed design flow: Compensating package effects in the trim routine keeps the additional silicon area at a minimum, leading to a compact design. All relevant stresses - normal stresses σ'_{xx}, σ'_{yy}, and σ'_{zz} - can be compensated for. This reduces the BGR error after packaging to a competitive value of 0.25%, including the 3σ circuit inaccuracy and the measured worst-case packaging drift.

TABLE I. IMPACT OF STRESS DRIFT ON CIRCUIT DEVICES.

device	impact on	mechanism	typ. value
Q_1	V_{BE1}	piezojunction effect	$\approx$ 10 mV
Q_1 and Q_2	$V_{BE1} - V_{BE2}$	bias dependence of piezoj. effect	$\approx$ 0.1 mV
R_2	$V_{BE1} - V_{BE2}$	piezoresistive effect	$\approx$ 0.1 mV
R_2	V_{BE1}	piezoresistice effect	$\approx$ 0.1 mV
OTA, $R_1/R_2, R_3/R_4$	V_{BG}	finite gain error, resistive divider	$\approx$ 0 mV

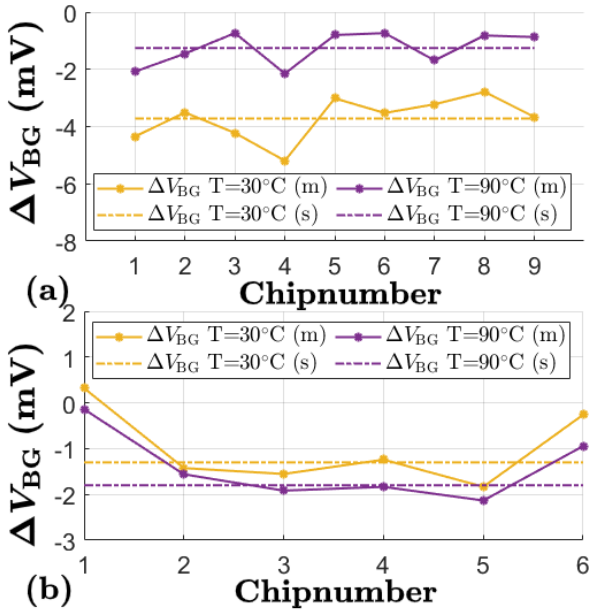

Fig. 10. (a) Simulated and measured relative drift of V_{BG} after packaging at T = 30 °C and T = 90 °C (m = measurement, s = simulation), and (b) simulated and measured relative drift of V_{BG} at T = 30 °C and T = 90 °C after package aging (m = measurement, s = simulation). Stress drifts of Q_1, Q_2, R_1, and R_2 have been included in simulations. The aging experiment comprised 300 cycles between T = -40 °C and T = 145 °C with 30 min exposure time according to IEC 60068-2-14 Test Na.

TABLE II. COMPARISON OF THE PROPOSED BGR DESIGN.

	This Work	VLSI'20 [9]	TCAS-I'17 [10]	ISSCC'15 [11]	JSSC'11 [6]
Technology (nm)	180 CMOS	180 CMOS	800 BiCMOS	130 CMOS	160 CMOS
Area (mm²)	0.11	0.38	0.28	0.034 (*)	0.12
Supply Voltage (V)	1.8 +/- 10%	1.8 +/- 10%	5.2	1.5 +/- 10%	1.8 +/- 10%
Reference Voltage (V)	1.24	1.1419	3.657	1.215	1.0875
Reference Inaccuracy (3σ)	+/- 0.25% incl. packaging	+ 0.02%, - 0.12%	N/A	+/- 0.08%	+/- 0.15%
Temp. Range (°C)	-55 to 110	-40 to 125	-40 to 110	-40 to 120	-40 to 125
Temp. Drift (ppm/°C)	7-13 box method	2.07	+/- 3	7	5-12 box method
PSRR (dB)	74 @ DC	76 @ DC	127 @ DC	N/A	74 @ DC
Power (μW)	20 core + 25 buffer	30.6	3900	N/A	99
Package stress compensation	3 normal stresses	-	-	2 in-plane stresses	-

(*) excluding ADC, digital core, temperature and stress sensors for stress compensation

V. CONCLUSION

Mechanical stress after packaging can result in significant performance drifts of high-precision analog circuits. The stress drift of a BGR as an example circuit, can be simulated with the proposed design flow. Additionally, the impact of package aging can be predicted. The resulting data can already be used during circuit design and layout, e.g., for a blind trim on wafer-level. The stress drift models can easily be included as Verilog-A-blocks in the circuit simulator. They combine piezoresistive sensitivity of the circuit device with the stress pattern in the IC package for precise simulation of circuit performance drifts.

ACKNOWLEDGMENT

This work is funded by the DFG (Deutsche Forschungsgemeinschaft) project STAMPS (BR 6306/1-1 and HI 2230/1-1) and the BMBF project VE-FIDES (16ME0527). We thank Roland Lange, Marco Lang and Thomas Grill from Continental for supporting the package material aging tests.

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