Two 5.6 mW Over-Neutralized 120 GHz Low-Noise Amplifiers in 14 nm FinFET CMOS

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***Abstract*—This paper presents two low noise amplifiers (LNAs) in 14 nm FinFET technology for D-band applications. FinFET transistors suffer from low gain at frequencies beyond 100 GHz. In addition, parasitic capacitance due to metal fill and high gate resistance makes it harder to design using this process at these frequencies. In this article, we present a device-centric design methodology. Additionally, the RC over-neutralization technique is employed to counteract the low device gain. Furthermore, we provide layout considerations, critical to tackle the parasitics associated with scaled FinFET processes and very high frequencies beyond 100 GHz. The proposed techniques and careful millimeter-wave layout have enabled achieving several metrics which advance the state-of-the-art. To the best of our knowledge, we report the lowest power consumption at 5.6 mW, and the lowest core area of 0.03 mm^2 for a D-band LNA. We report two LNA realizations, a narrowband LNA with 9 GHz bandwidth, 15.2 dB gain and 5.5 dB minimum measured noise figure (NF) and a 18 GHz wideband LNA with 12.7 dB gain and 5.8 dB minimum measured NF. To our knowledge, they are the first 14 nm FinFET LNAs at D-band in a commercially available technology.**

***Index Terms*—FinFET, narrowband, neutralization resistance, Low Noise Amplifier (LNA), Noise Figure (NF), wideband**

I. Introduction

The demand for ultra-high data rates, driven by applications such as augmented reality [1] and various emerging millimeter wave (mmWave) radar [2] use cases, is propelling interest in the D-band (110-170 GHz). This spectrum, with a wide available bandwidth, offers a promising last-mile solution for dense user areas or targeted deployments in stadiums, factories, and airports.

Although III/V and SiGe HBT technologies offer superior RF performance, bulk CMOS is commercially viable due to its low cost, higher integration, and compact footprint. Most of the reported RF circuits in FinFET are at low frequencies [3], with more recent work on mmWave circuits [4], [5], [6], realized in 16 nm or 22 nm FinFET. Very few RF circuits have been reported in 14 nm FinFET [7] and to the best of the authors knowledge, this is the first reported 14 nm FinFET LNA operating in the D-band.

A recent D-band LNA in 22 nm SOI [1], demonstrated high gain and bandwidth using a 0.8 V supply. The design in [5] employed an active balun input stage to lower the noise figure and staggered tuning to achieve a 24% fractional bandwidth. In [2], RC overneutralization using explicit resistors helped increase gain per stage. Building on these approaches, we propose a systematic methodology to bias and size devices for low-power operation and extend the RC overneutralization technique [8] to derive optimal RC values, while accounting for device parameters, routing resistance, and parasitic fill capacitance, impact of which increases significantly in advanced technology nodes. We introduce layout strategies that mitigate parasitics in FinFET processes at mmWave frequencies, enabling design of compact, low-power, and high-gain D-band LNAs.

II. LNA Design Methodology

A. Device sizing and DC operating point

The optimal gate bias voltage and gate length for the SLVT transistor with high f_{max} were determined using the Figure of Merit (FoM) introduced in [9], which maximizes gain-bandwidth product and is given by

$$\text{FoM} = f_T \frac{g_m}{I_D}. \tag{1}$$

Fig. 1 shows the lowest value of NF_{min} and the maximum value of the FoM at the minimum gate length (l_{min}) and gate voltage of 340 mV. This combination ensures high gain and low noise at low bias currents for the LNA.

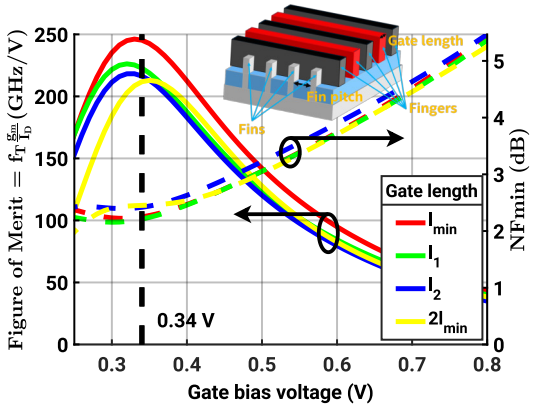
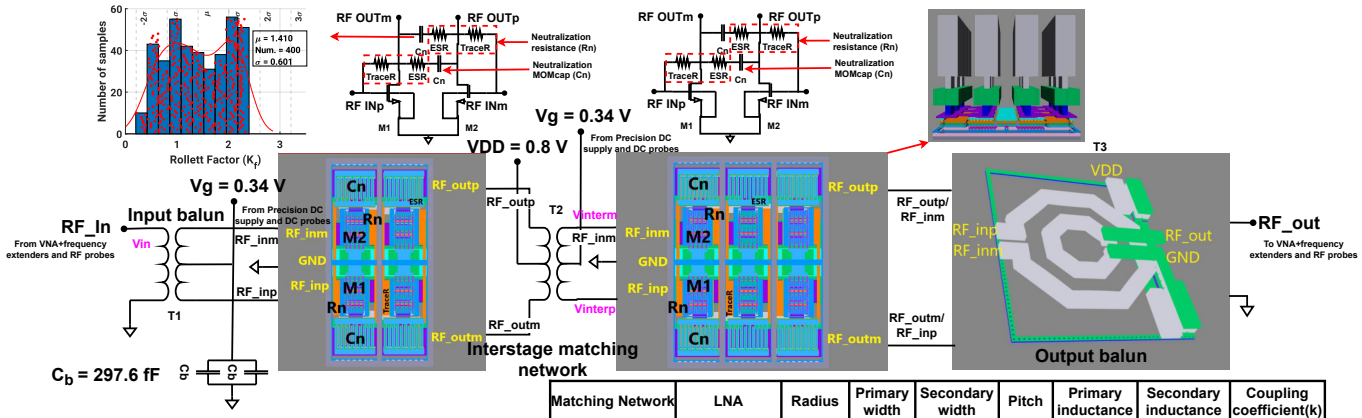


Fig. 1: Variation of FoM over gate bias voltage for different gate lengths ($l_{min} < l_1 < l_2 < 2l_{min}$) of FinFET transistor at 120 GHz.

FinFETs suffer from low gain at high frequencies and exhibit higher performance degradation with increasing transistor size compared to equally sized planar transistors [4]. To overcome this limitation and ensure a high f_{max}, small transistors with 4 fins and 8 fingers were chosen to realize individual unit cells of the neutralized differential pair (NDP).



Stage	Fins	Fingers	Gate length	Width	Cn / unit cell	Rn / unit cell
First stage (M1, M2)	4	8	14 nm	9.2 μm	3.38 fF	20
Second stage (M1, M2)	4	8	14 nm	13.8 μm	3.38 fF	20

Matching Network	LNA	Radius	Primary width	Secondary width	Pitch	Primary inductance	Secondary inductance	Coupling coefficient(k)
Input balun (T1)	Narrow and wide	37 μm	12 μm	4 μm	7 μm	186.2 pH	90.6 pH	0.54
Interstage (T2)	Narrowband	32 μm	3 μm	5 μm	10 μm	136 pH	60.5 pH	0.35
	Wideband	41 μm	3 μm	5 μm	14 μm	189.5 pH	84.4 pH	0.37
Output balun (T3)	Narrowband	35 μm	6 μm	8 μm	10 μm	124.6 pH	74 pH	0.36
	Wideband	36 μm	8 μm	8 μm	11 μm	120.6 pH	66.3 pH	0.37

Fig. 2: Schematic of neutralized differential pair.

B. Gain enhancement using lossy overneutralization

The neutralized differential pair, shown in Fig. 2, utilizes high Q MOM capacitors for capacitive neutralization (C_n). The inevitable equivalent series resistance (ESR) of these capacitor along with the parastic cross-coupled routing resistance (TraceR) are modeled as a neutralization resistance (R_n).

Lossy, capacitive over-neutralization [8] was used for LNAs in [2]. This gain enhancement technique decouples the dimensioning of C_n and R_n, enabling a wide range of suitable C_n-R_n combinations for neutralization. In this work, we identify an appropriate set for the LNA through a few simple steps:

- For a fixed device size, unconditional stability ($K_f > 1$) is achieved when C_n has a value between the two maxima of the G_{max}-C_n curve shown in Fig. 3a. Optimal neutralization for non-unilateral circuits is when C_n coincides with the peak of K_f ($K_{f,max}$). The ESR of the cross-coupled MOM capacitor imposes the lower limit on R_n.
- The G_{max} heat map on the C_n-R_n pre-layout plot from Fig. 3b, indicates that it predominantly peaks for C_n values beyond optimal neutralization [10], which we consider to be between the $K_{f,max}$ and $K_f = 1$ loci.
- Conversely, Fig. 3c, indicates (NF_{min}) is lowest for under-neutralized differential pairs, i.e. for values of C_n between $K_f = 1$ and $K_{f,max}$ loci respectively.
- A merit of single stage amplifier can be examined by looking at the term G_{max}/NF_{min} (the higher, the better). Friis formula helps extend this approach to multi-stage amplifiers assuming the same stage size. Thus, we define a match-independent FoM as

$$\text{FoM}_{\text{two-stage}} = \frac{G_{max}}{NF_{min} + \frac{NF_{min}-1}{G_{max}}}. \quad (2)$$

The G_{max} consideration precedes that of NF_{min} because a high gain stage of the amplifier would ensure an overall lower noise figure for a multi-stage amplifier.

- The $\text{FoM}_{\text{two-stage}}$ heat map on the C_n-R_n pre-layout plot, depicted in Fig. 3d, indicates the region in which the $\text{FoM}_{\text{stage}}$ is highest for the respective R_n and C_n pairs. Finally, accounting for stability and PVT variations including trace resistance tolerances, can help converging on an appropriate C_n-R_n pair for the LNA design.

Adopting this approach and accounting for parasitics due to metal fill and routing in post-layout, a 3.38 fF neutralization capacitor and 20 Ω neutralization resistance were realized.

C. Unit cell layout

To neutralize MOS transistors, with a small parasitic C_{gd} of few femtofarad, a correspondingly small neutralization capacitor is required. This can be realized using single-metal MOM capacitors, which are susceptible to PVT variations and modeling inaccuracies [11]. Their small footprint opens up spaces within the unit cell, which is occupied by metal

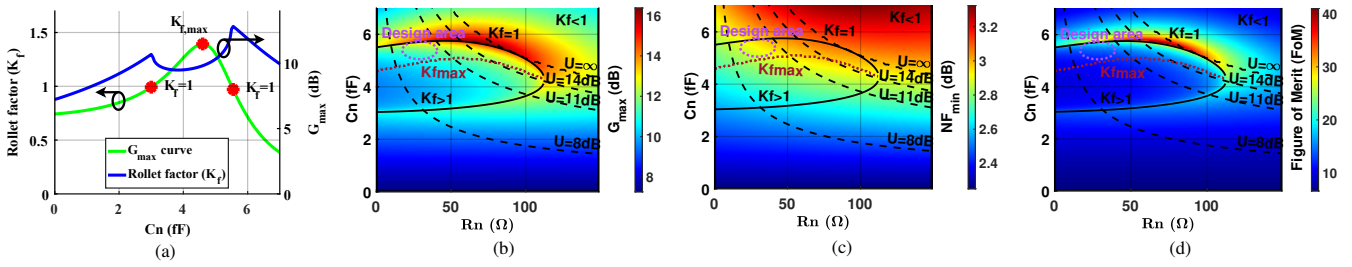
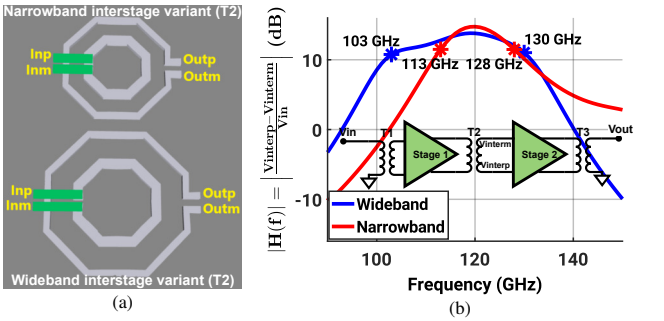


Fig. 3: (a) G_{max} and Rollett factor shown over C_n and variation of (b) G_{max} (c) NF_{min} and (d) $\text{FoM}_{\text{stage}}$ over the C_n-R_n pre-layout plot for the 9.2 μm wide neutralized differetnial pair at 120 GHz.

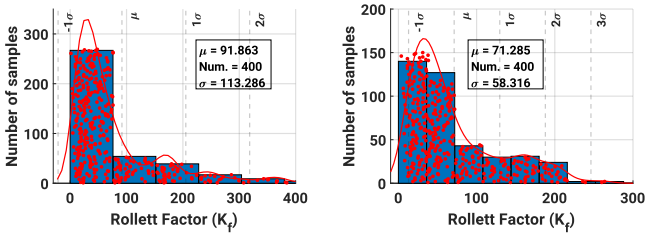


(a) (b)

Fig. 4: Interstage transformers (a) 3D model (b) simulated voltage transfer function from the input to the secondary side of T2.

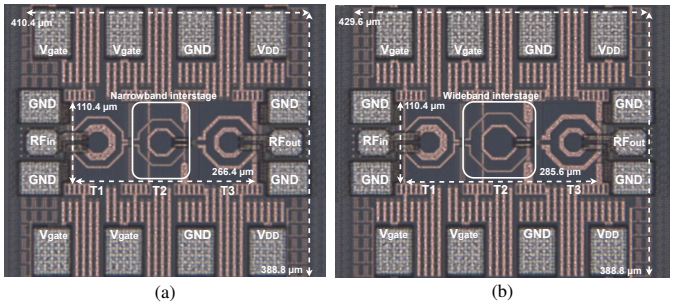
fill. This increases the parasitic capacitance of the amplifier and shifts the operating region of the neutralized amplifier, a phenomenon common in FinFET's at mmWave frequencies.

To combat these issues, an area efficient approach of tripling the number of transistors in parallel within a unit cell was adopted, as shown in Fig. 2. This helped reduce the unit cell count by 67%, lower inductive phase and amplitude imbalances [12], improve the power per unit area and modularity of the unit cell. The Miller capacitance per unit cell triples, which requires larger MOM capacitors realized between multiple metal layers for neutralization. Reduction in open spaces reduced the metal fill, improving control over parasitic capacitance within the amplifier. The impact of process and mismatch variations of the MOM capacitor on unit cell and LNA circuit stability was analyzed through a post-layout, 400 sample, global Monte Carlo (MC) simulation. The MC simulation in the top left of Fig. 2 shows the unit cell may be unstable due to variations in the 3.38 fF MOM capacitor. However, when the unit cell is matched using lossy transformers within the circuit, the MC simulation in Fig. 5 shows both LNA cores are unconditionally stable at 120 GHz.



(a) (b)

Fig. 5: Monte Carlo simulation for 3.38 fF MOM capacitor used in the amplifying stages of the (a) narrowband (NB) LNA (b) wideband (WB) LNA.



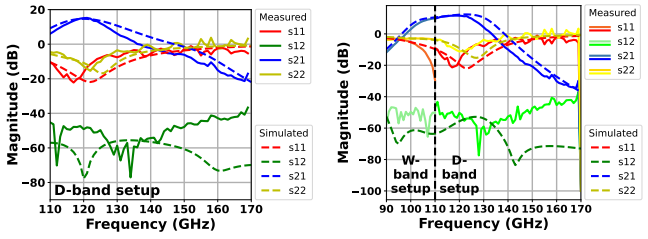
(a) (b)

Fig. 6: Chip microphotograph of (a) narrowband LNA (b) wideband LNA.

The small FinFET device in the unit cell has a large gate resistance of 92.8 Ω, due to their 3D structure, which also contributes to a NF_{min} of 2.27 dB at 120 GHz. Thin metal layer connections add resistance to the extrinsic transistor network, increasing the NF. A multi-tiered parasitic extraction and electromagnetic simulation approach ensured that parasitics due to routing, metal fill, and due to the matching networks were captured accurately and absorbed into the design approach.

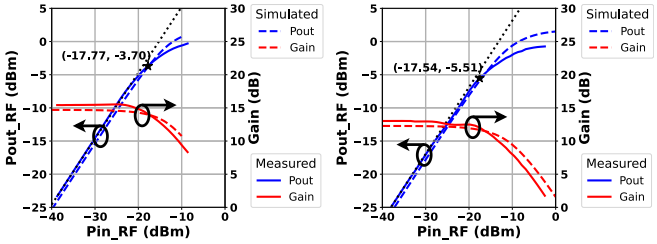
D. Transformer-based matching networks

In this work, we use a single-metal, 1:1 spiral interleaved transformer [13] for the matching networks. A parametric cell of the interleaved transformer is optimized through an EM simulation procedure that maximizes the transducer power gain [14]. Capacitors are connected to the secondary centre-tap of the input balun for broadband balance compensation [15] and vice versa for the output balun. The narrowband interstage transformer has a primary and secondary inductance of 136 pH and 60.5 pH respectively. On the other hand, the inductances of the wideband interstage transformer is 189.5 pH and 84.4 pH at the primary and secondary, respectively. Both transformers have a similar coupling coefficient of around 0.36. Fig. 4a and Fig. 6 show the geometric differences between the matching networks. Fig. 4b shows the 27 GHz wideband response and 15 GHz narrowband response of the LNAs.



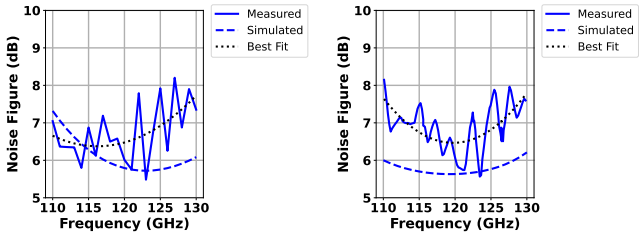
(a) (b)

Fig. 7: Measured and simulated S-parameters of (a) NB LNA (b) WB LNA.



(a) (b)

Fig. 8: Measured and simulated large signal parameters of (a) NB LNA (b) WB LNA.



(a) (b)

Fig. 9: Measured and simulated noise figure of (a) NB LNA (b) WB LNA.

TABLE I: Comparison and performance summary of D-band LNA's

Ref.	Tech.	Top.	f_0 (GHz)	Gain (dB)	Min. meas. NF (dB)	Avg. NF (dB)	BW (GHz)	Pdc (mW)	IP_{1dB} (dBm)	Core Area (mm^2)	FoM*	FoM_{AB}**
Narrowband	14 nm FinFET	Diff.	120	15.2	5.5	6.5	9	5.6	-17.8	0.03	4.62	11.55
Wideband	14 nm FinFET	Diff.	120	12.7	5.8	6.5	18	5.6	-17.5	0.03	2.53	12.66
[1]	22 nm SOI	Diff.	130	17	6.5	≤ 8	24.8	60	-19	0.13	0.39	0.58
[2]	28 nm CMOS	Diff.	120	13.3	5.6	≤ 7	15	25.2	-17.3	0.03	0.72	3
[5]	16 nm FinFET	Diff.	200	12	8.3	≤ 9	48	28	-12.4	0.06	1.13	4.52

* $\text{FoM} = \frac{\text{Gain(lin.)}\cdot \text{IP}_{1dB}\,(\text{mW})\cdot f_0\,(\text{GHz})}{(\text{NF}_{\min}\,(\text{lin.})-1)\cdot \text{P}_{dc}\,(\text{mW})}$ ** $\text{FoM}_{AB} = \frac{\text{Gain(lin.)}\cdot \text{IP}_{1dB}\,(\text{mW})\cdot \text{BW(GHz)}}{(\text{NF}_{\min}\,(\text{lin.})-1)\cdot \text{P}_{dc}\,(\text{mW})\cdot \text{CoreArea}(\text{mm}^2)}$, where A=Core Area ($mm^2$) and B=Bandwidth (GHz).

III. Measurement Results

The narrowband and wideband LNAs occupy an area of 0.159 mm^2 and 0.167 mm^2, respectively, yet having a similar core area of 0.03 mm^2. Both LNAs are driven by a 0.8 V supply and have a very low measured power consumption of 5.6 mW.

The D-band setup comprising Rohde and Schwarz ZNA67, Vertigo Technologies Active loadpull setup, Infinity waveguide D-band probes, and VDI WR6.5 frequency extenders was used for S-parameter and large signal measurements. Additionally, the W-band setup consisting of Keysight PNA-X and Agilent W-band frequency extenders were used for the wideband LNA S-parameter measurements.

The measured and simulated results for both LNAs exhibit good correlation, as seen in Fig. 7. The peak measured gain for the narrow and wide band LNA are 15.2 dB at 121 GHz and 12.7 dB at 119 GHz, respectively. The output 1 dB compression of the narrow and wideband LNAs are -3.7 dBm and -5.5 dBm, respectively, both of which are shown in Fig. 8. The system shown in Fig. 10 was used for Y-factor noise figure measurements. The average in-band noise figure of the amplifiers was 6.5 dB at 120 GHz, as seen in Fig. 9. The variability in noise figure measurements can be attributed to the difficulty in doing on-wafer noise figure measurements [16].

Table I summarizes the performance of the LNA in this work and compares it to other state-of-the-art LNAs operating at D-band and G-band frequencies.

IV. Conclusion

This paper presented a D-band LNA in 14 nm FinFET technology. The proposed device-centric and layout methodology along with lossy RC overneutralization resulted in the design of two LNAs exceeding the state of the art. The narrowband LNA has a 9 GHz bandwidth, 15.2 dB gain and 5.5 dB NF and a wideband LNA with an 18 GHz bandwidth, 12.7 dB gain with 5.8 dB NF.

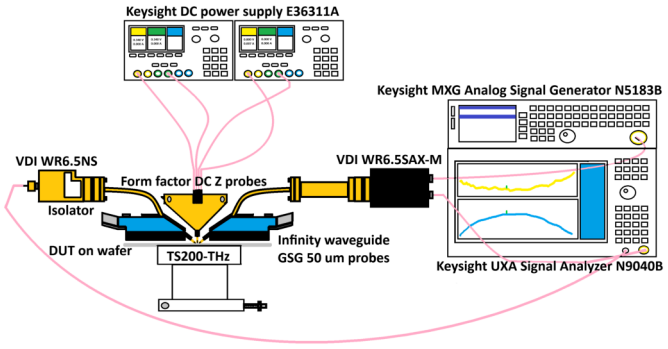


Fig. 10: D-band on-wafer Noise Figure measurement setup.

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