Total Energy Minimization of Duty-Cycled, Multi-V_{dd} SoCs with Execution-Time Guarantees

Chi-Hsiang Huang, Kevin Patiño Sosa, Arindam Mandal, Julian Arenas,
Diego Peña-Colaiocco, and Visvesh S. Sathe
School of Electrical and Computer Engineering, Georgia Institute of Technology
Atlanta, USA
Email: chuang464@gatech.edu

***Abstract*—Existing Minimum Energy Point (MEP) tracking architectures are limited to tuning the supply-voltage (V_{dd}) of a single domain, and minimize energy only during active computation. However, these architectures are ill-suited to practical ultra-low power SoCs which employ multiple V_{dd} domains, and duty-cycle their operation: performing tasks during brief intervals (*Run*) between long durations in a powered-down low-leakage state (*Sleep*). This paper presents an MEP tracking architecture that minimizes total energy consumption for a multi-V_{dd}, duty-cycled SoC executing evolving, time-bound tasks across power cycles. Measurements on a 65nm CMOS SoC test chip demonstrate that the approach achieves a 1.43× energy reduction over state-of-the-art MEP tracking.**

***Index Terms*—minimum energy point (MEP), constrained optimization, voltage regulator, multi-domain, duty-cycling**

I. Introduction

Existing MEP tracking techniques dynamically adjust the digital domain V_{dd} to balance workload-dependent switching losses, and PVT-dependent leakage losses [1]–[6] to operate at an energy-optimal setting (V_{mep}). Recent studies incorporate losses in the voltage converter and regulator to minimize the total energy drawn from a power supply (E_{IN}) at execution time [2]–[5], with some providing minimum clock frequency guarantees (f_{clk}). However, previous work on single-variable V_{dd} optimization restricts the search space (Fig. 1a), leading to suboptimal energy efficiency. In contrast, independently tuning each domain i to $V_{\mathrm{dd,i}}$ allows finding an optimal configuration with distinct $V_{\mathrm{dd,i}}$ values. Furthermore, current techniques that aim to minimize energy-per-cycle during execution neglect the significant V_{mep}-lowering effect of *Sleep* mode. The energy losses incurred in *Sleep* are drawn during *Wake* as the supply charges domains back to their respective V_{dd} values [5]. Thus, minimizing total energy across the entire power cycle spanning *Sleep*, *Wake*, and *Run* states, while also guaranteeing task execution time ($T_{\mathrm{run}} \leq T_{\mathrm{run,max}}$), is crucial (Fig. 1b). Finally, MEP tracking bandwidth limits E_{IN} minimization. SoC tasks and program flows can vary abruptly from one power cycle to the next. However, current tracking needs multiple *Run* iterations to converge and cannot track these abrupt MEP changes (Fig. 1c). The architecture described in this paper performs multi-V_{dd} tracking to minimize E_{IN} over a complete power cycle with execution time guarantees under constantly evolving SoC tasks.

This work was supported by SRC under GRC task 3160.026

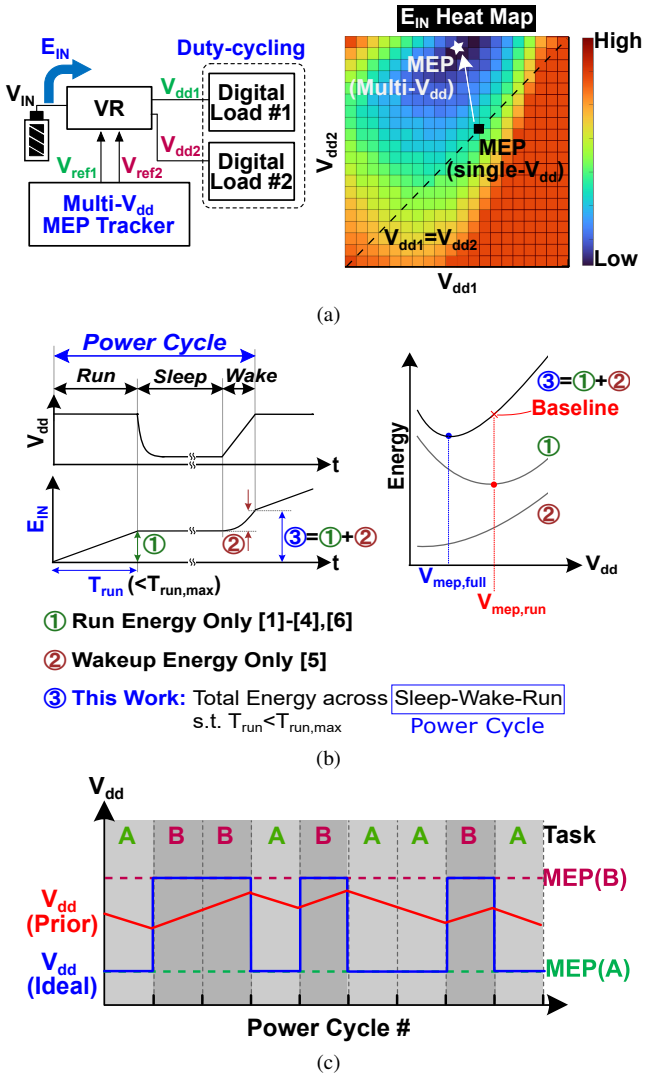


Fig. 1. Key elements of effective MEP tracking. (a) Lower E_{IN} via multivariate V_{dd} tuning in a 2-domain SoC vs. conventional single-variable tuning. (b) Tracking E_{IN} across the full power cycle reveals a lower MEP than *Run*-only approaches. (c) MEP varies with task; the proposed method enables fast, task-aware context switching, in contrast to conventional techniques.

II. Architecture and Implementation

A. Multi-V_{dd} tuning and regulation

Fig. 2 shows an overview of the system. A single-inductor-multiple-output (SIMO) converter provides compact, domain-scalable, and energy-efficient V_{dd} regulation of multiple SoC domains. Domains $V_{dd,core}$ and $V_{dd,acc}$ are clocked with a tunable replica oscillator (TRO) that modulates f_{clk} with V_{dd} [7] to maintain correct functionality. The MEP tracker measures E_{IN} and adjusts $V_{dd,core}$ and $V_{dd,acc}$ to minimize energy while ensuring $T_{run} \leq T_{run,max}$. E_{IN} minimization is performed across an entire power-cycle, accounting for all losses incurred in the system: both spatially (regulator and loads) and temporally (across *Sleep*, *Run* and *Wake*). Switching activities and core-accelerator data dependencies, and therefore MEPs, are highly task-dependent. Task-based tracking is performed to maintain MEP operation despite frequent changes in SoC tasks in each new power cycle. The *Power State Controller* sets the duty cycle and timing of each of the switches in the system.

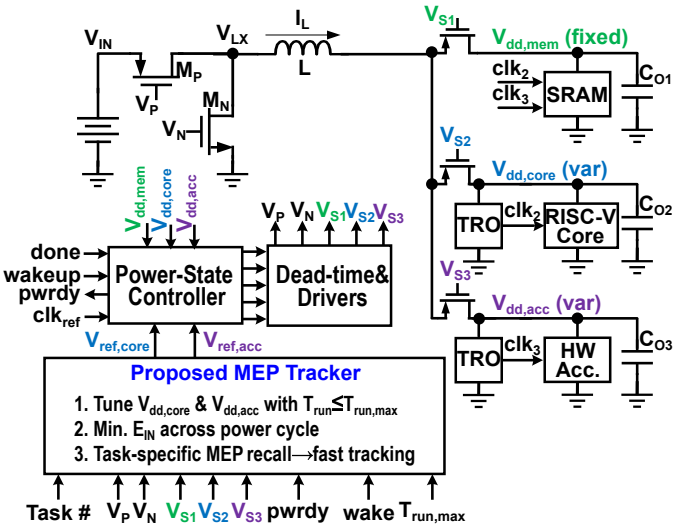


Fig. 2. Overall architecture of the SIMO-regulated SoC for total energy minimization.

B. Cross-task MEP tracking under $T_{run} < T_{run,max}$ constraints

Fig. 3 describes the E_{IN} descent operation by the *MEP tracker*. Descent occurs in two phases: *Dirn. Search* and *Move*. In *Dirn. Search*, the controller measures E_{IN} over eight directions in the vicinity of the current MEP to identify the steepest legal descent direction ($T_{run} < T_{run,max} - \Delta$) before transitioning to the *Move* phase during which $V_{dd,i}$ values are incrementally adjusted every new power cycle to move in the steepest descent direction until either increases or $T_{run} \geq T_{run,max} - \Delta$. The controller then enters *Dirn. Search* to find a new descent direction.

The *MEP Tracker* is designed to support simultaneous multi-task MEP tracking despite bandwidth limitations inherent in gradient descent tracking (Fig. 1c). Fig. 4 outlines the

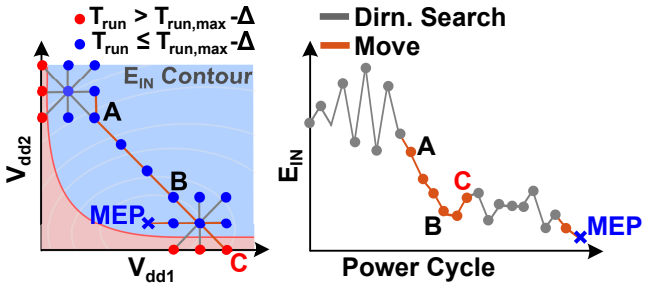


Fig. 3. The Gradient Descent algorithm transitions $V_{dd,i}$ through a sequence of successive *Search* and *Move* phases.

organization of the tracker. At the beginning of each new power cycle, the E_{IN}-*Measure* module first measures E_{IN} over the preceding cycle. If the task for the current cycle differs from the previous one, the *Tracker* stores task-specific state variables — including E_{IN}, $V_{dd,i}$, and descent-phase — in the Task Context Memory (*TCM*). Subsequently, it loads the state variables for the present task from the *TCM* and verifies if the previously stored execution instance finished within a user-defined margin (Δ): $T_{run} \leq T_{run,max} - \Delta$. The tracker deems any $V_{dd,i}$ assignment that lies within Δ of $T_{run,max}$ to be too close to failure and therefore unsuitable for MEP exploration. Otherwise, the descent algorithm uses the assignment to calculate subsequent $V_{dd,i}$ traversals. The *TCM* thus supports simultaneous task-specific MEP tracking by the optimizer.

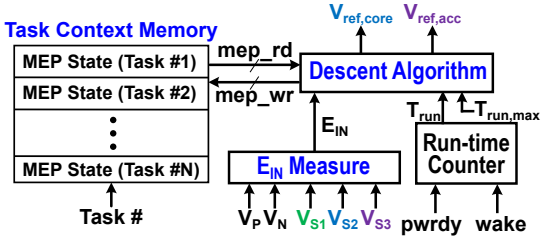
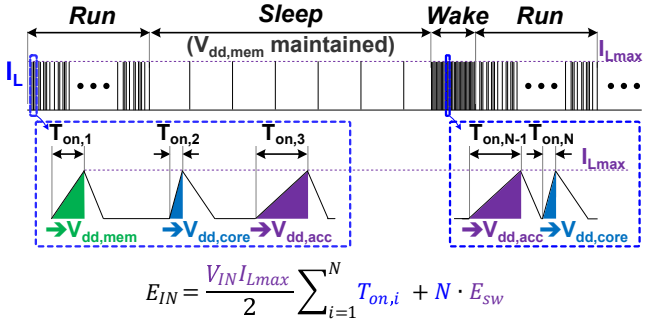


Fig. 4. Proposed MEP tracker. The descent algorithm relies on E_{IN} measurements and a *Task Context Memory* to indpendently guide MEP tracking across various tasks.

To determine full power cycle-wide E_{IN}, the E_{IN} *Measure* module calculates the total charge draw from the SIMO converter. The constant-current Pulse-Frequency Modulation (PFM) scheme, typical in low-power regulators (Fig. 5), simplifies this calculation, as the charge is proportional to the total high-side bridge driver on-times ($\Sigma T_{on,i}$) during the power cycle. This measurement accounts for SIMO conduction, SoC switching, and SoC leakage losses. SIMO converter switching losses are obtained by tracking bridge driver transitions within the power cycle, and scaling them by the energy loss per transition. The module then combines these two loss components to obtain E_{IN}.

III. Measurement Results

A test-chip presenting the proposed architecture was fabricated in a 65nm CMOS process and its die photograph



$$E_{IN} = \frac{V_{IN} I_{Lmax}}{2} \sum_{i=1}^{N} T_{on,i} + N \cdot E_{sw}$$

Fig. 5. SIMO inductor current (I_{L}) over a power cycle. Shaded regions indicate durations of charge delivery from the supply to the regulator.

is shown in Fig.6. It includes a RISC-V processor, multiple hardware accelerators, and an SRAM. MEP tracking circuits present a 1.75% area overhead and a 0.35% energy overhead to the system. Measurements are reported for a power-cycle period (T_{PC}) of 30ms; however, the design does not impose any constraints on T_{PC}. RISC-V program execution — its control flow including function calls and serial-parallel dependencies between processor and accelerators – dictates both T_{run} and the MEP-optimal $V_{\mathrm{dd,i}}$ configuration. A synthetic load is included in each domain to emulate various loading scenarios. $V_{\mathrm{dd,mem}}$ is fixed at 0.6V, while $V_{\mathrm{dd,core}}$ and $V_{\mathrm{dd,acc}}$ are dynamically tunable between 0.36V and 0.6V.

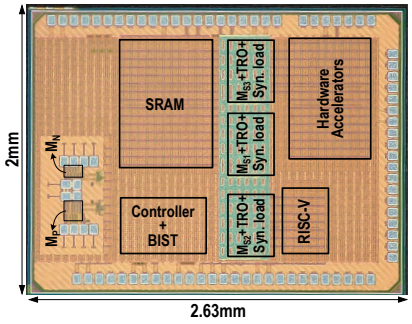


Fig. 6. Test-chip die photograph.

Fig. 7 shows the measured operation of the proposed system over a complete power cycle. A simplified version of domain-charge recycling is adopted from [5] to further reduce E_{IN}. $V_{\mathrm{dd,mem}}$ is maintained at 0.6V during *Sleep* to retain SRAM data. Fig. 8 shows the trajectory of multi-V_{dd} assignments by the proposed MEP tracker without performance constraints. Detailed bench measurements were performed to measure E_{IN} across $V_{\mathrm{dd,i}}$ combinations to identify the true optimum (MEP*). The proposed tracker successfully converges to, and dithers around a steady-state value, achieving E_{IN} within 2.2% of the true minimum. The contour plot, derived from bench measurements, confirms the convexity of the optimization problem, validating the descent methods.

Fig. 9 shows measured run-time tracking under performance constraints. The trajectory of both, T_{run} and the multi-V_{dd} are shown. For demonstration purposes, the system is configured

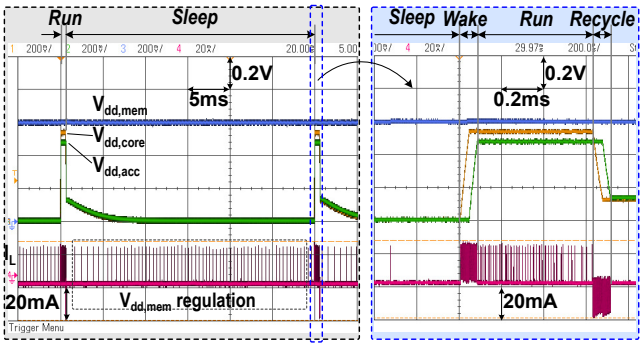


Fig. 7. Measured oscilloscope waveforms of the proposed system operation over a complete power cycle.

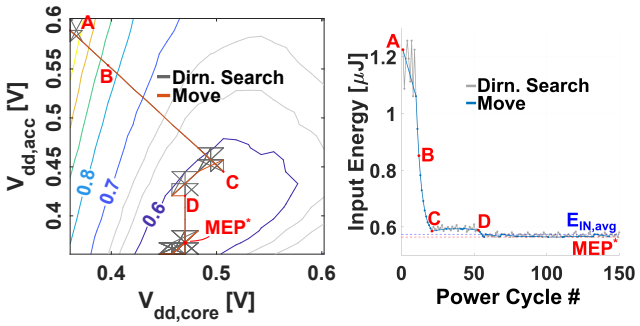


Fig. 8. Measured multi-V_{dd} trajectory guided by the proposed tracker without $T_{\mathrm{run,max}}$ constraints and corresponding E_{IN} at runtime, at various trajectory points, and good convergence to MEP.

to operate without $T_{\mathrm{run,max}}$ constraints for the first 210 power cycles. The controller therefore converges near the true unconstrained optimum, MEP(unconst). A $T_{\mathrm{run,max}}$ constraint is applied at cycle 210, prompting the controller to adjust $V_{\mathrm{dd,i}}$ assignments toward the feasible region in the direction of steepest T_{run} descent, eventually converging to within 0.32% of the true constrained minimum.

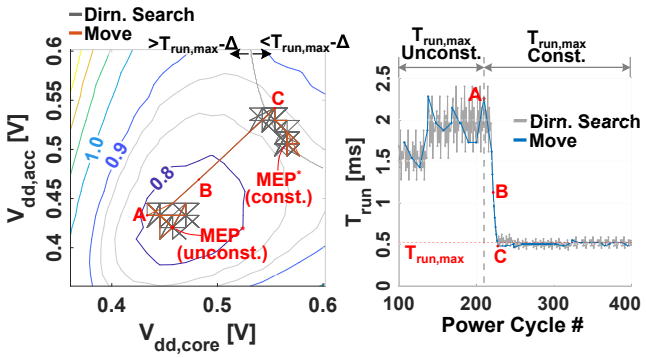


Fig. 9. Measured multi-V_{dd} trajectory controlled by the proposed tracker with constraints applied at cycle 210 and E_{IN} at corresponding points in the trajectory, which converge to the true MEP.

Fig. 10 demonstrates MEP tracking while performing two tasks (*A* and *B*) that alternate every five power cycles. Each task has a distinct MEP as a result of different control flow and processor-accelerator dependencies. Measured $V_{\mathrm{dd,core}}$ and $V_{\mathrm{dd,acc}}$ traces are shown, both with and without *TCM* enabled. By maintaining program-dependent MEP state, the *TCM* enables the tracker to rapidly reposition $V_{\mathrm{dd,i}}$ to their previously best-known MEP configurations when tasks abruptly change. Energy measurements are also compared to the baseline controller, which tracks only the *Run*-stage MEP with a uniform V_{dd} assignment across all domains. This baseline represents existing state-of-the-art implementations. The cMEP tracker achieves E_{IN} reductions of 29.9% and 16.7% with and without Recycle operation, respectively.

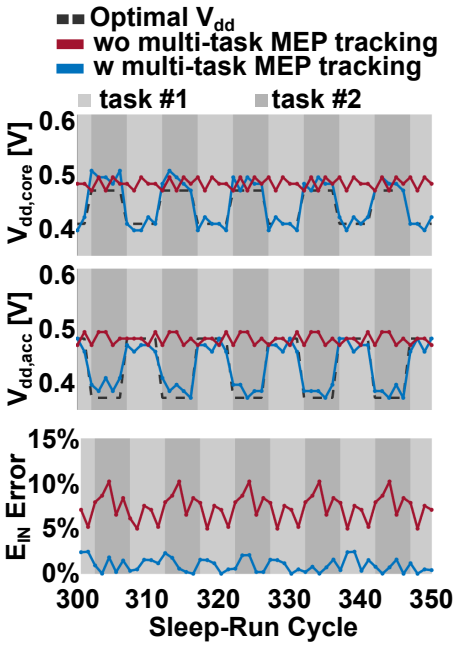


Fig. 10. Measured $V_{\mathrm{dd,core}}$, $V_{\mathrm{dd,acc}}$ and E_{IN} error (relative to true minimum energy) under alternating program execution with and without Task Context Memory.

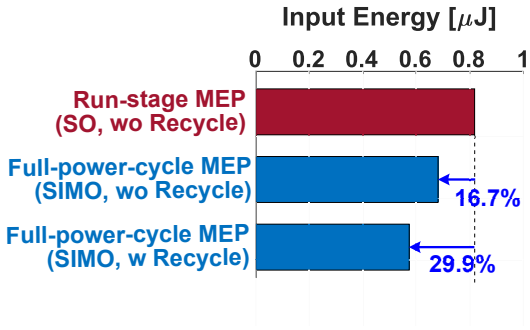


Fig. 11. Measured per-power cycle E_{IN} of the proposed MEP tracker compared to the baseline.

Table I compares the proposed design to prior work. Compared to the state-of-the-art, the proposed design minimizes multi-domain SoC energy consumption and achieves 1.43× energy reduction compared to the baseline while providing multi-task MEP tracking.

TABLE I. Comparison with related work.

	[2]	[5]	[6]	This work	
Process	65nm	65nm	65nm	**65nm**	
Regulator(Domains)	SC(1)	Buck(1)	Buck(1)	**SIMO(3)**	
Loads	Cortex M0 core + FFT	Cortex M0 core + SRAM	RISC-V + SRAM	**RISC-V + SRAM + Hardware Accelerators**	
Input Voltage (V)	1.2	1.8	1.5	**1.8**	
Output Voltage (V)	0.38 to 0.58	0.6 to 1	0.4 to 1.1	**0.36 to 0.7**	
Inductor/Capacitor	250 pF	10 µH & 10 µF	22 µH & 4.7 µF	**10 µH & 1 µF**	
MEP Tracking Scope	Run only	Sleep and Wake	Run only	Run only (Baseline)	**Sleep, Wake, and Run (entire Power Cycle)**
Performance Constrained Tracking / Constrained Type	Yes / Frequency	No	No	No	**Yes / Total Run-time**
Domains optimized by MEP Tracker	Single	Single	Single	Single	**Multi-domain**
Multi-task Tracking	No	No	No	No	**Yes**
Tracking E_{IN}/EPC Error (%)	<1*	<5	<2.3	N/A	**<2.2**
Normalized energy reduction **	1x*	N/A	N/R	1x	**1.43x**

*Estimated from its measurement results

**Relative to E_{IN} with only single-V_{dd} *Run*-stage MEP tracking over a *Sleep-Run* cycle

IV. Conclusion

We demonstrate an MEP tracking architecture for duty-cycled SoCs with multiple V_{dd} domains that dynamically tunes $V_{\mathrm{dd,i}}$ to minimize the total energy drawn from the power source while guaranteeing execution time. This work minimizes full-power-cycle MEP with *Task Context Memory* enabled support for simultaneous MEP tracking across multiple tasks that may be executed over successive power cycles.

Acknowledgment

Carlos Tokunaga, Edevaldo Pierera, Stefano Pietri, and Keith Bowman for their valuable input.

References

[1] Y. K. Ramadass and A. P. Chandrakasan, "Minimum Energy Tracking Loop With Embedded DC–DC Converter Enabling Ultra-Low-Voltage Operation Down to 250 mV in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, 2008.

[2] F. u. Rahman, R. Pamula, and V. S. Sathe, "Computationally enabled minimum total energy tracking for a performance regulated sub-threshold microprocessor in 65-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 494–504, 2020.

[3] J. Lee, S. Miyoshi, M. Kawaminami, D. Blaauw, D. Sylvester, Y. Zhang, Q. Dong, W. Lim, M. Saligane, Y. Kim, S. Jeong, J. Lim, and M. Yasuda, "A Self-Tuning IoT Processor Using Leakage-Ratio Measurement for Energy-Optimal Operation," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 1, pp. 87–97, 2020.

[4] N. H. Tseng, B. K. Wu, T. P. Huang, C. Y. Lee, K. H. Chen, Y. H. Lin, S. R. Lin, and T. Y. Tsai, "A series stacked FinFET structure for digital low dropout regulators with minimum energy point technique for 37.5% energy reduction in Cortex M0 processor," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 2021-May, pp. 28–31, 2021.

[5] C.-H. Huang, A. Mandal, D. Peña-Colaiocco, E. P. D. Silva, and V. S. Sathe, "Regenerative breaking: Optimal energy recycling for energy minimization in duty-cycled domains," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 1, pp. 68–77, Jan. 2023.

[6] X. Liu, S. Kamineni, J. Breiholz, B. H. Calhoun, and S. Li, "A 194nw energy-performance-aware lot soc employing a 5.2nw 92.6% peak efficiency power management unit for system performance scaling, fast dvfs and energy minimization," in *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, 2022, pp. 224–225.

[7] C.-H. Huang, Y. Chen, X. Sun, A. Mandal, V. R. Pamula, N. Kurd, and V. S. Sathe, "Improving simo-regulated digital soc energy efficiencies through adaptive clocking and concurrent domain control," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 1, pp. 90–102, 2022.