A 3.6-6.6GHz Multiphase Class-G Doherty Digital Power Amplifier Achieving 48.9% Peak Drain Efficiency in 22 nm FD-SOI CMOS

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***Abstract*— This paper presents a multiphase Doherty class-G digital power amplifier (DPA) with time-interleave (TI) LOs. The multiphase Doherty structure is proposed to improve the efficiency for quadrature Doherty DPA. To further enhance the efficiency at deep power back-off (PBO) levels, class-G and time-interleave LOs are also incorporated, which lead to 120 efficiency peaks. The fabricated DPA achieves peak drain efficiency (DE) of 48.9% with 23.1 dBm output power at 4 GHz, and 27.1% DE with 12dB PBO, which is 6~8% better than others. With 64-QAM modulated signals, the DPA achieves measured average drain efficiency of 35.5% while attaining error vector amplitude (EVM) of -33.4dB.**

Keywords*— *Digital Power Amplifier, Doherty, Multiphase, Class-G, Time-Interleave, Drain Efficiency, Switching PA

I. INTRODUCTION

The wireless communication systems nowadays employ complex QAM modulation that requires PA to work with high peak-to-average-power-ratio (PAPR). Hence, efficiency enhancement in deep PBO levels becomes critical. Recently, IQ-cell sharing quadrature class-G Doherty DPAs (Q-DPA) have demonstrated good efficiency at deep PBO levels[1~3]. However, the inherent poorer efficiency for quadrature DPA due to the combination of I and Q components limits the achievable efficiency. As reported in [2], for quadrature DPA to switch phase from 0° to 45°, the system efficiency drops from 32% to about 16%. By changing the combinations of main and peaking PA at different operation regions, the power added efficiency (PAE) for quadrature DPA only improves to 27% for 45° [3].

In this paper, we propose a multiphase Doherty DPA (MDPA) structure to overcome the quadrature DPA limitation. In combination with other techniques, such as class-G, time-interleave LOs, our DPA can achieve 120 efficiency peaks and enhance the efficiency at PBO larger than 12dB. The architecture and circuit blocks of M-DPA will be discussed in section II. This is then followed by measurement results in section III. Conclusions are given in section IV.

II. MULTIPHASE DIGITAL PA WITH MULTIPLE EFFICIENCY ENHANCEMENT TECHNEQUES

A. Operation of Multiphase Doherty DPA

The IQ-cell sharing quadrature DPA suffers from power loss for capacitor switching (P_{SC}) during combination of I and Q components to achieve the desired output phase, as shown below[2]:

$$P_{SC} = \frac{p_1(N-p_1)}{N^2}CfV^2 + \frac{p_2(N-p_2)}{N^2}CfV^2 \quad (1)$$

where N is the total number of the DPA cells (I+Q), p_1 and p_2 represent the number of turn-on cells for I and Q respectively. If only I or Q component is functioning, the DPA is operating in polar mode with the best efficiency as the loss (P_{SC}) is only associated with the functioning I or Q component. The efficiency is the worst for 45° phase as there will be loss from both components. Hence, by introducing 4 additional diagonal phases (45°, 135°, 225°, and 315°), we can retain the best efficiency of polar mode. In addition, to synthesize any phase component that falls between the I/Q and diagonal phase components, the efficiency would also be better due to their smaller phase difference.

Fig. 1(a) shows the different operation regions of the quadrature Doherty DPA to enhance efficiency. However, it was noted that the best efficiency is only attained at region II while the efficiencies at other regions are compromised. With the proposed MDPA, the efficiencies at different regions can be improved significantly, as shown in Fig. 1(b).

As illustrated, at region I, any points within the region can be achieved by combining the main PA working with I component and peaking PA working with diagonal phase component (45°). The efficiency is enhanced as both main and

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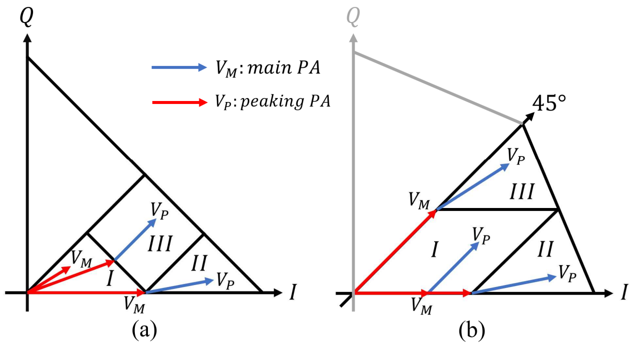

Region	I	II	III
Quadrature Doherty	low	moderate	lowest
Multiphase Doherty	**high**	**moderate**	**moderate**

(c)

Fig. 1. Region split and operation mode of (a) conventional quadrature Doherty DPA [2] and (b) proposed multiphase Doherty DPA and (c) efficiency table.

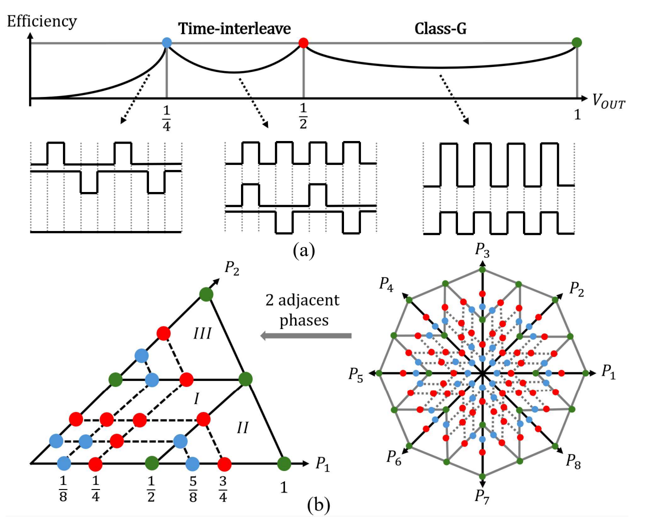

Fig. 2. (a) Efficiency enhancement techniques for main/peak PA (b) 120 efficiency peaks for multiphase input based on switching power loss.

peaking PAs are working in polar mode. At region II or III, the main PA is fully turned on at either I or diagonal phase component with maximum efficiency, while the peaking PA is then working in less efficient cell sharing mode by combining the I and the diagonal phase component within the peaking PA to achieve any point within the region. However, the resulting cell sharing mode is still more efficient than conventional quadrature DPA due to the smaller phase difference between the two combined components (45° vs 90°). The efficiency table is also shown in Fig. 1(c).

B. Multiple Efficiency Peaks

To achieve multiple efficiency peaks at different PBO, similar class-G and time-interleave LOs techniques [4] are employed for main PA and peaking PA respectively, depending on their desired output amplitude.

As shown in Fig. 2 (a), when the main PA is working with amplitude above 0.5×V_{out_peak}, class-G technique is applied by combining main PA cells working at either V_{DD} or 2×V_{DD}. For main PA to output voltage between ¼ to ½ of V_{out_peak}, main PA will employ time-interleave technique for some cells while the remaining cells are working at V_{DD}. Below ¼ V_{out_peak}, only time-interleave cells are deployed. Similar approaches are applied for peaking PA.

Hence, as illustrated in Fig. 2(b), by applying the efficiency enhancing technique together with the multiphase approach, for the three regions sandwiched between the two adjacent phases, 21 efficiency peaks can be obtained. In total, to cover any points within the whole region, a total of 120 efficiency peaks can be achieved.

C. Circuit Implementation

As shown in Fig. 3, the proposed MDPA is composed of three parts. They are the DPA arrays with power combiner, the multiphase generation block, and the digital decoder.

As illustrated, there are two main PA and two peaking PA arrays. All PA arrays are identical. Each array has 16 unary phase-shared cells controlled by 5-bits MSB and 6 binary cells controlled by 6-bits LSB. To balance the chip area and DAC resolution, the LSB cells are constructed using C-2C structure [5]. The phase-shared PA cell consists of level shifter and phase selection multiplexer. The phase-shared PA cell can choose between V_{DD} and 2×V_{DD}, and can be driven by either I/Q or diagonal phase components. Each component can be chosen to be normal or time-interleave clock phase. Main PA and peaking PA output are then sent to the two inputs of the transformer. Here, two transformers are employed with their secondary coils connected in parallel to maximize the output power level. The transformers are designed using thick metal layers to minimize the loss. In addition, shunt capacitors are added at the two secondary coil outputs for load pull consideration.

To generate the 8 phases required for the proposed MDPA, injection lock ring oscillator (ILRO) is employed. Super-harmonic injection is used here with input frequency being twice the output frequency of ILRO. To minimize the phase mismatch, the delay cell of the ring oscillator is tunable to minimize the frequency difference between the desired output frequency and the free-running frequency of the ILRO. The

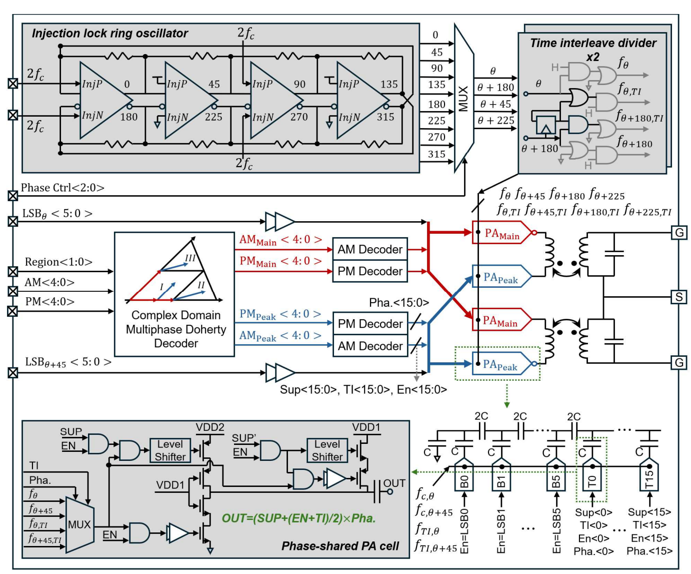

Fig. 3. Circuit details of the proposed multiphase Doherty DPA.

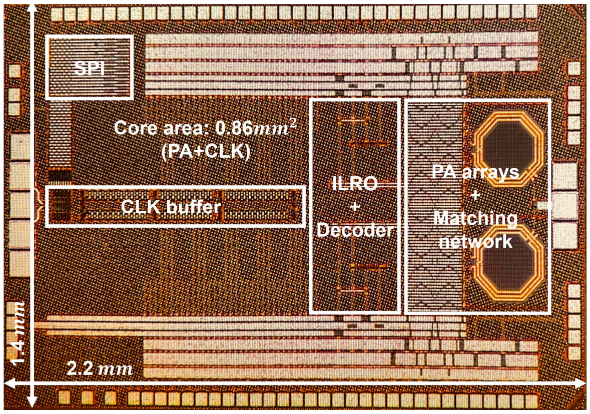

Fig. 4. Chip microphotograph in 22nm FDSOI CMOS process.

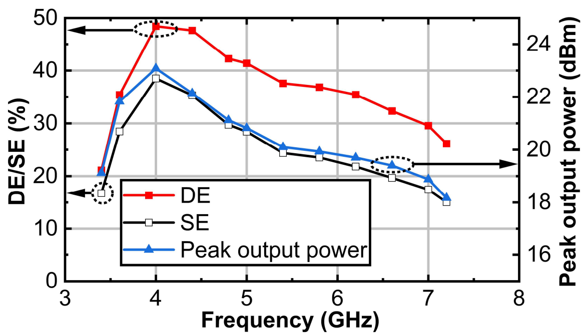

Fig. 5. Measured peak output power and efficiency versus frequency for CW input.

resulting phases are then chosen through a MUX before being sent to time-interleave divider. This will generate both normal and time-interleave clock phases.

Finally, the digital decoder's main objective is to map the input baseband data into the desired I/Q and diagonal phase components for main and peaking PAs, which are the amplitude (AM_{main}/AM_{peak}) and phase (PM_{main}/PM_{peak}) control signals.

III. Measurement Reauslts

The proposed MDPA is fabricated in 22-nm FDSOI process, occupying a total area of 2.2mm×1.4mm with core area of only 0.86 mm^2, as shown in Fig. 4.

A. CW Measurements

As shown in Fig. 5, the DPA achieves a peak power of 23.1 dBm and peak drain efficiency (DE) of 48.9% at 4 GHz with a continuous wave (CW) input. As drain efficiency is highly related to the switch resistance and the matching network loss, the low switch resistance provided by 22-nm FDSOI through back-gate bias tuning, as well as the low loss transformer realized with thick metal and low loss FDSOI substrate help. After including the other support blocks, the peak system efficiency (SE) becomes 38.9% at 4 GHz. Wideband matching network is adopted in our design, which exhibits two measured resonant frequencies at 4.0 GHz and 7.4 GHz. This is about 0.3-GHz lower than our original design, and could be due to inaccurate modelling of interconnect. The

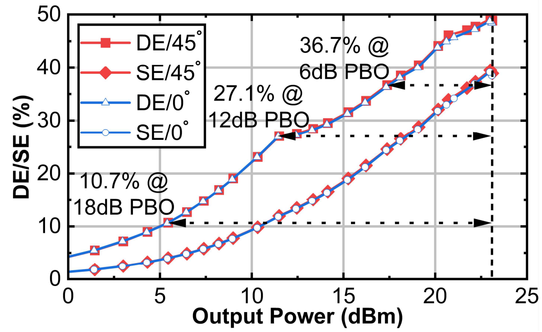

Fig. 6. Measured drain/system efficiency versus output power at 4GHz with CW input.

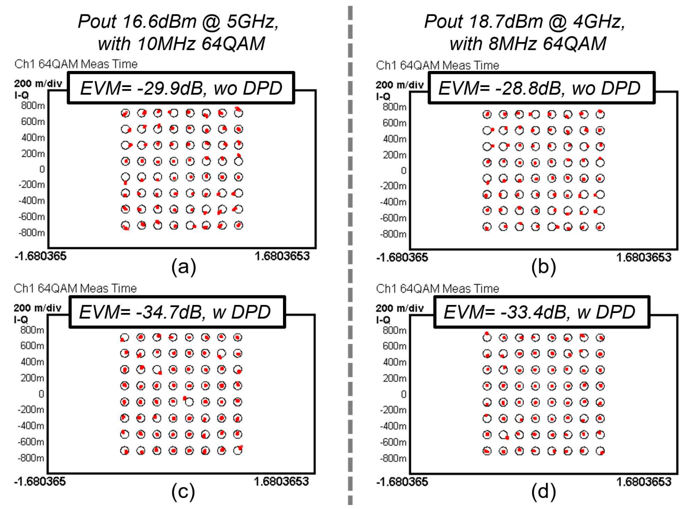

Fig. 7. Measured EVM and constellations at 4GHz with 8MHz 64QAM (a) without DPD and (c) with DPD; at 5GHz with 10MHz 64QAM (b) without DPD and (d) with DPD.

measured DE and SE are above 30% and 20% from 3.6GHz to 6.6GHz respectively.

Fig. 6 plots the efficiencies versus output power levels at 4 GHz. Through the proposed efficiency enhancement techniques, the MDPA achieves 46.1%/36.7%/27.1%/10.7% DE with PBO of 2.5/6/12/18 dB respectively. This is about 6~10% better than other reported works, as shown in Table I.

B. RF Modulation Measurements

To evaluate the linearity performance, 64-QAM modulated baseband data are sent to our MDPA. The EVM measurements at 4 and 5-GHz carrier frequencies are shown in Fig. 7. Without digital pre-distortion (DPD), the resulting EVM is around -28.8/-29.9 dB at 4/5 GHz. In polar DPA, the EVM at lower output power without DPD is usually better. In our case, it is limited due to phase mismatches, time-interleave accuracy and etc. However, with DPD, the EVM is improved to -33.4/-34.7 dB. Fig. 8 shows the EVM and DE at different PBO levels for 4 and 5-GHz carrier frequency. As illustrated, with DPD, the MDPA can achieve EVM better than -30 dB over more than 30-dB dynamic range. With our proposed technique, the DPA achieves DE and SE of 35.5% and 22.4% respectively with 4.4-dB PBO at 4 GHz. At deeper PBO levels of 7.2dB an

Table I. Comparison with state-of-the-art DPAs

		This work		JSSC 2024 [3]		JSSC 2024 [6]		JSSC 2021 [2]		ISSCC 2021 [7]		ISSCC2025 [8]	
Architecture		**Multiphase Doherty Class-G with TI**		Quadrature Doherty Class-G		Time-domain Quadrature		Quadrature Doherty Class-G		Polar Current Model		Multiphase Subharmonic	
Technology		**22nm**		28nm		65nm		65nm		65nm		65nm	
Supply (V)		**1.6/0.8**		2.2		2.4		2.55/1.25		--		1.2	
Frequency** (GHz)		**3.6 ~ 6.6**		1.9 ~ 2.9		2.6		2.2		5.2 ~ 6.2		21 ~ 28	
Peak Pout (dBm)		**23.1**		29.9		20.6		27.8		27		19.8	
Efficiency at PBO (%)	Peak	**48.9 (DE)**	**38.9 (SE)**	38.0 (PAE)	--	37.8 (PAE)	--	--	32.1 (SE)	40.1 (DE)	--	38.3 (PAE)	24.6 (SE)
	2.5dB	**46.1 (DE)**	**33.9 (SE)**	31.8* (PAE)	--	31.5* (PAE)	--	--	27.9* (SE)	34.7* (DE)	--	28.0* (PAE)	--
	4dB	**40.5 (DE)**	**28.8 (SE)**	30.0* (PAE)	--	29.5* (PAE)	--	--	25.1* (SE)	29.2* (DE)	--	24.5* (PAE)	--
	6dB	**36.7 (DE)**	**24.6 (SE)**	27.3* (PAE)	--	27.6* (PAE)	--	--	20.1* (SE)	26.3 (DE)	--	19.0* (PAE)	--
	12dB	**27.1 (DE)**	**12.0 (SE)**	17.9* (PAE)	--	14.7* (PAE)	--	--	10.1* (SE)	21.1 (DE)	--	15.2* (PAE)	--
	18dB	**10.7 (DE)**	**4.0 (SE)**	11.0* (PAE)	--	6.8* (PAE)	--	--	3.9* (SE)	--	--	5.6* (PAE)	--
# of Efficiency peak		**120**		32		--		16		--		--	
Carrier Frequency (GHz)		**4**	**5**	2.3		2.6		2.2		5.4		24	
Modulation		**8/16MHz 64QAM**	**10/20MHz 64QAM**	20MHz 64QAM LTE		40MHz 64QAM		20MHz 1024QAM		20MHz 256QAM		200MHz 64QAM	
Average Pout (dBm)		**18.7/18.6**	**16.6/15.7**	24.5		16.4		21		22		9.5	
PBO (dB)		**4.4/4.5**	**4.2/5.1**	5.4		4.2		6.8		5		10.3	
Average Efficiency (%)		**35.5/32.7 (DE)**	**29.3/27.5 (DE)**	25.3 (PAE)		26.4 (PAE)		18.4 (SE)		27.4 (DE)		22.3 (DE)	
EVM (dB)		**-33.4/-31.1**	**-34.7/-30.4**	-25		-25.7		-43		-33.5		-34.3	
Chip size (mm²)		**0.86 (core)/ 3.08 (whole)**		0.74 (core)		1.3 (whole)		0.9 (core)		7.1 (whole)		0.74(core)	

*: estimated from figures **: DE/PAE>30%

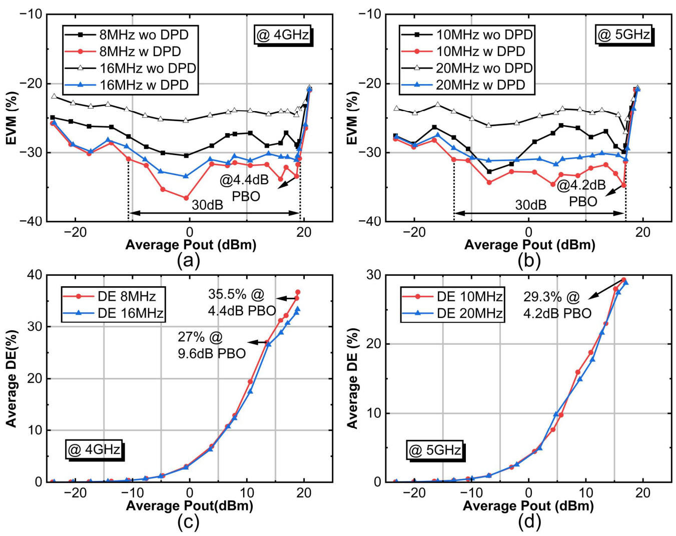

Fig. 8. Measured EVM and average DE versus average Pout at (a) (c) 4GHz with 8/16MHz 64QAM and at (b) (d) 5GHz with 10/20MHz 64QAM.

9.6dB, it also achieves DE of 31.3% and 27.0%.

Compared to quadrature Doherty DPA [2, 3, 6], we achieve better drain and system efficiency, proving the advantage of multiphase over quadrature. It should be noted that our peak output power is much smaller than [2, 3], which is detrimental to the SE estimation. Hence, our better SE illustrates that the power of our supporting circuits is also smaller than others. In terms of operating frequency range, we look at the frequency which exhibits DE above 30%, and our work exhibits 3 times operating frequency range than others for sub-6-GHz PAs.

IV. Conclusion

This paper presents a multiphase class-G Doherty DPA with time-interleave LOs. Through the proposed multiphase Doherty technique, we can achieve better efficiency peaks than conventional quadrature Doherty. Together with other efficiency enhancing techniques, the proposed DPA exhibits 120 efficiency peaks, achieving peak DE and SE of 48.9% and 38.9% respectively. It also demonstrated 6~8% better DE than other reported quadrature DPA works.

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