Investigating the Lateral Trap Position Dependence of RTN Amplitudes in FD-SOI MOSFETs

Nitish Kumar*, Maryline Bawedin, Gérard Ghibaudo, and Christoforos Theodorou
CROMA, Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP , 38000 Grenoble, France
*Email: nitish.kumar@grenoble-inp.fr

***Abstract*— The drain current variations caused by a single trapped charge along the channel length at the gate oxide/silicon channel interface, are analyzed using 3D TCAD modeling in 28 nm FD-SOI MOSFETs for both linear and saturation regions. The study highlights the influence of the trap's lateral position on the corresponding RTN amplitude in both weak and strong inversion modes, with a contribution from both carrier number and mobility fluctuations, in conjunction with short-channel effects. The results emphasize the need to account for RTN amplitude modulation by the trap lateral position in both the linear and saturation regions for more realistic noise simulations in nano-scale circuits, and some practical approaches are proposed for modeling and characterization purposes.**

Keywords*— *Interface traps, RTN, BTI, Short channel effects, FD-SOI MOSFETs, TCAD modeling.

I. Introduction

Fully depleted (FD) silicon-on-insulator (SOI) field-effect transistors (FETs) are already an established technology in complementary metal-oxide-semiconductor (CMOS) digital [1], analog [2] and RF [3] circuits, thanks to their superior ability to minimize leakage currents, reduce power consumption, minimize short-channel effects (SCEs) and variability, and provide the possibility of back-bias threshold voltage control [1]. This performance improvement is primarily attributed to the thin silicon layer being fully depleted of charge carriers.

However, as CMOS downscaling advances, trapping-related effects become more important, such as: an increase in low-frequency noise (LFN) and LFN variability [4], along with discrete current-level switching over time, referred to as random telegraph noise (RTN) [5], [6], as well as a worsening of bias temperature instabilities (BTI) [7]. RTN/BTI can significantly impact the performance of both analog and digital circuits, in particular RTN switching events which are often characterized by very high amplitudes (up to 20 % of DC current [6]). It is therefore critical to properly understand how this amplitude is influenced by parameters such as the trap position in the oxide [8] or across the channel [9]. For the latter in particular, to the best of our knowledge, there is a lack of detailed simulation study of how exactly the lateral trap position affects the drain current and why. The works of Asenov's group [8], [10], [11], although well documented in the literature, are limited to probing the electrostatic impact on the carrier density (not the channel mobility), and only in weak inversion when examining the influence of drain-source voltage (V_{DS}) in short channels. Other teams, including ours, have reported strange dependencies of the RTN amplitude with V_{DS} [12]-[15], and suggested ways to use this behavior to laterally localize the trap, but they did not particularly attribute these effects to specific fluctuations such as channel charge or mobility, nor to SCEs like drain-induced barrier lowering (DIBL) or source-drain proximity effect (SDPE).

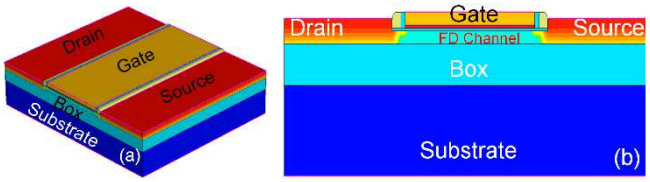

Fig. 1. (a) 3D schematic view of high-k/metal gate 28 nm FD-SOI MOSFETs and (b) cross-sectional view along the channel length of 28 nm FD-SOI MOSFETs.

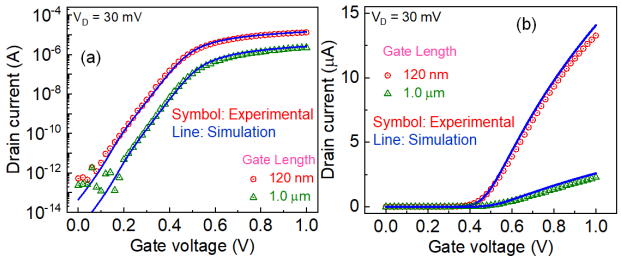

Fig. 2. Calibrated transfer characteristics (*I-V*) with measured data of 28 nm FD-SOI FETs for 120 nm and 1 µm gate lengths.

Finally, we recently demonstrated [16] that the classic carrier number fluctuation with correlated mobility fluctuation (CNF/CMF) model [17] cannot properly capture the drain bias dependence for traps near the edges. A lot of TCAD-based RTN amplitude simulations are also documented [8]-[11], but most researchers have focused on the linear region of operation. However, from a circuit operation point of view, the analysis and comprehension of RTN amplitude in the saturation region is very important, and should be a requirement for a proper model development for circuit simulators.

The aim of this work is to reveal the physical mechanisms (i.e., local charge or mobility fluctuations) behind RTN/BTI amplitude behaviors in both linear and saturation regions, by varying the single trap position along the channel length, for various channel lengths, and from weak to strong inversion. A promising modeling approach is also proposed.

II. Experimental and Simulation Details

A. 28nm FD-SOI MOSFET Structure Details

Fig. 1 shows the 3D and cross-sectional simulated n-channel FD-SOI MOSFET, based on the 28 nm FD-SOI technology process from ST Microelectronics [1]. The channel thickness is 7 nm, with a 23 nm buried oxide (BOX). The channel width is 300 nm, and the gate length varies from 30 nm to 1 µm. TiN metal is used as the gate electrode on top of a high-k gate dielectric with an effective equivalent oxide thickness of ~1.8 nm. The electrically measured transfer characteristics at room temperature are shown in Fig. 2 in the linear region, with a drain voltage (V_D=30 mV) for 120 nm and 1 µm gate lengths.

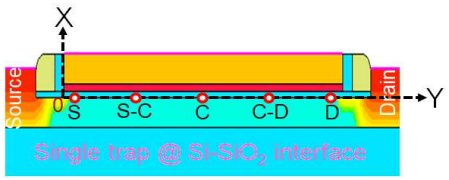

Fig. 3. Schematic view of single trapped charge selected positions at the channel-gate oxide (SiO_2) interface along the channel length: S: Source, S-C: between Source and Center, C: center, C-D: between center and drain, D: Drain.

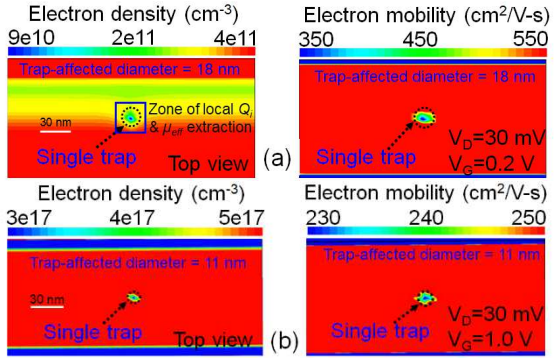

Fig. 4. Top view of electron density and mobility showing the impact of a single trap at the interface of the channel and gate oxide in the center of the linear region (V_D = 30 mV) for (a) V_G = 0.2 V and (b) V_G = 1.0 V.

B. TCAD Model Calibration with Experimental Data

Fig. 2 shows the calibrated transfer characteristics in both log and linear scales for 28 nm FD-SOI MOSFETs with 120 nm and 1 µm gate lengths, simulated on the *Sentaurus* 3D TCAD platform using the following device physics models. The drift-diffusion (DD) transport equation, along with the Philips unified, Lombardi, and high-field saturation models, is solved by accounting for the effects of impurity doping, carrier-carrier scattering, phonon scattering, surface roughness, Coulomb scattering, and high-field saturation mobility. The density gradient model is used to account for quantum effects. With these models, the calibrated transfer characteristics show excellent agreement between the simulation and experimental data (taken from [18]), as shown in Fig. 2 for 120 nm and 1 µm gate lengths.

C. TCAD Configuration for Single Trap Analysis

The drain current variation due to the presence of a single trapped charge, i.e. the RTN amplitude, ΔI_D, is simulated by considering a single acceptor-like trap charge at the interface between the channel and gate oxide, as shown in Fig. 3. Since this work concerns only the electrostatic impact and not the trap occupancy, the trap is considered always at its charged state (negative charge) for all bias conditions. The effect is analysed for evenly spaced lateral trap positions, from source to drain, at 6 nm grid points along the channel length. The TCAD-modeled contour plots of electron density (Q_i) and mobility (μ_{eff}) distribution in a 120 nm gate length channel, featuring a single trap at its center, are shown in Fig. 4, for subthreshold and strong inversion conditions in linear regime. It can be clearly seen that the single trapped charge significantly influences both Q_i and μ_{eff}, revealing that both will contribute to ΔI_D. Moreover, the trap-affected region diameter, as well as its influence on Q_i and μ_{eff}, is much higher in the subthreshold regime compared to the strong inversion, meaning that the 'trap range' is also bias- and position-dependent.

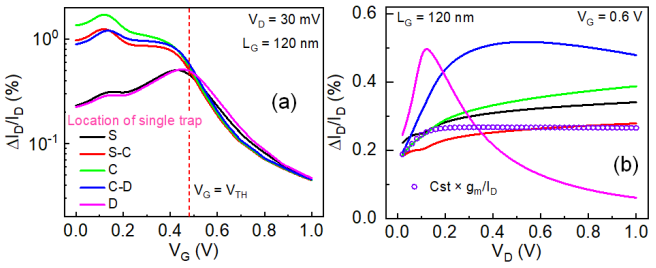

Fig. 5. Dependence of the relative RTN amplitude on (a) gate voltage (V_G) in linear region and (b) drain voltage (V_D) above the threshold voltage (V_G = 0.6 V) for a 120 nm gate length.

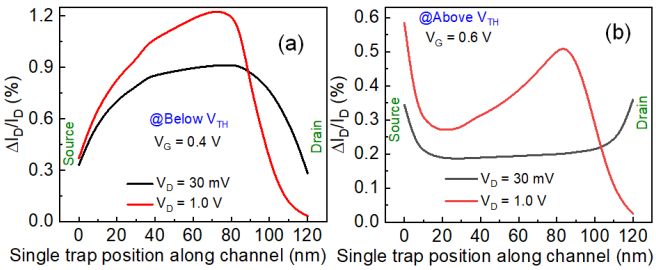

Fig. 6. Dependence of the relative RTN amplitude on the position of a single trap from source to drain in the linear and saturation regions: (a) $V_G < V_{TH}$ and (b) $V_G > V_{TH}$.

III. Results And Discussion

A. First observations

To obtain an overview of how ΔI_D depends on the lateral trapped charge position and channel length variation in the linear and saturation regions, the relative RTN amplitude ($\Delta I_D/I_D$) as a function of gate voltage in the linear region is shown in Fig. 5(a) for five trap positions (as in Fig. 3). It can be clearly seen that the impact is higher at the centre of channel, where the potential barrier is maximized in the weak inversion regime [11]. ΔI_D is also significantly attenuated near the source and drain in the weak inversion regime, due to the SDPE i.e., potential pinning at the channel edges near S (source) and D (drain). The effect of a single trap is stronger in weak inversion and begins to decrease significantly near the threshold voltage, due to the screening of the Coulomb potential of the trap charge by the inversion charge [11]. It is also worth noting in Fig 5(a), how all five curves almost coincide above the threshold voltage, V_{TH} = 0.48 V, revealing how uniform is the carrier channel in strong inversion in ohmic regime. However, the relative ΔI_D as a function of drain voltage above V_{TH} (V_G=0.6 V), as shown in Fig. 5(b), reveals a very different dependence for each position across the channel, especially for the two edges (S and D). ΔI_D in deep saturation (V_D = 1 V) becomes almost negligible when the trap is near the drain, due to the local channel depletion (Fig. 5(b)). Additionally, the relative ΔI_D increases with drain voltage when a single trap charge is located at or near the centre. It is significantly higher near the drain in the linear region but attenuates in the saturation region, a behaviour similar to what was reported in [9] for traps in the channel, and in [15], [16], for oxide traps. This amplitude reflects substantial variations in carrier density and/or mobility, from C (centre) to D in both linear and the saturation region. Fig. 6(a) shows the relative RTN amplitude ($\Delta I_D/I_D$) as a function of a single trap position from S to D, below V_{TH}, revealing a bell-shaped curve, with a peak between C and D in the linear region. However, in the saturation region, the peak is slightly shifted towards C with a higher value.

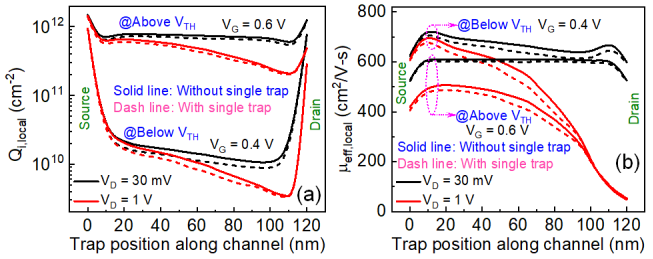

Fig. 7. The local trap region (a) electron density and (b) mobility with and without a single trap along the trap position in the linear and saturation regions for $V_G < V_{TH}$ and $V_G > V_{TH}$.

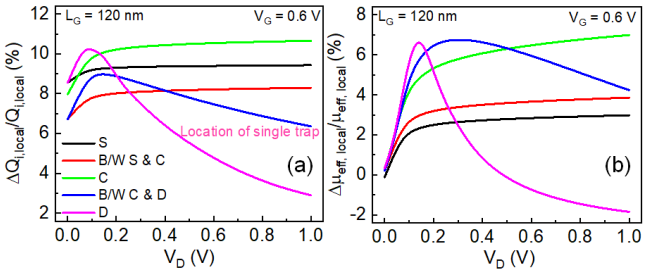

Fig. 8. The local trap region (a) electron density and (b) mobility variations as a function of V_D above V_{TH}.

Above V_{TH} (see Fig. 6(b)), while $\Delta I_D/I_D$ follows a parabolic-shaped curve moving from source to drain in linear region, in the saturation region, this behavior is reversed at the drain side of the channel, resembling the dependence below V_{TH}, revealing a complete control of this part by V_D.

B. Probing charge and mobility variations

In Fig. 7 are presented the local values of carrier density ($Q_{i,local}$) and mobility ($\mu_{eff,local}$) versus the trap position, extracted using a square region of 24x24 nm^2 (to capture all the 'trap range') around the trapped charge, to account for the whole trap range. In both regions, the $Q_{i,local}$ variation is significantly higher than the mobility one at the position of the $\Delta I_D/I_D$ peak, as can clearly be seen in Fig. 7. Moreover, there is a clear pinning of both $Q_{i,local}$ and $\mu_{eff,local}$ right next to S and D, which can explain the behavior of $\Delta I_D/I_D$ in Fig. 5(a). The pinch-off effect near the drain in the saturation region is also clearly visible in $Q_{i,local}$ and $\mu_{eff,local}$, as it seems to almost cancel out any conductivity variation near the drain.

For a deeper understanding of the simulated behavior shown in Fig. 5(b), the relative change in electron density ($\Delta Q_{i,local}/Q_{i,local}$) and mobility ($\Delta\mu_{eff,local}/\mu_{eff,local}$) of the trap region is plotted in Fig. 8, as a function of drain voltage in strong inversion. Indeed, there is a high resemblance with the $\Delta I_D/I_D$ versus V_D curves of Fig. 5(b), and their values are in the same order of magnitude, indicating that the local $\Delta Q_{i,local}/Q_{i,local}$ and $\Delta\mu_{eff,local}/\mu_{eff,local}$ variations are both key quantities in the interpretation of the RTN behavior. Indeed, if we consider both sources of variations, and account for a position-dependent trap range pre-factor, Y_t, and SDPE factor, λ_t (V^{-1}), we can create an approximative formula (1) and quite closely reproduce the data of Fig. 5(b), as shown in Fig. 9(a).

$$\Delta I_{D,t}/I_D = Y_t \times \left(\Delta Q_{i,local}/Q_{i,local} + \Delta\mu_{eff,local}/\mu_{eff,local}\right) \times (1 + \lambda_t V_D) \quad (1)$$

This underlines the importance of local charge and mobility modeling when trying to model RTN amplitudes. Our assumption that the $\Delta I_D/I_D$ peak is related to the channel pinch-off near D is also supported by the way it shifts exactly as $V_{D,SAT} = V_G - V_{TH}$, as shown in Fig. 9(b).

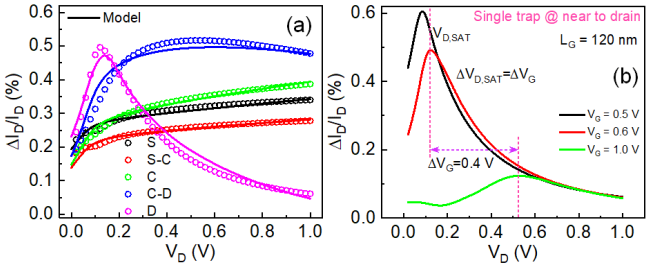

Fig. 9. Dependence of the relative RTN amplitude on V_D for (a) V_G = 0.6 V, modeled with (1), and (b) for 3 different values of V_G.

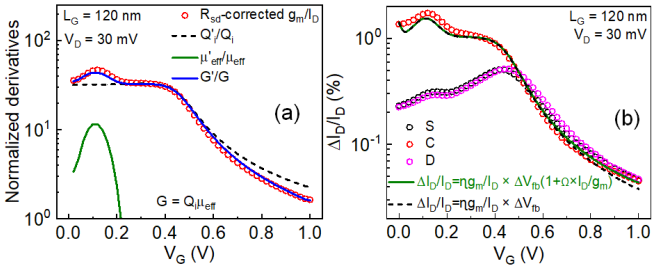

Fig. 10. (a) Normalized derivatives of local carrier density and mobility to validate the hump effect in the subthreshold regime (V_G ~100 mV). (b) Classical CNF/CMF model fitting with RTN amplitude for the single trap at the centre in the linear region.

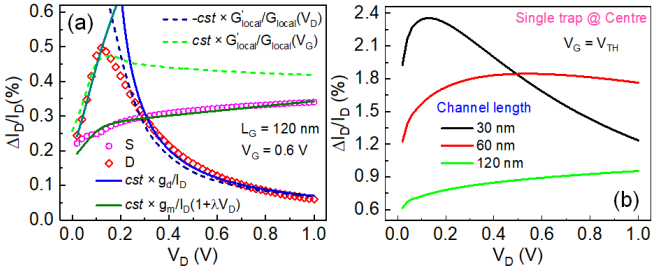

Fig. 11. (a) Correlation between normalized RTN amplitude, transoconductance (g_m) and dynamic channel conductance (g_d), and normalized local conductance derivatives, for S and D traps. (b) Normalized RTN amplitude versus V_D at $V_G = V_{TH}$ for 3 different gate lengths.

C. Applicability of CNF/CMF model for characterization

A well-established experimental RTN characterization method is the CNF model [17], which suggests that $\Delta I_D/I_D$ should be proportional to g_m/I_D. As Fig. 10(a) illustrates, g_m/I_D contains both normalized gate voltage derivatives of carrier density and mobility, which constitute the normalized derivative of the local conductance, ($G_{local} = Q_{i,local}\mu_{eff,local}$), but only for the C position. This correlation is valid only near the central trap, as it is representative of the average conductance. Thanks to this, for C trap, the CNF/CMF model ($\Delta I_D/I_D = \eta\, g_m/I_D \times \Delta V_{fb}(1 + \Omega\, I_D/g_m)$), where η a 'trap range' amplitude pre-factor and $\Delta V_{fb} = q/WLC_{ox}$ the induced flatband voltage shift, can successfully fit the relative RTN amplitude in the linear region, as shown in Fig. 10(b). For trap near S or D ends, and below V_{TH}, that are governed by SDPE, the g_m/I_D trend cannot work. Fig. 5(b) shows that, for the saturation region, the g_m/I_D approach does not hold up even for the trap at C or S.

However, accounting for DIBL through the parameter λ (V^{-1}) and taking $\Delta I_D/I_D = cst \times g_m/I_D(1 + \lambda V_D)$ can help fit quite well the S trap data, as seen in Fig. 11(a). For the trap near D, as in linear regime, the $\Delta I_D/I_D$ data seem to follow of the g_m trend only below 0.2 V. Above that voltage, where the channel region near D is pinched off, the data seem to follow the $g_d = dI_D/dV_D$ trend instead.

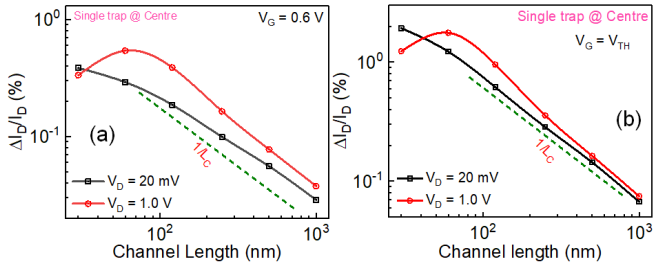

Fig. 12. Dependence of the relative RTN amplitude on channel length scaling: (a) above the V_{TH} (V_G = 0.6 V) and (b) at the V_{TH} in the linear and saturation regions.

We can attribute this to the fact that the conductance (G_{local} = $Q_{i,local}\mu_{eff,local}$) is fully controlled locally by the drain voltage. Indeed, Fig. 11(a) demonstrates how the normalized V_D-derivative of G_{local} is almost identical to the g_d trend. This finding provides an alternative path for both RTN modeling and characterization purposes.

D. Effect of channel length downscaling

The impact of SCEs on the RTN amplitude is illustrated in Fig. 11(b). They become visible for channel lengths of 60 nm and 30 nm, even for the C trap. In fact, $\Delta I_D/I_D$ is already attenuated at a very low V_D for L_C = 30 nm, revealing the importance of SCE consideration for RTN modeling, for all the trap positions. Concerning the channel length scaling of the C trap RTN amplitude, shown in Fig. 12(a) for V_G=0.6 V, it does not follow the $1/L_C$ scaling law. However, this is corrected once the V_{TH} roll-off SCE is accounted for, by extracting the RTN amplitude at $V_G = V_{TH}$ (Fig. 12(b)). As expected, in saturation region, even at $V_G = V_{TH}$, the $1/L_C$ scaling law does hold below L_C = 300 nm. Finally, the "inverse scaling effect" [19] is only observed in saturation region.

IV. Conclusion

The impact of a single trap position, along the channel length, on the RTN amplitude, has been explored in detail for 28 nm FD-SOI MOSFETs in all operation modes. In particular, the variations of both carrier density and mobility near the trap were monitored through 3D TCAD simulations, in order to relate them to the RTN amplitude in a coherent way that reveals the role of SCEs. This underlines the importance of developing models for local charge and mobility variations. It was also shown that the CNF/CMF model for medium length (120 nm) channel may only be valid for traps near the channel center in linear region and near the source in saturation. However, using the channel dynamic conductance (g_d) can help identifying traps near the drain in saturation, as it reflects the local conductance sensitivity. The relative RTN amplitude was found to scale with $1/L_C$ down to 30 nm, but the classical approaches do not work at such lengths, even for traps near the channel center.

Acknowledgment

This work was supported by the "DEFINSIM" IPCEI project. The authors would also like to thank ST Microelectronics, Crolles, France for providing critical information to support our calibration process.

References

[1] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," *2012 Symposium on VLSI Technology (VLSIT)*, Honolulu, HI, USA, 2012, pp. 133-134.

[2] F. Arnaud *et al.*, "28nm FDSOI Platform with Embedded PCM for IoT, ULP, Digital, Analog, Automotive and others Applications," *ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC)*, Cracow, Poland, 2019, pp. 7-10.

[3] L. Nyssens *et al.*, "28 FDSOI RF Figures of Merit down to 4.2 K," *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, San Jose, CA, USA, 2019, pp. 1-3.

[4] M. Banaszeski da Silva, H. P. Tuinhout, A. Zegers-van Duijnhoven, G. I. Wirth and A. J. Scholten, "A Physics-Based Statistical RTN Model for the Low Frequency Noise in MOSFETs," in IEEE Transactions on Electron Devices, vol. 63, no. 9, pp. 3683-3692, Sept. 2016.

[5] M. Luo *et al.*, "Impacts of Random Telegraph Noise (RTN) on Digital Circuits," *in IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1725-1732, June 2015.

[6] X. Wang *et al.*, "Statistical distribution of RTS amplitudes in 20nm SOI FinFETs," 2012 IEEE Silicon Nanoelectronics Workshop (SNW), Honolulu, HI, USA, 2012, pp. 1-2.

[7] M. Toledano-Luque, B. Kaczer, J. Franco, P. J. Roussel, T. Grasser, and G. Groeseneken, "Defect-centric perspective of time-dependent BTI variability". Microelectronics Reliability, vol. 52, no.9-10, pp. 1883-1890, September-October 2012.

[8] Brown, Asenov and Roy, "RTS amplitudes in decanano n-MOSFETs with conventional and high-k gate stacks," *2004 10th International Workshop on Computational Electronics*, West Lafayette, IN, USA, 2004, pp. 159-160.

[9] W. Fang *et al.*, "Study of ΔID/ID of a single charge trap in utbox silicon films," *2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Guilin, China, 2014, pp. 1-3.

[10] Z. Zhang *et al.*, "Comparative study on RTN amplitude in planar and FinFET devices," *2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM)*, Toyama, Japan, 2017, pp. 109-110.

[11] A. Asenov *et al.*, "RTS amplitudes in decananometer MOSFETs: 3-D simulation study," *in IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 839-845, March 2003.

[12] E. Simoen, B. Dierickx, B. De Canne, F. Thoma, and C. Claeys, "On the gate- and drain-voltage dependence of the RTS amplitude in submicron MOSTs," Appl. Phys. A, vol. 58, no. 4, pp. 353–358, Apr. 1994.

[13] C. Marquez, N. Rodriguez, F. Gamiz, R. Ruiz, and A. Ohata, "Electrical characterization of Random Telegraph Noise in Fully-Depleted Silicon-On-Insulator MOSFETs under extended temperature range and back-bias operation," Solid-State Electronics, vol. 117, pp. 60–65, Mar. 2016.

[14] H. C. Han *et al.*, "A 4-Terminal Method for Oxide and Semiconductor Trap Characterization in FDSOI MOSFETs", *25th International Conference on Noise and Fluctuations ICNF 2019*, EPFL, Jun 2019.

[15] A. Tataridou *et al.*, ""Pinch to Detect": A Method to Increase the Number of Detectable RTN Traps in Nano-scale MOSFETs," *2021 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2021, pp. 1-5.

[16] O. Gauthier *et al.*, "Applicability of the Carrier Number Fluctuations Model for Random Telegraph Noise of Nanoscale MOSFETs Operating in Saturation," *2023 International Conference on Noise and Fluctuations (ICNF)*, Grenoble, France, 2023.

[17] O. Roux dit Buisson, G. Ghibaudo, and J. Brini, "Model for drain current RTS amplitude in small-area MOS transistors," Solid-State Electronics, vol. 35, no. 9, pp. 1273–1276, Sep. 1992.

[18] F. Serra di Santa Maria *et al.*, "Comprehensive Kubo-Greenwood modelling of FDSOI MOS devices down to deep cryogenic temperatures," Solid-State Electronics, vol. 192, 2022.

[19] T. Kim, N. Franklin, C. Srinivasan, P. Kalavade and A. Goda, "Extreme Short-Channel Effect on RTS and Inverse Scaling Behavior: Source–Drain Implantation Effect in 25-nm nand Flash Memory," in IEEE Electron Device Letters, vol. 32, no. 9, pp. 1185-1187, Sept. 2011.