A 45–100 GHz SiGe Power Amplifier with Stability and Linearity Enhancement Techniques Achieving 1863 GHz GBW and 20 dBm P_{sat}

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***Abstract*—This paper presents an ultra-wideband (UWB) power amplifier (PA) with enhanced stability and linearity. The PA comprises four differential cascode stages with a two-way differential power combining architecture at the last stage. The metal-oxide-metal (mom) capacitor-based stability-enhancement technique and an adaptive-bias circuit are proposed to improve the stability and linearity of the PA, respectively. Designed and fabricated in a 0.13-μm SiGe BiCMOS technology, the PA can achieve a 3-dB gain bandwidth from 45 to 100 GHz with a peak gain of 30.6 dB at 94 GHz. The 3-dB saturated output power (P_{sat}) bandwidth ranges from 62 to 100 GHz with a peak P_{sat} of 20 dBm and a peak power-added efficiency (PAE) of 17.3% at 92 GHz. The output-referred 1-dB compression point (OP_{1dB}) is 16.5 dBm at 92 GHz. In addition, modulation measurements with data rates up to 18 Gb/s (limited by the bandwidth of the commercial receiver module) are demonstrated for the PA operating in the linear mode. It can also transmit a 1-GBaud single-carrier 64-quadrature-amplitude modulation (QAM) signal centered at the frequency of 94 GHz under an average output power of 15.5 dBm with –24 dB error-vector magnitude (EVM) and 10% PAE without predistortion. The PA occupies an area of 1.15×0.79 mm^2 with a core area of 0.9×0.26 mm^2.**

***Keywords*—Adaptive bias, efficiency, power amplifier (PA), power combining, quadrature-amplitude modulation (QAM), SiGe BiCMOS, stability, ultra-wideband (UWB).**

I. Introduction

The ever-growing demand for high data transmission rates and high spatial sensing accuracy has driven the rapid development of millimeter-wave (mm-Wave) wireless systems in communication, radar and imaging applications. For mm-Wave frequencies, especially in the V, E and W bands [1]–[4], have been attracting great attention and have been researched extensively in B5G/6G wireless communication and sensing systems. Meanwhile, as one of the core features of 6G, integrated sensing and communication (ISAC) is an important development trend for future wireless networks. From the perspective of the RF front-end supporting mm-Wave ISAC systems, wideband operation and superior linearity are required to deal with the sophisticated digital waveforms designed for accurate sensing and reliable communication. As an important building block in a wideband transmitter (TX) front-end (FE), a power amplifier (PA) has a dominant impact on the performance of the entire TX, especially bandwidth (BW) and linearity. Therefore, a wideband, high-gain, high-linearity and efficient PA is needed to meet the requirements of wireless systems.

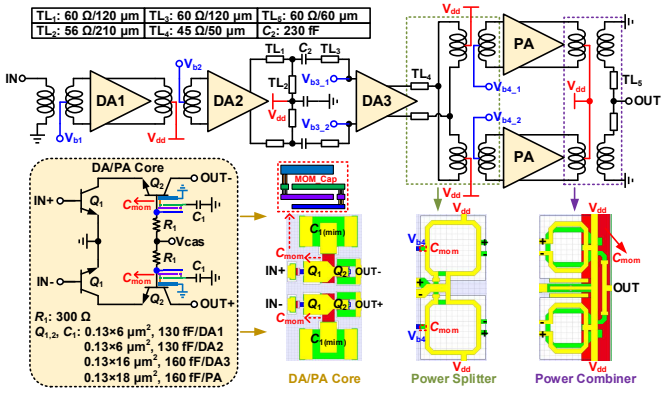
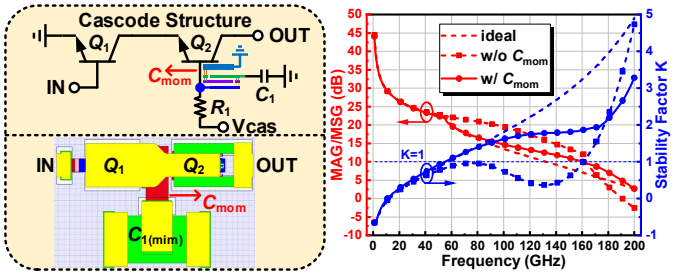


Fig. 1. Schematic of the proposed UWB PA and the layouts of the key passive components.

Compared with III–V compound technologies, silicon-based technologies (CMOS/BiCMOS) have the advantages of low cost and high integration, making them increasingly popular in the design of on-chip systems. However, with the increase of frequency, the performances of transistors and passive devices in silicon-based technologies will decline rapidly, which will limit the gain, output power and efficiency of mm-Wave PAs, and also lead to the deterioration of the stability. A lot of efforts have been made to solve these problems in silicon-based technologies. In order to improve the power gain, a multi-stage cascode structure is commonly used in the design of mm-Wave PAs [1], [5]. Power combining techniques can overcome the power limitation of individual transistor in silicon-based technologies [2], thereby achieving higher output power. However, whether it is multiple stages or multi-way power combining, it will increase the number of transistors, leading to potential instability and low efficiency of mm-Wave PAs, which are very necessary to be addressed. To date, no silicon-based PA that can cover the V, E and W bands simultaneously with a saturated output power (P_{sat}) approaching 20 dBm and a power-added efficiency (PAE) greater than 15% has been reported.

In this paper, a four-stage differential cascode ultra-wideband (UWB) PA which can operate from V to W-band is presented. The metal-oxide-metal (mom) capacitor-based stability-enhancement technique and an adaptive-bias circuit are proposed to improve the stability and linearity of the PA, respectively. In addition, a transformer-based two-way current power combiner is used to further enhance the output power.



(a) (b)

Fig. 2. (a) Cascode structure and its layout with the proposed mom capacitor-based stability-enhancement technique. (b) Simulated MAG/MSG and stability factor K of the differential cascode structure with and without C_{mom} at the transistor size of 0.13×12 μm^2.

II. Circuit Design and Analysis

Fig. 1 presents the schematic of the UWB PA which includes four differential cascode stages with a transformer-based two-way differential power combining architecture at the last stage. The proposed mom capacitor-based stability-enhancement technique and adaptive-bias circuit are adopted in each stage to improve the stability, linearity and efficiency of the PA, respectively. In addition, a compact power splitter is utilized between the last two stages to reduce the chip size.

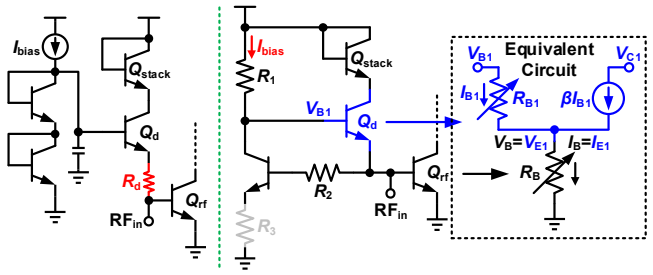
A. MOM Capacitor-Based Stability-Enhancement Technique

For the circuit of DA/PA core shown in Fig. 1, a necessary routing is used to connect the base of transistor Q_2 to a grounded capacitor C_1 in the layout design. This routing can be seen as an inductor and it has a positive-feedback on gain, known as g_m-boosting technique which is commonly used in terahertz circuit design with low transistor gain. However, this routing should be as short as possible while the transistor gain is high enough with a general stability, otherwise the stability will be deteriorated. In the design of the proposed PA, the transistor itself has a sufficient gain within 100 GHz, thus a grounded mom capacitor C_{mom} is placed between the base of transistor Q_2 and the metal-insulator-metal (mim) capacitor C_1, as shown in Fig. 2(a). Since the routing between the base of transistor Q_2 and capacitor C_1 has become a part of C_{mom}, the positive-feedback is greatly reduced.

Fig. 2(b) shows the simulated maximum available/stable gain (MAG/MSG) and stability factor K of the differential cascode structure with and without C_{mom} at the transistor size of 0.13×12 μm^2. Without C_{mom}, the stability factor is below 1 within 160 GHz, means there is potential instability at V, E and W-band. Contrarily, the transistor becomes unconditionally stable with C_{mom} above 55 GHz. Meanwhile, the simulated MAG/MSG and stability factor with C_{mom} are highly consistent with ideal results. It is indicated that the routing between the base of transistor Q_2 and capacitor C_1 has been almost completely absorbed by C_{mom}.

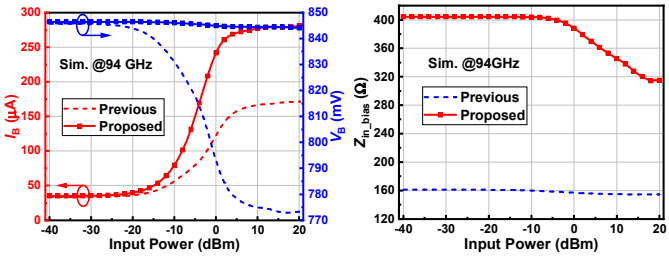
B. Adaptive-Bias Circuit

In communication systems, PAs need to have good linearity and high power back-off efficiency to transmit high-order modulation signals with time-varying envelopes.



(a) (b)

Fig. 3. (a) Previously reported HBT-based adaptive-bias circuit. (b) Proposed adaptive-bias circuit and its equivalent circuit model.



(a) (b)

Fig. 4. Simulated results using the previous and proposed adaptive-bias circuits under the same quiescent condition. (a) Base current I_B and voltage V_B of Q_{rf}, and (b) real part of input impedance of the adaptive-bias circuit versus input power.

Different from the conventional bias circuit which provides a fixed voltage, the adaptive-bias circuit can track the input power level and adjust the bias condition dynamically to avoid premature gain compression and reduce power consumption during power back-off.

Unlike voltage-controlled field-effect transistors (FETs), heterojunction-bipolar transistors (HBTs) are current-controlled devices that require both appropriate voltage and current to be supplied to the base simultaneously. For a HBT-based PA and adaptive-bias circuit, the adaptive-bias circuit should be able to dynamically adjust the current flowing into the base of the RF transistor with the variation of input power and keep the bias voltage as constant as possible. Fig. 3(a) shows the previously reported HBT-based adaptive-bias circuit [5]. The transistor Q_d can provide an increasing base current for the RF transistor Q_{rf} with the increase of input power, and the resistor R_d determines the ratio of input power that could be detected by Q_d. However, the existence of resistor R_d will cause a rapid drop in bias voltage with the increase of input power. Moreover, the input impedance of this adaptive-bias circuit is relatively low, thus leading to the leakage of RF signals.

In order to further improve the linearity and efficiency of a PA, a modified adaptive-bias circuit is proposed and applied in the PA design, as shown in Fig. 3(b). The resistor R_1 can be used at the absence of the external tunable current source. The resistor R_d is removed to make the bias voltage of Q_{rf} more stable, and the resistor R_2 (typically kΩ-level) is utilized to increase the input impedance of the adaptive-bias circuit. According to the equivalent circuit model (R_2 is neglected due to high impedance) shown in Fig. 3(b), the emitter current I_{E1} of Q_d can be derived as

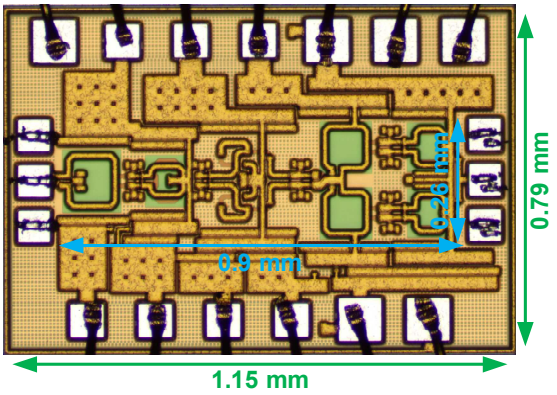


Fig. 5. Die micrograph of the PA.

$$I_{E1} = \frac{V_{B1} - V_{E1}}{R_{B1}}(1+\beta) = \frac{V_{E1}}{R_B}, \quad (1)$$

where R_{B1} and R_B are the base equivalent variable resistors of Q_d and Q_{rf}, respectively, β is the current gain, V_{B1} and V_{E1} are the base and emitter voltages of Q_d, respectively. By eliminating V_{E1} in (1), the expression of V_{B1} can be given as

$$V_{B1} = I_{E1}\left(\frac{R_{B1}}{1+\beta} + R_B\right). \quad (2)$$

With the help of the current source I_{bias}, the V_{B1} in (2) is invariant theoretically. On the contrary, R_{B1} and R_B will decrease with the increase of input power, and the I_{E1} will increase accordingly. In the proposed adaptive-bias circuit, the variation of the bias voltage V_B with the increase of input power can be expressed as

$$\begin{aligned} \Delta V_B &= (I_B + \Delta I)(R_B - \Delta R) - I_B R_B, \\ &= R_B \Delta I - \Delta R (I_B + \Delta I) \end{aligned} \quad (3)$$

where I_B is the base current of Q_{rf}, ΔI and ΔR are the variations of the base current and base equivalent resistor of Q_{rf}, respectively. It can be seen that R_B is greater than ΔR and ΔI is less than I_B+ΔI. Therefore, the value of ΔV_B depends on the change rates of the base current and base equivalent resistor of Q_{rf}.

Fig. 4 shows the simulated results at 94 GHz using the previous and proposed adaptive-bias circuits under the same quiescent condition. It can be seen that the proposed adaptive-bias circuit can provide a larger base current I_B for Q_{rf} than that provided by the previous adaptive-bias circuit with the increase of input power, as shown in Fig. 4(a). The base voltage V_B of Q_{rf} only has a slight decrease with the increase of input power under the proposed adaptive-bias circuit, which is far better than that under the previous adaptive-bias circuit. In addition, the real part of input impedance of the proposed adaptive-bias circuit is much higher than that of the previous adaptive-bias circuit with the increase of input power, as shown in Fig. 4(b). This indicates that the proposed adaptive-bias circuit can effectively avoid the leakage of RF signals and premature gain compression caused by the increase of input power, thereby improving the linearity and efficiency of a PA. It is noteworthy that the resistor R_3 can be used to increase the bias voltage V_B of Q_{rf} in the proposed adaptive-bias circuit.

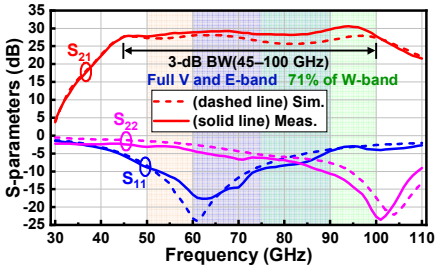


Fig. 6. Simulated and measured S-parameters of the PA.

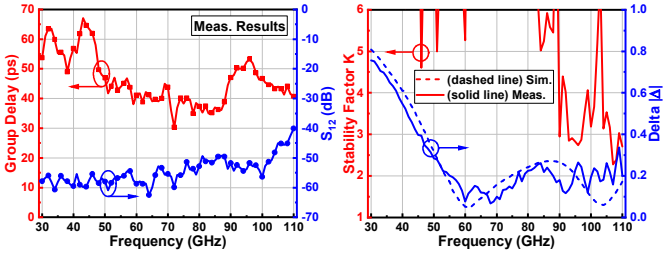


Fig. 7. Simulated and measured (a) group delay and S_{12}, and (b) stability factor K and delta |Δ|.

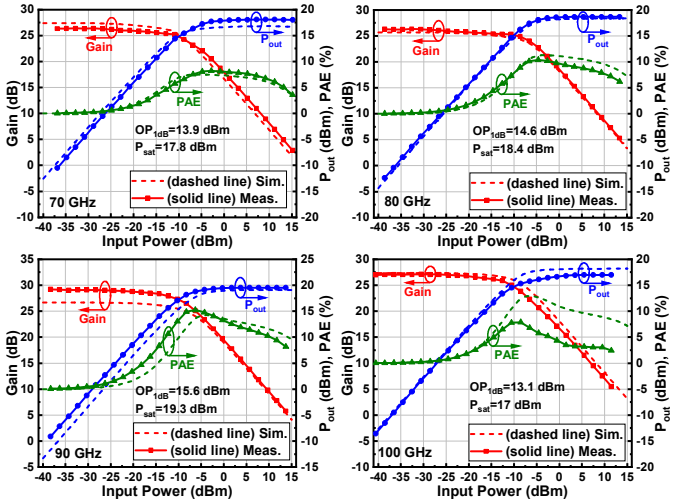
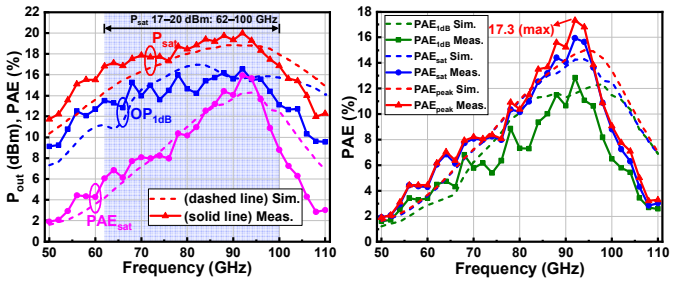


Fig. 8. Simulated and measured output power, PAE and power gain versus input power at 70, 80, 90 and 100 GHz.

III. Measurement Results

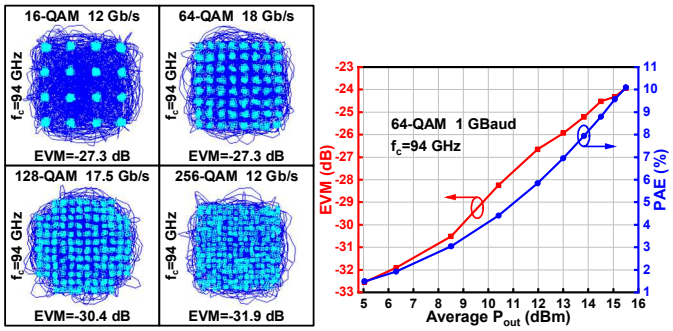
The UWB PA is designed and fabricated in a 0.13-μm SiGe BiCMOS technology. Fig. 5 exhibits the die micrograph of the PA. The overall chip area is 1.15×0.79 mm^2 with a core area of 0.9×0.26 mm^2. With the use of the proposed adaptive-bias circuit in each stage, the PA operates in class AB with a quiescent V_B of 845 mV and consumes a power of 205 mW under a 3.3 V voltage supply.

Fig. 6 shows the simulated and measured S-parameters. The PA achieves a 3-dB gain BW from 45 to 100 GHz with a peak gain of 30.6 dB at 94 GHz. It can be seen that the PA can operate in the full V, E and 71% of W-band. The measured group delay is around 40 ps from 50 to 110 GHz and the measured S_{12} is below –50 dB from 30 to 100 GHz, as presented in Fig. 7(a). The simulated and measured results in



(a) (b)

Fig. 9. Simulated and measured (a) OP_{1dB}, P_{sat} and PAE_{sat}, and (b) three different PAEs versus frequency.



(a) (b)

Fig. 10. Measured (a) constellations using different modulation schemes and (b) EVM and PAE versus average output power for a 1-GBaud 64-QAM signal centered at 94 GHz.

Fig. 7(b) indicate that the PA is unconditionally stable from 30 to 110 GHz.

Fig. 8 shows the simulated and measured output power, PAE and power gain versus input power. The output-referred 1-dB compression points (OP_{1dB}) of the PA are 13.9, 14.6, 15.6 and 13.1 dBm at 70, 80, 90 and 100 GHz, respectively. Fig. 9(a) shows the simulated and measured OP_{1dB}, P_{sat} and PAE_{sat} versus frequency. Fig. 9(b) illustrates the simulated and measured PAE_{1dB}, PAE_{sat} and PAE_{peak} versus frequency. The 3-dB P_{sat} BW ranges from 62 to 100 GHz with a peak P_{sat} of 20 dBm and a peak PAE of 17.3% at 92 GHz. The OP_{1dB} is 16.5 dBm at 92 GHz and still greater than 13 dBm within the entire 3-dB P_{sat} BW.

The PA was also measured with different modulation signals centered at 94 GHz. Fig. 10(a) shows the measured constellations using 16, 64, 128 and 256-quadrature-amplitude modulation (QAM) schemes, respectively. Limited by the BW (92–96 GHz) of the commercial receiver module used in the modulation measurement, the highest data-rate of 18 Gb/s is obtained with –27.3 dB EVM using a 64-QAM signal centered at 94 GHz. Moreover, the PA can also transmit a 1-GBaud single-carrier 64-QAM signal centered at 94 GHz with –24 dB EVM and 10% PAE at an average output power of 15.5 dBm without predistortion, as shown in Fig. 10(b).

Table 1 summarizes the performance of the PA and makes a comparison with other state-of-the-art PAs. It can be seen that the PA achieves the highest gain, GBW, OP_{1dB}, P_{sat} and data-rate. In addition, the PA also has a competitive PAE. To the authors' knowledge, this is the first Si-based PA which can cover the V, E and W bands with a peak P_{sat} of 20 dBm.

Table 1. Performance summary and comparison.

Ref.	**This work**	[1]	[2]	[3]	[4]
Tech.	**130-nm SiGe**	130-nm SiGe	65-nm CMOS	28-nm FD-SOI	65-nm CMOS
Freq. (GHz)	**45~ 100**	68.5~ 90	82.7~ 86.7	97~ 107.3	67.8~ 108.2
Gain (dB)	**30.6**	26.7	29.3	23.7	20.8
GBW (GHz)	**1863**	465	117	158	443
OP_{1dB} (dBm)	**16.5**	16.32	16.2	12.3	11.7
P_{sat} (dBm)	**20**	18.5	19.1	15.1	15.1
PAE (%)	**17.3**	12.9	8.6	18.6	23.1
Data Rate (Gb/s)	**18**	N/A	N/A	N/A	12
P_{DC} (mW)	**205**[#]	N/A	582[#]	N/A	N/A
Area (mm^2)	**0.91 0.23***	0.684	0.72 0.172*	0.32 0.054*	0.039*

*Core area. [#]Quiescent power consumption.

IV. Conclusion

In this paper, an UWB PA with a 3-dB gain BW from 45 to 100 GHz is presented. The proposed mom capacitor-based stability-enhancement technique and adaptive-bias circuit are used to improve the stability, linearity and efficiency of the PA, respectively. The 3-dB P_{sat} BW of the PA ranges from 62 to 100 GHz with a peak P_{sat} of 20 dBm and a peak PAE of 17.3% at 92 GHz. The modulation measurements demonstrate high linearity performance of the PA.

Acknowledgment

This work was supported in part by the National Natural Science Foundation of China under Grant 62188102, and in part by the Fundamental Research Funds for the Central Universities under Grant 2242022k60008.

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