Performance improvement in sub-2nm node Nanosheet-FETs through optimization of spacer interface and dopant activation

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***Abstract*—Nanosheet-based FETs (NSFETs) are replacing FinFETs beyond the 2nm technology node. In these architectures, dopant deactivation and interface carrier trapping become increasingly prominent. This study investigates the impact of phosphorus (de)activation and SiN/Si interface traps in 45 nm gate pitch NSFETs under varying thermal budgets. Through a combination of targeted experiments and TCAD simulations, we predict that mitigating interface traps and optimizing dopant activation in source/drain regions leads to a factor 2.47 increase in drive current at fixed off-current. Finally, we propose a processing alternative to minimize interface trap density in nanosheet channels.**

Keywords—NSFET, GAA, traps, Dit, SiN, thermal budget, inner spacers, dopant activation, diffusion, defects, simulation.

I. Introduction

Nanosheet (NS)-based device architectures have emerged as the successors to the FinFET architecture in industry-leading logic nodes [1-4]. Although Nanosheet-FETs (NSFETs) share most of the processing steps with FinFET devices, two crucial differences are the source/drain (S/D) growth and the role of gate spacers (Fig. 1). Compared to previous architectures, where each S/D region is grown from a single epitaxial seed, epitaxy in gate-all-around (GAA) devices starts from multiple nucleation points and evolves with different growth directions (Fig. 1b). This leads to the formation of extended defects where the different epitaxial seeds merge, which can result in stress relaxation, dopant deactivation and overall device performance degradation [5-7]. At the same time, the GAA nature of NSFETs and the continued shrinking of gate lengths lead to a relative increase of the NS channel interface area with gate spacers versus with the gate stack. The interface of silicon with dielectric spacer materials has been reported to be highly decorated with traps, leading to high interface trap densities (Dit), impacting device performance and reliability in planar devices [8]. An increased Dit contribution in scaled GAA devices is therefore expected.

In this work we show how the combination of experiments targeted at the determination of material properties, in conjunction with calibrated TCAD simulations, reveals the impact of individual contributors to current transport in sub-2nm node NSFET devices. In particular, we show how interface traps at the SiN gate spacers and dopant deactivation in S/D, which both depend on the thermal budget applied, affect the NSFET performance. We propose a new process to reduce interface traps at the nanosheet channel.

II. Devices' performance and Dit investigation

A. Device fabrication and electrical data

The devices investigated in this work are single nanosheet nMOS transistors [9] with process flow depicted in Fig. 1a and dimensions reported in Table 1. The device sub-Fin ground plane (GP) is implanted with boron to form a punch-through stopping layer (PTSL). Gate spacers and inner spacers (ISP) are made of SiN, and the source/drain regions are formed by growing epitaxially in-situ doped Si:P at 670 °C with 3% phosphorus concentration [5]. We define respectively process A and process B as a process without and with an additional rapid thermal annealing (RTA) at 950 °C for 1.5 s following S/D epitaxy (Fig. 1b). The replacement metal gate consists of 1+2+3 nm TiN+TiAl+TiN layers and W filling, while M0 contacts are made with Ti+TiN+W.

The device electrical characteristics normalized by the nanosheet perimeter (W_{eff} = 2(T_{NS} + W_{NS}) = 47 nm) are reported in Fig. 2a for both the linear (V_{ds} = 0.05 V) and the saturation regime (V_{ds} = 0.7 V). A clear boost in drive current is measured for process B, associated with lower access resistance due to the additional thermal anneal as the higher

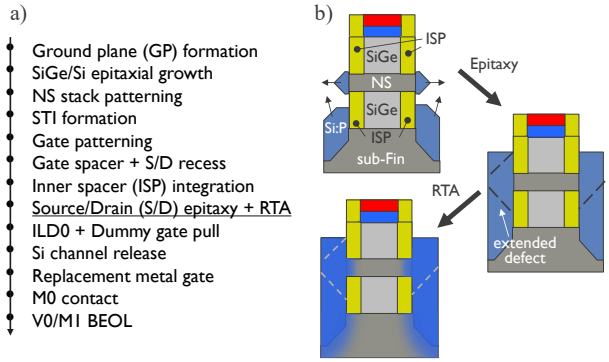

Figure 1: a) Process flow for the fabrication of NSFET devices. b) Detailed look at Si:P S/D epitaxy and rapid thermal anneal (RTA) steps. Dashed lines represent defects formed due to the merging of the different epi growth fronts.

Device dimensions			
Gate pitch (CPP)	45 nm	NS thk. (T_{NS})	5.5 nm
Gate length (L_g)	12 nm	ISP thk. (T_{ISP})	6 nm
NS width (W_{NS})	18 nm	S/D recess (H_{PC})	25 nm

Table 1: Physical device dimensions.

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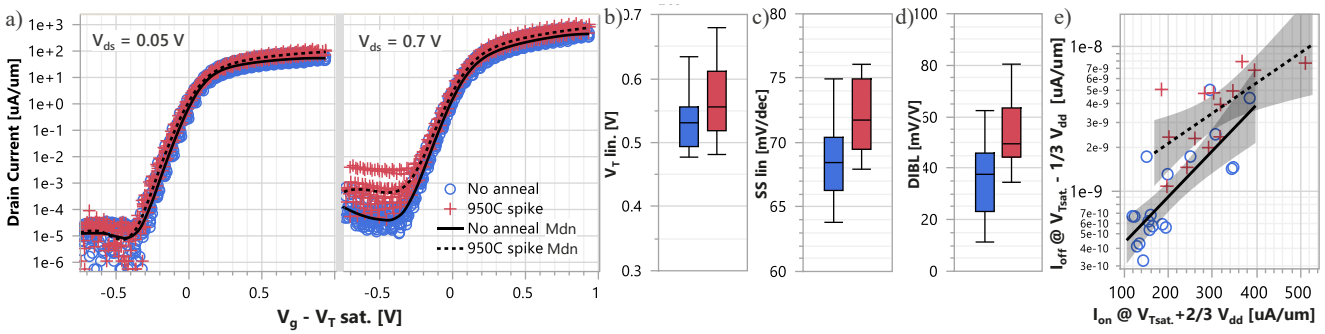

Figure 2: a) Devices I_d-V_g characteristics in the linear (V_{ds} = 0.05 V, left) and saturation regime (V_{ds} = 0.7 V, right), shifted by saturation threshold voltage. b) No clear V_T roll-off is observed for process B even if more dopant diffusion is expected. c, d) Gate control is slightly degraded for process B leading to higher SS and DIBL. e) Larger off current at V_{ds} = 0.7 V leads to decreased I_{on}/I_{off} ratio for process B.

thermal budget leads to improved contact and junction resistivities, as well as enhanced phosphorus diffusion [10, 11]. The threshold voltage of the devices is expected to decrease due to shorter effective gate length in the RTA case. This is not observed (see Fig. 2b), suggesting that additional dopant-independent factors affect device turn-on. Gate control is slightly degraded for process B as seen from the higher subthreshold swing (SS) and drain induced barrier lowering (DIBL) (Fig. 2c, d). Although the off current in the linear regime is not impacted, it is increased in the saturation regime leading to decreased I_{on}/I_{off} ratio when applying an RTA (Fig. 2e). It is observed that the transconductance characteristics of nFETs are significantly degraded, suggesting high interface trap densities at the device channel. As will be shown in Section III.B, it is not possible to explain the magnitude of this degradation by simulating realistic Dit values at the gate stack, which suggests that additional interface traps are introduced by the SiN inner and outer gate spacers.

B. *Investigation of SiN/Si interface traps*

Dit values up to 1×10^{13} $cm^{-2}eV^{-1}$ have been reported at the interface of different gate spacer dielectrics with silicon. The negative charge of the traps depletes the carriers below the gate spacers in planar transistors [8]. To confirm the presence of SiN/Si Dit, we have processed MOS capacitors with plasma-enhanced atomic layer deposition (PEALD) SiN layers as gate oxide. In addition to wafers with different SiN thicknesses, one wafer underwent chemical oxidation (chemox) before SiN deposition, while in another case SiN was replaced by a 4 nm SiO_2 layer grown by rapid thermal oxidation (RTO) to provide a reference point. A 1.9 nm-thick HfO_2 layer was deposited on top of the dielectric layers followed by 5 nm of TiN and finally W gate filling.

The Dit values of MOS capacitors are extracted using the conductance method at a frequency of 100 kHz, and the values extracted from n-well devices on n-Si or p-Si substrates are plotted vs the extracted effective work function (EWF) in Fig. 3. It is observed that the wafer type does not affect the extracted Dit values. The expected high Dit values at the SiN/Si interface are confirmed, especially when a 1.5 s 850 °C post deposition anneal (PDA) in N_2 atmosphere is applied after HfO_2/SiN deposition. This kind of anneal is usually performed after the deposition of high-k (HK) layers in the gate stack to reduce intrinsic defects, although here it is seen to increase the Dit at the SiN/Si interface. The thermal budget of the HK PDA resembles the one experienced by the spacers during RTA after the deposition of S/D regions in process B, except that during the latter the peak temperature is even higher (950 °C).

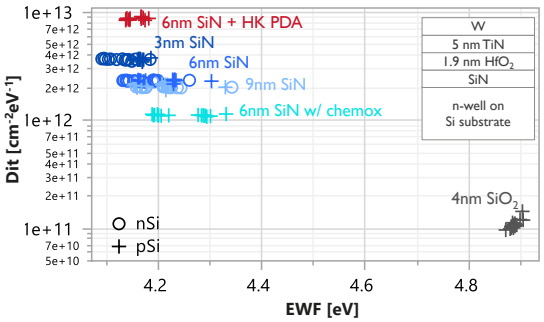

Figure 3: Density of interface trap (Dit) vs effective work function (EWF) extracted from MOS capacitors with different dielectric layers as gate oxide.

III. Impact of Doping (De)Activation and Spacer Dit

To understand more in detail the impact of the additional thermal budget on device performance and interface traps, a TCAD analysis is carried out using Sentaurus SProcess, capturing structural information, dopant diffusion and activation, and SDevice, capturing the current-voltage characteristics [12].

A. *Process simulation*

The device processing is reproduced using layout-based process simulations and different temperature ramps are implemented for process A and B. The S/D and PTSL doping concentrations were measured experimentally through secondary ion mass spectroscopy (SIMS) on blanket test structures, resulting in $[P]_{S/D} \approx 1\times10^{21}$ cm^{-3} and $[B]_{PTSL} \approx 2\times10^{19}$ cm^{-3}, the latter being consistent with the simulated GP implants.

A comparison of the simulated TCAD structure and expected phosphorus chemical distribution with cross-sectional transmission electron microscopy (TEM) and scanning spreading resistance microscopy (SSRM) [13] images is shown in Fig. 4. Due to the higher thermal budget in process B, enhanced dopant diffusion is expected both in the device sub-Fin and NS channel. Although SSRM data shows a clear phosphorus diffusion enhancement in the device

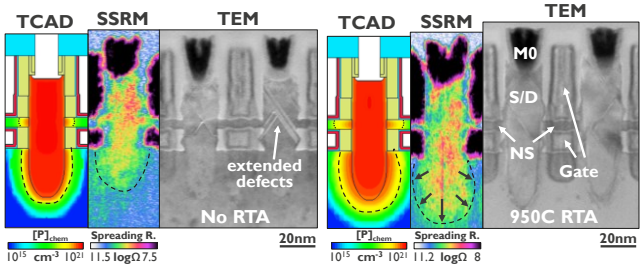

Figure 4: Comparison of TCAD structure (left, M0 and gate not shown) with SSRM and TEM images of devices with and without RTA.

sub-Fin when the RTA is applied, no clear difference is observed in carrier concentration in the nanosheet. Finally, the TEM images show several extended defects in the S/D regions for both processes. These defects likely form when epitaxy seeds from the substrate and from the nanosheet ends merge, although partial recrystallization happens during the anneal in process B [6]. The Boron in the PTSL is simulated to be all active after post-implantation anneal. Given the starting phosphorus chemical concentration and employing the transient cluster model, which implements one type of dopant-defect interaction impacting dopant activation, the simulated active concentration in the S/D regions are $[P]^{A}_{act} = 1.8\times10^{20}$ cm^{-3} and $[P]^{B}_{act} = 4\times10^{20}$ cm^{-3} for process A and B respectively. These values are consistent with the values reported using micro-Hall measurements on planar structures [5].

B. Device simulation and TCAD calibration

Drift diffusion (DD) transport is implemented for device simulations with anisotropic density gradient (DG) corrections to account for quantum confinement effects. Ballistic mobility is calibrated to MonteCarlo methods, and carrier saturation velocity is then tuned to account for the reduction in the magnitude of saturation currents. EOT is fixed to 0.85 nm, and the Ti/Si:P contact resistivity (ρ_c) for different active phosphorus concentrations ($[P]_{act}$) is estimated with the empirical relationship using data from transmission line model (TLM) structures [5, 14]:

$$\rho_c \approx 10^{(8.944 - 0.840*\log10([P]act))}. \quad (1)$$

The Dit values from Fig. 3 are used as initial input for device simulations, while traps at the SiO_2/Si gate interface are kept at 1×10^{11} $cm^{-2}eV^{-1}$. Both case consider a uniform distribution of acceptor traps across the band-gap as an approximation. The gate work function expected for the employed metal stack is in the range of 4.3 - 4.4 eV. In the simulations, the gate work function is tuned to match the threshold voltage of the experimental Id-Vg characteristics.

The Id-Vg characteristics that more closely match the distribution median (see Fig. 2) were selected and used for the calibration of our simulations shown in Fig. 5. An excellent match of the simulations output and the experimental data is achieved after reducing the amount of active dopants compared to what is estimated by process simulations. For process A, the active phosphorus is tuned to 3×10^{19} cm^{-3}, down to 17% of the original active concentration, while for process B, the active phosphorus is reduced to 2×10^{20} cm^{-3}, corresponding to 50% of the original active concentration. TCAD simulations use the values of active dopants to determine the S/D resistivity, so it is possible that they are underestimated to account for the impact of defects on transport, which is not simulated. With this in mind, the active concentrations used for the calibration correspond to phosphorus activation rates of ~3% and ~20% without and with the application of the 950 °C RTA, respectively. The active phosphorus concentration for process A is lower than what has been reported for as-grown Si:P [5, 6], suggesting that extended defects are an obstacle for phosphorus activation in nano-cavities such as S/D regions of GAA transistors.

The values of Dit at the SiN/Si interfaces used in device simulations are $Dit_A = 3\times10^{12}$ $cm^{-2}eV^{-1}$ and $Dit_B = 1.5\times10^{13}$ $cm^{-2}eV^{-1}$, which are consistent with the values extracted experimentally in Fig. 3. Solid evidence for the correct

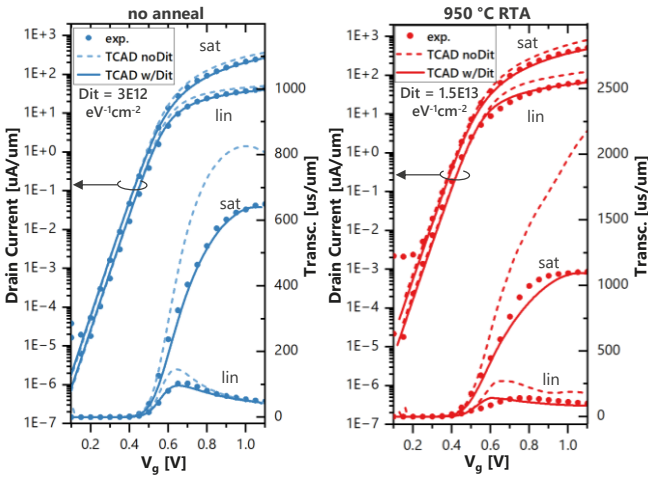

Figure 5: Median I_d-V_g and transconductance characteristics used for TCAD device calibration. A strongly improved agreement is achieved when using the experimental Dit values at SiN/Si interfaces.

modelling of the transport inside the device is given by the significantly improved match in transconductance (g_m) both in the linear and saturation regime. The agreement is not as good for process B, possibly due to the fact that considering a uniform energy distribution is not optimal when considering high trap densities. Note that the calibrated gate work functions for both cases are $WF_{G,A}$ = 4.67 eV and $WF_{G,B}$ = 4.71 eV, which are higher than the expected values, suggesting that fixed charges might delay device turn-on. The simulated linear SS and DIBL simulated are SS_A = 68 mV/dec, SS_B = 70 mV/dec, and $DIBL_A$ = 41 mV/V, $DIBL_B$ = 61 mV/V, again in agreement with median experimental results (see Fig. 2c, d).

C. Predictive NSFETs performance improvement

With the calibrated TCAD models, we explore the potential benefit of optimized spacers and S/D regions on drive current (measured at 0.7 V from a fixed off current of 40 nA/um) and saturation subthreshold swing (Fig. 6). For this purpose, devices were modelled with thinner inner spacers (3 nm compared to the original 6 nm), as well as reduced SiN/Si interface traps (Dit = 1×10^{12} $cm^{-2}eV^{-1}$ instead of the values reported in Fig. 5). Due to the detrimental role of interface traps, the main performance benefit is obtained for both processes when reducing the ISP thickness, resulting in a drive current boost of more than 55% while also improving SS. As this approach leads to increased parasitic capacitance, reducing the overall trap density at the spacer material/Si interfaces is an alternative option. This may result in 25% and 58% drive current increase for process A and B, respectively. For process B, a decrease in Dit is accompanied by a shorter

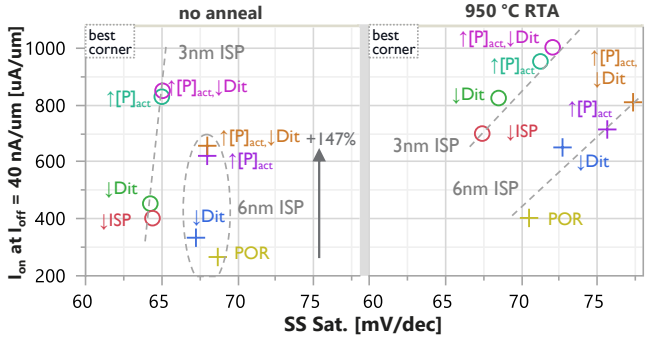

Figure 6: Predicted I_{on} at I_{off} = 40 nA/um + V_{dd} (0.7 V) vs saturation subthreshold swing (SS Sat.) for NSFETs without (left) and with (right) a 950 °C RTA.

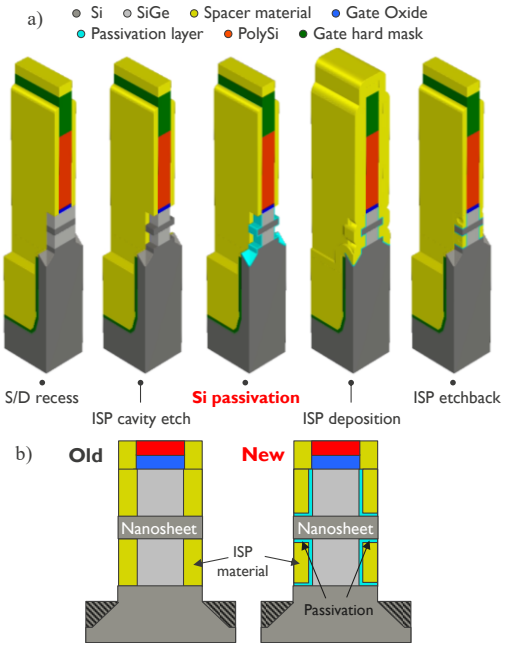

Figure 7: a) Alternative processing scheme including silicon passivation prior to inner spacers deposition and etchback. b) In the new process, an interfacial passivation layer sits between the nanosheet horizontal facets and the ISP material reducing interface trap densities.

L_g effective due to lower carrier trapping in the ISP region which, in this case of enhanced diffusion, results in increased SS. Ideal active phosphorus concentrations (as reported in Section II.A) were also simulated, which correspond to ideal cases where dopant deactivation is limited, for example with the use of a laser anneal [6]. In the case of process A with 6 nm inner spacers, this leads to a factor 2.33 increase in drive current without SS degradation, highlighting how doping deactivation in phosphorus-doped silicon is a crucial obstacle to performance. Considering an additional Dit reduction leads to increased I_{on} at fixed I_{off} by a factor 2.47 compared to the initial baseline.

IV. Channel Passivation Prior to Inner Spacers Deposition

Fig.6 shows that reducing the amount of traps at the interface between gate spacers and the nanosheet channel is an important step towards improved NSFET device performance. Fig. 3 shows that the extracted Dit on MOS capacitors can be three times lower when the silicon surface is passivated using chemical oxidation before SiN deposition. For this reason, a new processing scheme is proposed in Fig. 7. In a conventional process flow, after source/drain recess and inner spacer cavity etch, the inner spacer material (commonly SiN) is conformally deposited, which leads to direct inner spacer dielectric/nanosheet interfaces. To mitigate the trapping phenomena at this interface, inner spacer deposition is preceded by a silicon passivation step. This can be achieved with a silicon oxidation step, or alternatively via the deposition of a passivating layer. As a result, an interfacial passivation occurs on the horizontal facets of the nanosheet channel inside the ISP cavities, thus mitigating the impact of interface traps. The dielectric layers on the channel tips are duly etched back. The thickness of the passivating layer should be controlled to limit potential wet-chemistry leakage paths affecting source/drain integrity during channel release.

V. Conclusions

The combination of targeted experiments and TCAD simulation shows that interface traps at the gate spacer are a significant obstacle to optimal nMOS NSFET device performance. While performing a rapid thermal anneal after S/D growth can lead to defects recrystallization and to increased active phosphorus concentrations, the higher thermal budget also affects the distribution of traps at SiN/Si nanosheet interfaces. By reducing the amount of these traps, up to 58% increase of drive current at fixed off current is expected. Combining realistic lower trap densities with optimized dopant activation in S/D regions can finally lead to a factor 2.47 drive current improvement, without subthreshold swing degradation. A novel processing scheme including nanosheet passivation prior to inner spacer formation is proposed in order to reduce interface trap densities at the nanosheet/inner spacers interfaces.

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