A 11.3-to-14.1 GHz Voltage-Domain Noise-Shaping Fractional-N Digital PLL

Yaqian Sun, Wei Deng, Haikun Jia, Angxiao Yan, Hongzhuo Liu, Junyang Yin and Baoyong Chi
School of Integrated Circuits, Tsinghua University, Beijing, China
wdeng@tsinghua.edu.cn

***Abstract*—In this paper, an all-voltage-domain bang-bang fractional-N PLL with noise shaping is presented. The quantization error cancellation (QE CXL) and noise shaping are implemented in voltage domain with a C-2C DAC, which also serves as the sampling capacitor in the voltage sampler. The proposed QE cancellation based on C-2C DAC avoids the intrinsic nonlinearity in traditional RC-based DTC. Phase detection is also performed in voltage domain with a comparator, acting as a voltage domain BBPD (V-BBPD). The prototype, fabricated in a 65-nm CMOS process, operates at 11.3 to 14.1 GHz. The measured integrated jitter (10 kHz–40 MHz) is 46 fs in integer-N mode and 78 fs in fractional-N mode, without any digital predistortion (DPD). The entire PLL consumes 15 mW and achieves a figure of merit (FoM) of -255 dB and -250 dB for integer-N and fractional-N modes, respectively.**

***Index Terms*—bang-bang phase detector (BBPD), digital to analog converter, noise shaping, PLL**

I. Introduction

Bang-bang digital PLL is particularly appealing due to its low power consumption, compact size, low complexity, and ease of integration into modern scaled CMOS technologies. However, due to the quantization noise of the bang-bang detector, it is difficult for the bang-bang digital PLLs to outperform analog PLLs. Noise shaping BBPD is proposed in [1] to reduce the quantization noise contribution of BBPD. However, while synthesizing fractional-N frequencies, a digital-to-time converter (DTC) is used to remove the quantization error. The RC-based DTC suffers from intrinsic nonlinearity caused by different ramp under different input control words. Other integer-N PLL with noise shaping phase detector is proposed in [2] and [4]. However, their effectiveness has not been verified in fractional-N PLL.

In order to solve the above-mentioned issues, this work proposes a frac-N PLL with QE cancellation, noise shaping, and phase detection all performed in voltage domain. A C-2C DAC is adopted to implement QE cancellation and noise shaping, while also serving as the sampling capacitor. Phase detection is also performed in voltage domain with a voltage comparator. The main advantages of this structure are: 1. The QE compensation is embedded into CDAC by charge sharing, which saves hardware and power consumption overhead; 2. The CDAC acts as a digital-to-voltage converter (DVC), which is ideally linear compared to the RC-based DTC; 3. The noise shaping is achieved with LSBs of the CDAC, without affecting the QE cancellation or adding extra delay generating circuits; 4. Compared to G_m based analog PLL, the voltage comparator used here is insensitive to input offset.

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II. Proposed Noise Shaping Bang-Bang PLL Architecture

The block diagram of the proposed PLL is shown in Fig. 1a. The red block shows the proposed C-2C DAC for QE cancellation and noise shaping. The total capacitance is 2C. Each capacitor's bottom plate can switch to 3 different voltage levels. Meanwhile, the voltage on the top plate of the MSB capacitor V_{s1} changes in binary. Fig. 1b shows the timing diagram of the PLL. When the PLL is in sampling phase, all switches are connected to V_{ref1}, the C-2C DAC acts as a sampling capacitor with a total capacitance of 2C. The current source charges the capacitor with a constant current and the charging time is based on the time error between ref and div. When the charging is complete, the time difference is reflected in the sampling voltage V_{s1}. When the PLL is in QE compensation mode, which is controlled by DVC_clk generated by the multi-phase generator, the switches will be switched to V_{ss} or V_{ref1} or remain unchanged based on the DVC control words generated by DVC logic, resulting in the change of V_{s1} to the desired value.

The $\Delta\Sigma$-modulator operates in MASH1-1 mode, therefore, QE is between 0 and $2T_{VCO}$. In traditional DTC-based frac-N PLL, the DTC should cover the range of $2T_{VCO}$. In the proposed sampling PLL, the sampling point should always fall within the linear region of the SPD. As shown in Fig. 2a, the ideal locking point is in the middle of the PD linear region. Therefore, the reference voltage of the comparator V_{cmp} is set to $V_{dd}/2$. This voltage cannot be set too large or small because it is also the common-mode voltage of the comparator. Since the QE error ranges from 0 to $2T_{VCO}$, the SPD linear range should be larger than $4T_{VCO}$. Sadly, the left-half part is wasted and this limits the largest achievable SPD gain.

In this work, we made some improvements to the $\Delta\Sigma$-modulator and proposed two-way QE cancellation scheme. By adding a minus-1 offset to the QE error, the QE error range is changed to $-T_{VCO}$ to T_{VCO}. As shown in Fig. 2b, both left and right sides of the locking point are used, and the

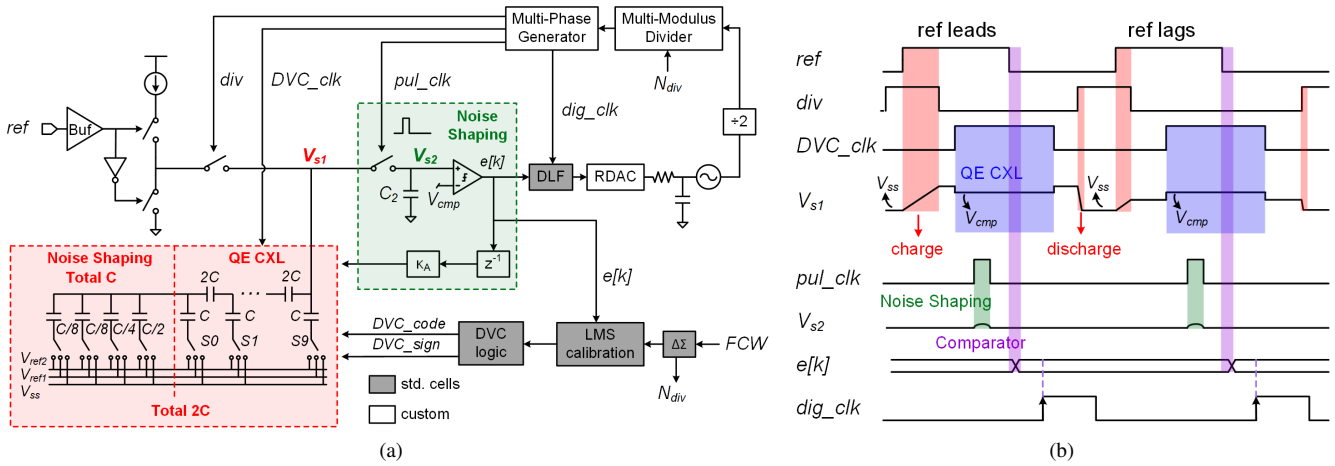


Fig. 1. (a) Proposed block diagram of the PLL; (b) Timing diagram of the PLL.

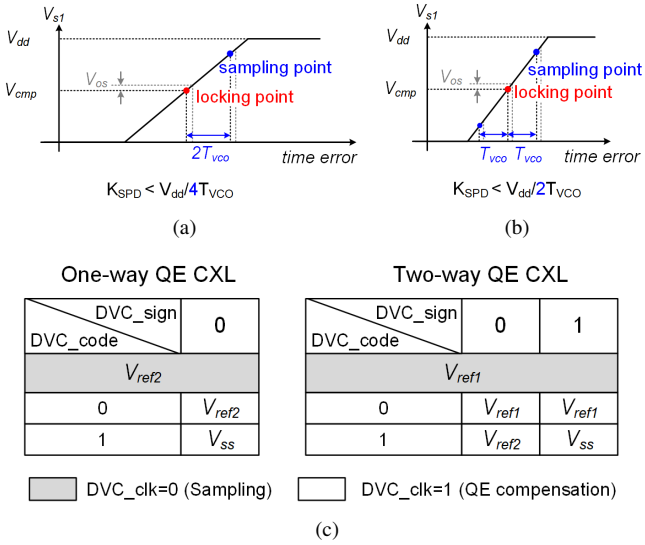


Fig. 2. (a) Owo-way QE CXL; (b) Two-way QE CXL; (c) DVC switch logic.

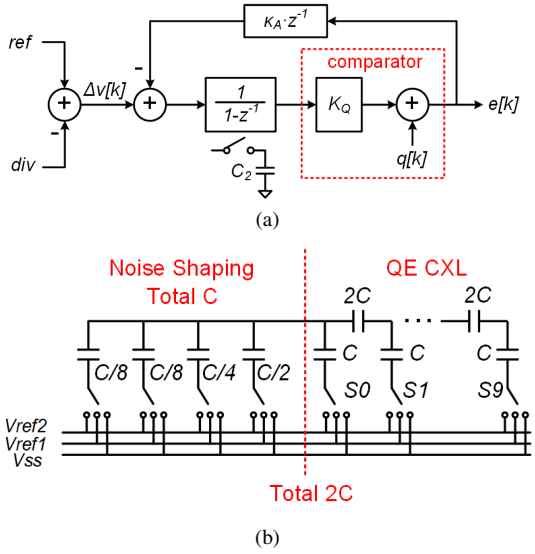


Fig. 3. (a) Linear model of the noise shaping scheme; (b) Noise shaping implemented in C-2C DAC.

largest achievable SPD gain is doubled compared to one-way QE cancellation in Fig. 2a. The DVC logic outputs both the value and sign of the C-2C control word. The DVC switch logic is shown in Fig. 2c.

Moreover, the voltage comparator is insensitive to input offset. If the comparator has an input offset of V_{os}, as shown in Fig. 1a with gray dash line, only the locking point will move from $V_{dd}/2$ to $V_{dd}/2 + V_{os}$. As long as the margin is larger than V_{os}, the sampling points still fall within the linear region of the SPD.

A. Noise Shaping Technique in Voltage Domain

The noise shaping scheme in the green box in Fig. 1a is modeled as the linear model as shown in Fig. 3a. The charging SPD detects the time difference Δt between ref and div and converts it to voltage Δv. The charge sharing between C-2C DAC and C_2 can be approximately modeled as an integrator. The voltage comparator is modeled as a gain block K_Q with quantization noise $q[k]$. With noise shaping, the input-referred quantization noise $q_{\Delta v}(z)$ is

$$q_{\Delta v}(z) = q(z) \cdot \frac{NTF(z)}{STF(z)} = q(z) \cdot \frac{1 - z^{-1}}{K_Q}, \qquad (1)$$

where NTF and STF is the noise transfer function and signal transfer function, respectively. Equation (1) reveals that the input-referred quantization noise of the voltage comparator is shaped by $(1 - z^{-1})$, a first-order $\Delta\Sigma$ modulator, and also suppressed by K_Q. When $\kappa_A = K_{SPD} \cdot \sigma_{\Delta v}$, K_Q has a maximum value, where $\sigma_{\Delta v}$ is the standard deviation of the time difference between ref and div in locked state.

The noise shaping can be implemented in the same C-2C DAC, as shown in Fig. 3b. The LSB capacitor of the C-2C DAC is split into 4 smaller capacitors with binary weight, keeping the total capacitance of 2C unchanged. The higher

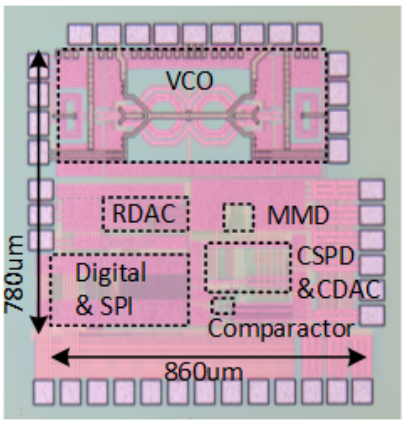
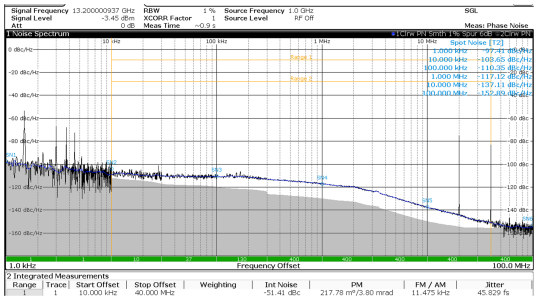
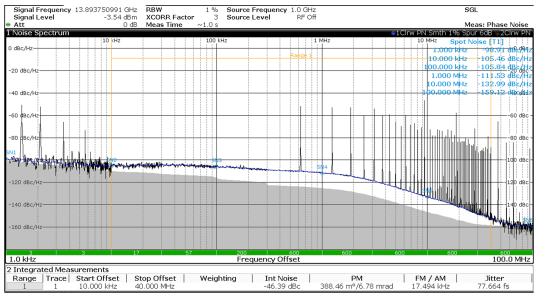


Fig. 4. Die micrograph.



(a)



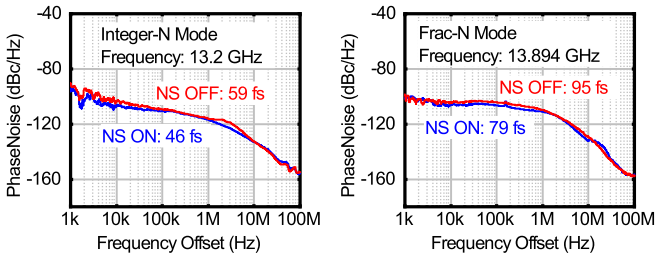
(b)

Fig. 5. Measured phase noise. (a) Integer-N Mode; (b) Frac-N Mode.

10 bits of the C-2C DAC are used for quantization error cancellation, while the lower 4 bits are used for noise shaping.

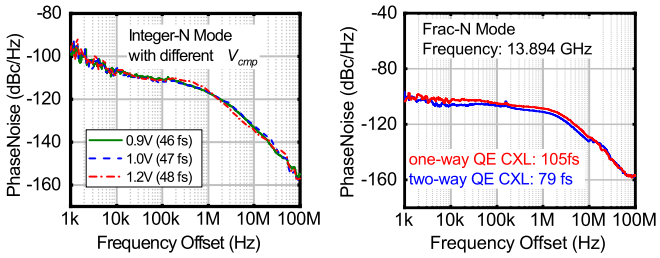
III. Circuit Implementation

Back to the block diagram shown in Fig. 1a, the VCO is implemented with a dual-core class-F topology [3], covering a frequency range of 11.3-to-14.1 GHz. With third-harmonic shaping, the output voltage is shaped into a pseudo-square oscillation waveform, reducing the impulse sensitivity function (ISF). The VCO is followed by a $\div 2$ divider based on a true single phase clock (TSPC) DFF, which divides the VCO frequency down to $\sim$6 GHz. Next, the multi-modulus divider (MMD), whose first two stages are implemented in TSPC logic while the subsequent stages use CMOS logic, divides this $\sim$6 GHz signal to reference frequency.



(a) (b)

Fig. 6. Comparison of measured phase noise (a) wi/wo noise shaping in integer-N Mode; (b) in frac-N Mode.



(a) (b)

Fig. 7. Comparison of measured phase noise with (a) different V_{cmp}; (b) one/two-way QE CXL.

Multi-phase generator (MPG) generates the clock signals for other blocks and ensures the correct phase relationships. As shown in Fig. 1b, first, when ref and div are both 1, the current source charges the CDAC. Second, after the falling edge of div, the charging ends and DVC_clk turns 1, enabling the QE cancellation and noise shaping process by switching the switches in C-2C DAC. This process is based on charge sharing and is rather fast. After that, pul_clk enables the charge sharing between CDAC and C_2. Third, at the falling edge of ref, the voltage comparator compares V_{s2} and V_{cmp} and outputs the 1-bit result $e[k]$. After that, dig_clk samples the result which is already prepared. Last, DVC_clk returns to 0 and resets the switches in C-2C DAC and then the C-2C DAC is discharged, getting ready for the next cycle.

IV. Measurement Results

The chip was fabricated in a 65nm CMOS process. The die micrograph is shown in Fig. 4. The PLL occupies 0.28 mm^2 area and dissipates 15 mW (excluding input and output buffers). The PLL has a tuning range of 11.3 to 14.1 GHz, synthesized from a 300 MHz external reference signal. The measured phase noise is shown in Fig. 5. The integer-N mode was measured at 13.2 GHz, achieving an integrated jitter of 46 fs (10 kHz-40 MHz). The random frac-N mode was measured at 13.894 GHz, with an integrated jitter of 78 fs. The performance difference between integer-N and fractional-N mode is because digital pre-distortion (DPD) is not employed. Fig. 6 shows the comparison of the measured phase noise with and without noise shaping both in integer-N mode and frac-N

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORK

	This work	JSSC'22 [1]	ESSERC'24 [2]	JSSC'25 [4]	JSSC'21 [5]	JSSC'22 [6]
Type	Frac-N	Frac-N	Integer-N	Integer-N	Frac-N	Integer-N
PLL Architecture	Digital	Digital	Digital	Digital	Analog	Analog
Noise Shaping	NS V-BBPD[b]	NS T-BBPD[c]	NS T-BBPD	NS ADC	No	No
Output Frequency (GHz)	11.3-14.1	12.9-15.1	4.2-5.8	4.3	7.7-9.1	9.6-12
Ref. Frequency (MHz)	300	250	50	134	100	100
Integer-N Jitter w/ Noise Shaping (fs)	46	69.5	305	133	121	48.6
Integer-N Jitter w/o Noise Shaping (fs)	55	76	556	520	N/A	N/A
Frac-N Jitter w/ Noise Shaping (fs)	78	79.7	N/A	N/A	135	N/A
Frac-N Jitter w/o Noise Shaping (fs)	126	87	N/A	N/A	N/A	N/A
Integration BW (Hz)	10k to 40M	1k to 100M	10k to 100M	1k to 100M	10k to 50M	1k to 100M
Power (mW)	15	10.8	2.5	13.7	4.5	5
FoM[a] Integer-N Mode (dB)	-255	N/A	-246.3	-249	-251.8	-259.2
FoM[a] Frac-N Mode (dB)	-250	-251.5	N/A	N/A	-250.8	N/A
Process (nm)	65	28	65	28	45	40
Active Area (mm^2)	0.28	0.21	0.12	0.27	0.1	0.13

[a] $\text{FoM} = 10\log_{10}[(\text{Power}/1\text{mW}) \cdot (\text{Jitter}/1\text{s})^2]$

[b] Voltage-domain BBPD [c] Time-domain BBPD

mode, both exhibit jitter reduction close to 20%. Fig. 7a shows the measured phase noise under different reference voltage of the comparator. As discussed above, the PLL is insensitive to the offset of the comparator. Fig. 7b shows the comparison of phase noise between one-way and two-way QE cancellation scheme. The jitter-power figure of merit (FoM) of the PLL is -255 dB for the integer-N mode and -250 dB for the fractional-N mode. A performance comparison table with state-of-the-art noise shaping PLLs is provided in Table I.

V. CONCLUSION

This paper presents a voltage-domain fractional-N digital PLL with noise shaping. The QE cancellation and noise shaping are implemented in the same C-2C DAC, which also acts as the sampling capacitor in the voltage sampler. Phase detection is also performed in voltage domain with a voltage comparator. With this architecture, this prototype achieves an integrated rms jitter of 46 fs in integer-N mode and 78 fs in fractional-N mode. With a power dissipation of 15 mW, the resulting jitter-power product is -255 dB in integer-N mode and -250 dB in fractional-N mode, which is comparable with noise shaping PLLs both in integer-N and fractional-N mode, and competitive with PLLs without noise shaping techniques.

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