Cryogenic performance assessment of FD-SOI transistors with counter-doped channel

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***Abstract*—We investigate the cryogenic performance of Fully Depleted Silicon-on-Insulator (FD-SOI) transistors, focusing on devices featuring counter-doped channels. We explore counter-doping as a potential strategy to mitigate the increased threshold voltage at cryogenic temperatures, aiming to reduce power consumption. We extract key performance metrics such as threshold voltage, subthreshold swing, and other relevant parameters from cryogenic measurements, and compare them against conventional FD-SOI devices. Our results demonstrate that counter-doping enables effective threshold voltage control without compromising electrical performance, positioning it as a promising solution for ultra-low-power cryogenic CMOS optimization in scalable quantum computing applications.**

***Index Terms*—Fully Depleted Silicon-on-Insulator (FD-SOI), Cryogenic CMOS, Counter-Doping, Threshold voltage, MOSFET, and Quantum Computing.**

I. Introduction

Cryogenic-CMOS is an emerging field with significant potential to drive advancements in large-scale quantum systems[1, 2] as well as high-energy physics[3]. Among the state-of-the-art CMOS technologies, Fully Depleted Silicon-on-Insulator (FD-SOI) is a strong candidate for addressing the demands of cryogenic environments. The FD-SOI technology offers superior electrostatic control, lower power consumption, and enhanced performance compared to bulk CMOS devices, making them well-suited for both analog and digital applications at cryogenic temperatures[4]. Predominantly, the technology's inherent back-biasing capability allows for dynamic threshold voltage (V_T) adjustment[5], enabling further optimization of performance and power efficiency, especially at cryogenic temperatures.

While back-biasing is an effective approach for V_T tuning, one significant disadvantage is the potential increase in leakage currents, particularly when the back-bias voltage is not properly restricted at higher voltages. Alternatively, approaches based on process modifications like backplane doping[6–8], gate-stack engineering[9–11], and channel counter-doping[12–15] can be used in combination with back-biasing to fine-tune the threshold voltage, thereby delivering a multi-V_T ultra-wide voltage range of operation. The performance and effectiveness of these techniques remain largely unexplored, particularly at cryogenic temperatures, where changes in dopant ionization levels and carrier freeze-out effects can significantly impact the device characteristics. This highlights the need for a detailed evaluation of these devices under cryogenic conditions.

In this work, we specifically focus on the cryogenic performance of transistors with a counter-doped channel. Through extensive electrical characterization, we extract and analyze key performance metrics at cryogenic temperatures, comparing them to those of conventional FD-SOI transistors. Our findings indicate a slight degradation in the off-state performance of nMOS devices, possibly due to the higher implantation dose used for nMOS compared to pMOS. However, at cryogenic temperatures, we observed no significant changes or degradation in critical parameters, such as transconductance and subthreshold swing. Overall, counter-doping proves to be a highly effective technique for V_T compensation, with a reduction of approximately $150\,\mathrm{mV}$ to $200\,\mathrm{mV}$ for counter-doped devices at zero back-bias (ZBB) without sacrificing electrical performance. This demonstrates the potential of counter-doping for optimizing device operation in cryogenic environments while maintaining low power consumption.

II. Methodology and Sample Details

We performed measurements on two distinct wafers, both fabricated using an FD-SOI process of GlobalFoundries. The first wafer features a more conventional-like FD-SOI channel, while the second incorporates a counter-doped channel, achieved through an additional dopant implantation step into the SOI channel. For simplicity, we refer to the former as the 'standard' wafer and the latter as the 'doped' wafer.

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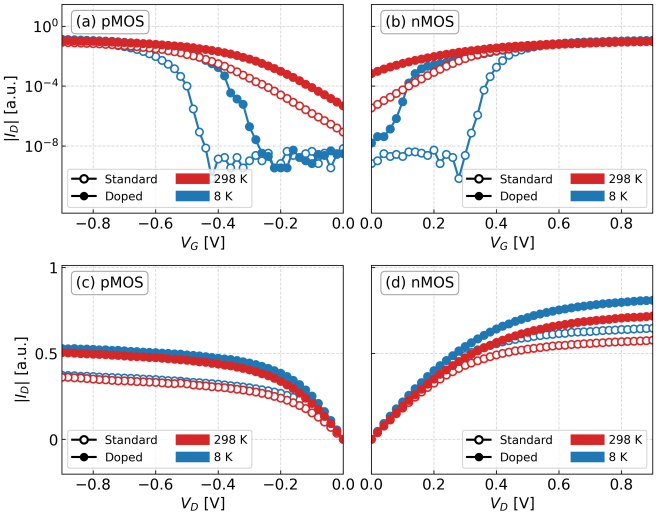

Fig. 1. (a-b) Measured transfer curves and (c-d) output curves of pMOS and nMOS transistors respectively at 8 K and 298 K. Curves are recorded in the linear mode ($|V_{D,lin}|$) and at $V_B = 0$. The currents are normalized to the maximum value.

For both wafers, transistors with different device dimensions were characterized from room temperature (RT) down to a base temperature of 8 K, including intermediate temperature steps. DC current-voltage (I-V) characteristics were obtained at each temperature step for different bias configurations, including the forward body biasing (FBB) conditions. We used an AttoDRY800 closed-cycle cryostat combined with a Keysight B1500 Semiconductor Analyzer to cool down the samples and record the I-V measurements respectively[16].

Although a wide selection of lengths and widths of these transistors were measured, only the small gate-length devices with approximately 4:1 width-to-length ratio, are discussed in this paper.

III. DC Cryogenic Characterization

The transfer characteristics of both 'standard' and 'doped' transistors measured at room temperature (RT) and 8 K are presented in Figure 1(a) and (b). These measurements were taken with zero back bias (ZBB) and in the linear mode of operation, i.e. at a minimal drain-source voltage ($|V_{D,lin}|$). At 8 K (blue traces), the transfer curves for both 'standard' and 'doped' devices shift towards higher absolute gate voltages ($|V_G|$).

A steeper transition from off- to on-state is observed at 8 K compared to RT due to the expected reduction of thermal voltage and phonon scattering. This also translates directly to the relatively higher currents at RT (red traces) for $V_G = 0$ V. The curves of the 'doped' devices (with filled markers) are shifted toward lower gate voltages at both RT and 8 K as compared to that of the standard devices, indicating a clear reduction of V_T induced by the counter-doping process.

Figure 1(c) and (d) show a comparison of output curves for the same devices in Figure 1(a) and (b) respectively. Current gain due to both cryogenic environment and counter-doping

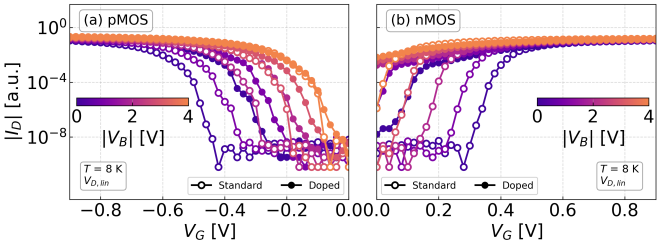

Fig. 2. Measured transfer curves of (a) pMOS and (b) nMOS transistors at 8 K for different forward body bias conditions. Curves are recorded in the linear mode ($|V_{D,lin}|$). The currents are normalized with respect to the maximum value.

effect is observed for both pMOS and nMOS devices. The current gain due to temperature for pMOS devices is comparatively smaller than that observed for nMOS devices. This is attributed to the differences in carrier mobility enhancement between electrons and holes at cryogenic temperatures.

Figure 2 shows the transfer curves for FBB configurations highlighting the impact of back bias on both 'standard' and 'doped' devices at 8 K. Evidently, the curves are shifted towards lower $|V_G|$ with increasing $|V_B|$ value, illustrating the uniform threshold control using FBB for both 'standard' and 'doped' devices. It can also be seen that applying a higher FBB to the 'doped' nMOS device forces the devices to remain almost in the on-state.

IV. Parameter Extraction

Using the measured I-V curves discussed in section III, critical device parameters are extracted and compared for both 'standard' and 'doped' devices. At first, we extracted the V_T values for the devices at all the bias configurations and temperature steps. The threshold voltages were determined using the constant current method[17]. In our case, we opted for a relatively higher reference level compared to the typical order of 1×10^{-7}A. This choice was made because the 'doped' devices exhibit significantly higher off-state currents than this typical level, leading to a negative V_T value, where we lack the measured data.

The V_T shifts observed towards lower values (as seen in Figure 2) with increasing FBB become even more apparent in Figure 3, which displays the extracted V_T values at 8 K plotted along with RT data. In general, a reduction of approximately 150 mV to 200 mV in V_T is observed due to counter-doping. It can be seen that the V_T values for the 'standard' device at RT (red circles) and the 'doped' device at 8 K (blue discs) are nearly aligned. This is seen for both nMOS and pMOS cases indicating an almost perfect compensation of the V_T at 8 K to match the 'standard' RT behavior.

Furthermore, we extracted the body factors or the back-bias coefficients from the slopes of the data in Figure 3 as $\gamma = |\Delta V_T/\Delta V_B|$. These values are summarized in Table I, and agree with the already reported values for conventional short-channel FDSOI devices measured at both RT and cryogenic temperatures[18, 19]. The lower γ values for pMOS devices are expected because the position of the inversion layer

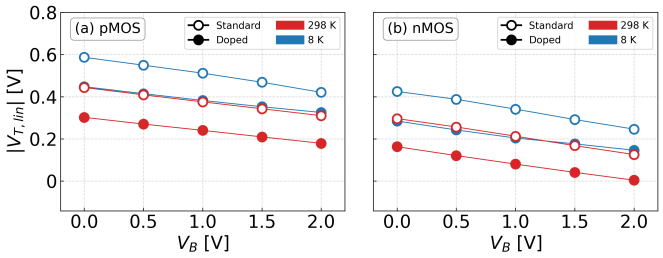

Fig. 3. Extracted threshold voltage values of (a) pMOS and (b) nMOS transistors plotted against the applied back-bias at 8 K and 298 K. The values are extracted at $|V_{D,lin}|$.

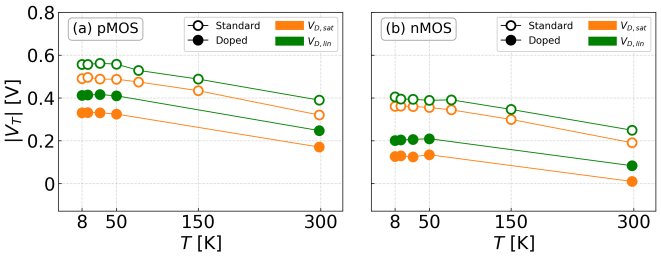

Fig. 4. Extracted threshold voltage values of (a) pMOS and (b) nMOS transistors plotted against the temperature at ZBB ($V_B = 0$ V).

TABLE I
ABSOLUTE VALUES OF BODY FACTOR (γ) AT RT AND CT FOR 'STANDARD' AND 'DOPED' DEVICES. ALL VALUES ARE IN $\mathrm{mV\,V^{-1}}$.

Die Type	pMOS		nMOS	
	8 K	298 K	8 K	298 K
Standard	78.4	67.2	89.2	85.7
Doped	63.5	61.6	72.6	81.1

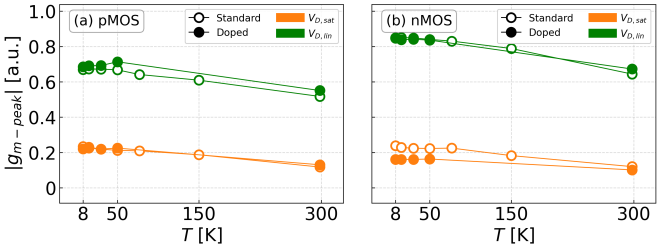

Fig. 5. Peak transconductance values of (a) pMOS and (b) nMOS transistors plotted against the temperature at ZBB ($V_B = 0$ V). The transconductance values are normalized with respect to the maximum value.

in the channel varies depending on the type of carriers and the channel material[20]. Additionally, the γ values for 'doped' transistors are also lower in comparison to the 'standard' devices for both pMOS and nMOS cases irrespective of temperature indicating a lower sensitivity of the back bias to the V_T.

Concerning the temperature dependence of the threshold voltage, Figure 4 shows the extracted V_T values at ZBB for linear ($|V_{D,lin}|$) and saturation ($|V_{D,sat}|$) modes. A common trend of V_T saturation towards cryogenic temperatures ($T < 50$ K) is observed for all the devices due to carrier freeze-out irrespective of the applied drain-source voltage. The V_T values extracted in the saturation mode are roughly 50 mV to 70 mV higher than the values in the linear mode because of the reduced potential barrier at $|V_{D,sat}|$. The difference in V_T values between 'standard' and 'doped' devices remains more or less the same across both pMOS and nMOS transistors throughout the entire temperature range. pMOS devices consistently exhibit a threshold voltage around 100 mV to 150 mV higher than that of nMOS devices as this is process-defined.

Figure 5 shows the peak transconductance (g_{m-peak}) values plotted against temperature extracted in both linear and saturation modes. The g_{m-peak} parameter indicates optimal current-driving capability and plays a critical role in determining gain, speed, and frequency response in analog circuits. A similar temperature dependence is also seen for the g_{m-peak} as seen in the case of V_T in Figure 4. However, the values of g_{m-peak} for the 'standard' and 'doped' devices are comparable without large deviations for all temperatures. This suggests that the counter-doping process has minimal or no impact on the g_{m-peak} metric. On the contrary, a current gain of roughly 20% is observed because of the counter-doping, which can be seen from the extracted on-current values from Figure 6(a). The off-current (Figure 6(b)) exhibits minimal sensitivity to the counter-doping for the pMOS device, while the nMOS device shows an increased off-current, likely due to a higher implantation dose. As expected, the off-currents are increasing with temperature due to the increased thermal energy of the carriers.

The subthreshold swing (SS) was extracted first for all data points in the subthreshold region as $SS = \partial V_G / \partial(\log_{10} I_D)$ for at least two orders of magnitude. The average of these values is plotted as SS_{avg} against temperature in Figure 7. It is important to note that for higher back bias, the off-currents are particularly high, especially for nMOS devices. As a result, the extracted SS values may not be fully confined to the subthreshold regime.

In general, a decreasing trend in the SS_{avg} is observed as the temperature decreases. Additionally, the plot shows the ideal SS values plotted against temperature as per the Boltzmann limit, obtained from SS $= \ln(10)kT/q$ where k is the Boltzmann constant, T is the temperature, and q is the elementary charge. Deviations from the ideal linear behavior can be seen for both 'doped' and regular devices, with the experimental values diverging from the theoretical curve, particularly at lower temperatures. This deviation, typically called SS saturation, has been consistently reported for transistors fabricated in different technologies[21] and is primarily attributed to the interfacial defects. Minor degradation of SS is seen for the 'doped' devices which is a direct consequence of the increased off-currents. However, this could be improved by further optimization of the counter-doping process.

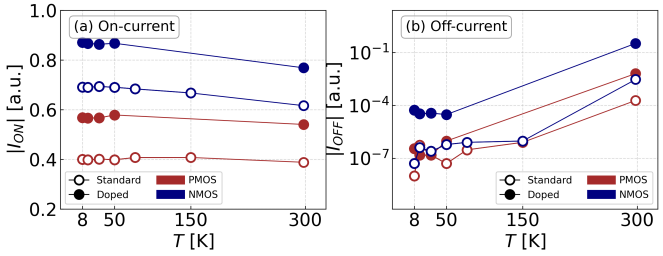

Fig. 6. Extracted (a) on- and (b) off-currents of pMOS and nMOS transistors plotted against the temperature at ZBB ($V_B = 0$ V). The on-current is extracted at $|V_G| = |V_D| = |V_{D,sat}|$ V and the off-current is extracted at $|V_G| = 0$ V.

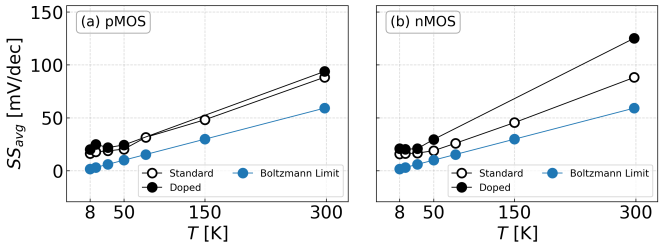

Fig. 7. Extracted SS of (a) pMOS and (b) nMOS transistors plotted against the temperature at zero back-bias ($V_B = 0$ V).

V. Conclusion

In summary, this work demonstrates the potential of channel counter-doping as an effective technique for tuning the threshold voltage of FD-SOI transistors, particularly in cryogenic environments. By enabling precise adjustments to the threshold voltage, counter-doping offers greater control over transistor behavior, which is crucial for optimizing power consumption and performance in systems constrained by the limited cooling power of dilution refrigerators. We roughly estimate that a 200 mV reduction in V_T could enable a 10-20% reduction in supply voltage, leading to approximately 20-30% dynamic power savings. While these results are encouraging, further investigation is needed to refine counter-doping levels to mitigate potential increases in leakage currents. Other factors such as noise characteristics, device variability, and mismatch issues require further exploration. Nevertheless, our work provides a starting point for the evaluation of counter-doped devices, especially at cryogenic temperatures.

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