A 30V, 0.1CV^2f, 224-level Fractional-N Supply Multiplying Pulser

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***Abstract*— This paper presents a 30V, 224-level fractional-N supply-multiplying pulser. A self-level-shifting latch circuit is also proposed to enable automatic level shifting of the gate-driving signal during the supply-boosting operation. Fabricated in an 180nm BCD process, the driver generates fine-grain, amplitude-controlled pulses up to 32.5V from a 5V input and operates up to 2 MHz, offering high efficiency and outperforming previous designs in control granularity.**

Keywords—Pulse generation, switched-capacitor converter, LDO, transducer driver, supply voltage multiplying, fractional-N, high power reduction, amplitude control.

I. Introduction

Electrostatic and piezoelectric transducers have become critical components in various emerging applications such as imaging, communications, haptics, and microrobotics [1–11]. These transducers are driven by high-voltage pulse drivers to generate amplitude-controlled outputs required for these applications, as shown in Figure 1. However, a major challenge arises from the substantial parasitic capacitance inherent in these transducers, which leads to high dynamic power (CV^2f) consumption and ultimately degrades the overall power efficiency of the system.

Recent research has focused on developing a novel high-voltage pulser that can minimize this reactive power loss. Charge-redistribution [5,6], energy-replenishing [7], and charge-recycling [8] techniques demonstrate a 30–80% reduction in CV^2f loss. However, these techniques not only require a high external supply voltage but also offer very limited or no control over pulse amplitude. For these class-D type drivers, pulse width modulation can be used to control the amplitude of the transducer output. However, high driving frequency(f), multiplied by the oversampling ratio, results in increased power loss.

Series-parallel switched capacitor circuit-based drivers [9–11] generate a high-voltage pulse signal from a low supply voltage by sequentially switching the flying capacitors from parallel to series. This eliminates the need for a high supply voltage and significantly reduces CV^2f loss. However, the pulse amplitude can only be controlled in integer multiples of the input supply voltage, and the complex level shifting of gate-driving circuits increase the design complexity.

II. Proposed Fractional-N Supply Multiplying Pulser

In this work, we present a fractional-N supply multiplying driver that provides a high-voltage pulse with precise amplitude control while simultaneously minimizing reactive power loss. Figure 2 shows the top diagram of the proposed pulser. The LDO regulator, controlled by a 5-bit Fine input, generates the main driver's supply voltage (V_{DDR})

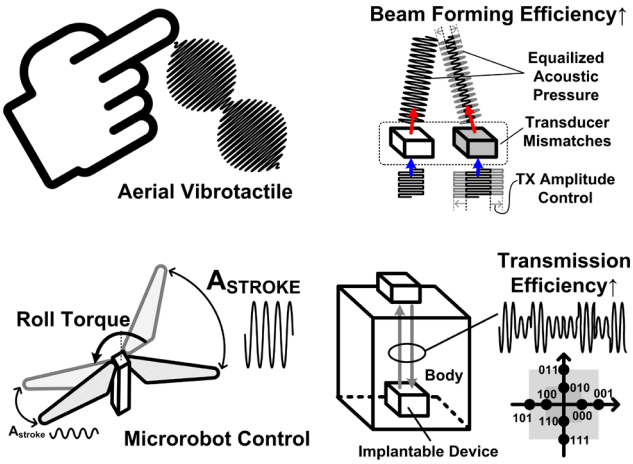

Fig. 1. Emerging applications for high-voltage, amplitude-controlled pulse drivers.

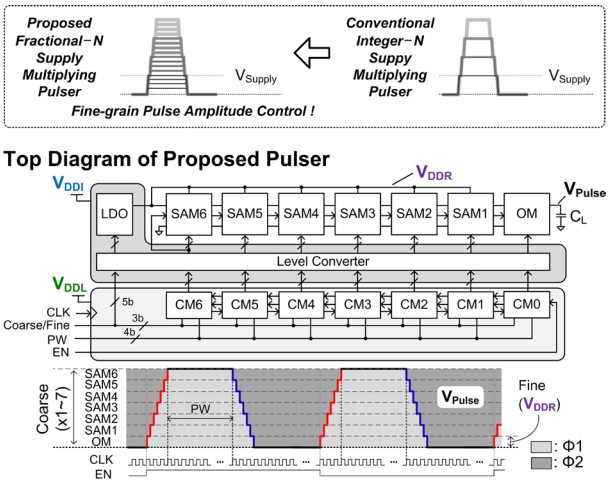

Fig. 2. Top diagram of the proposed fractional-N supply multiplying pulser.

from the input supply voltage (V_{DDI}). The main driver consists of six Supply Adder Modules (SAM1–6) and one Output Module (OM). The SAMs and OM operate in two phases: Φ1 and Φ2. As the operation progresses sequentially from OM to SAM6, transitioning from phase Φ2 to Φ1, the output pulse voltage (V_{Pulse}) rises. Conversely, as the transition shifts from phase Φ1 to Φ2, V_{Pulse} decreases. The 3-bit Coarse input (000–110) is applied to the control module (CM) to determine the V_{DDR} multiplication factor, which defines the amplitude of V_{Pulse}. Thus, using Coarse/Fine control, the proposed pulser can generate 224 levels of V_{Pulse} amplitude, achieving fractional-N multiplication of V_{DDI}. The period of V_{Pulse} is determined by the toggling period of the input signal EN, and the pulse width is controlled by a 4-

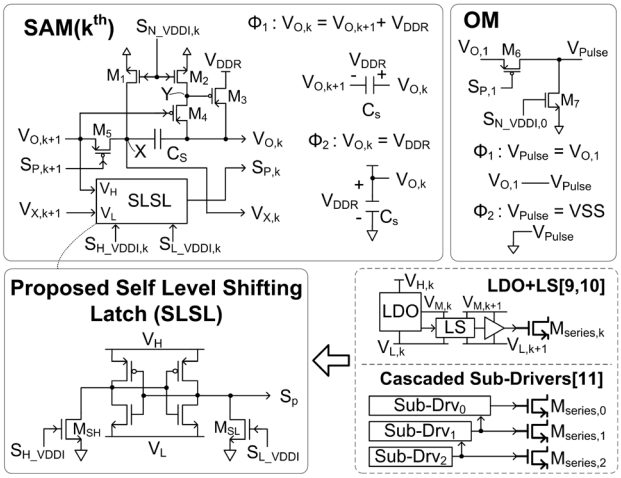

Fig. 3. Circuit diagram of the SAM, OM, and SLSL.

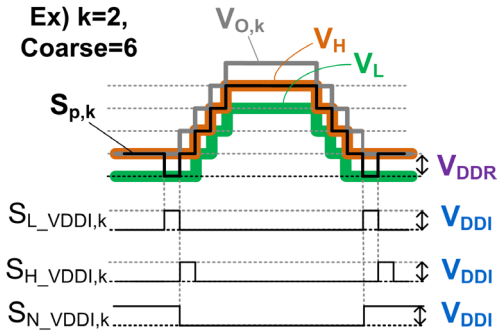

Fig. 4. Signal diagram of SAM2 when Coarse=6.

bit PW signal. The CM operates at a low-voltage supply V_{DDL} and controls the main driver through V_{DDL}-to-V_{DDI} logic level converters.

Figure 3 and 4 show the circuit and signal diagram of the SAM and OM. Each module is composed of high-voltage transistors with $|V_{GS}|_{MAX}$ of 5V. The OM outputs a ground value during the Φ2 phase or its input ($V_{O,1}$) during the Φ1 phase. The k^{th} SAM operates as follows: In the Φ2 phase, transistor M_3 turns on, and the module outputs V_{DDR}. In the Φ1 phase, transistor M_5 turns on, and the module adds V_{DDR} from its input ($V_{O,k+1}$). Here, capacitor C_S always stores V_{DDR} in both the Φ1 and Φ2 phase. Thus, when $V_{O,k}$ reaches the value of $V_{O,k+1}+V_{DDR}$, transistor M_4 turns on, causing M_3 to turn off. When the $(k+1)^{th}$ module switches to phase Φ1, $V_{O,k+1}$ also increases by V_{DDR}. At this point, the k^{th} module's M_5 switch must be on, so its gate signal $S_{P,k+1}$ also needs to increase by V_{DDR}.

The proposed simple self-level shifting latch (SLSL) automatically tracks $V_{O,k}$ changes for $S_{P,k}$ signal generation. $V_{O,k+1}$ and $V_{X,k+1}$ are connected to the supply rails V_H and V_L of SLSL, respectively. Since there is a storage capacitor C_S between $V_{O,k+1}$ and $V_{X,k+1}$, the voltage difference between them is always equal to V_{DDR}. When both the $(k-1)^{th}$ and k^{th} SAM are in the Φ2 phase, V_H is V_{DDR}, and V_L is at the ground level. In this state, $S_{P,k}$ should be V_{DDR} to turn off M_5 in the $(k-1)^{th}$ SAM. To switch the $(k-1)^{th}$ SAM from the Φ2 to the Φ1 phase, the S_{L_VDDI} signal is applied to set $S_{P,k}$ to the ground level, turning on M_5 in the $(k-1)^{th}$ SAM. Next, as the k^{th} SAM transitions from the Φ2 phase to the Φ1 phase, $V_{O,k}$

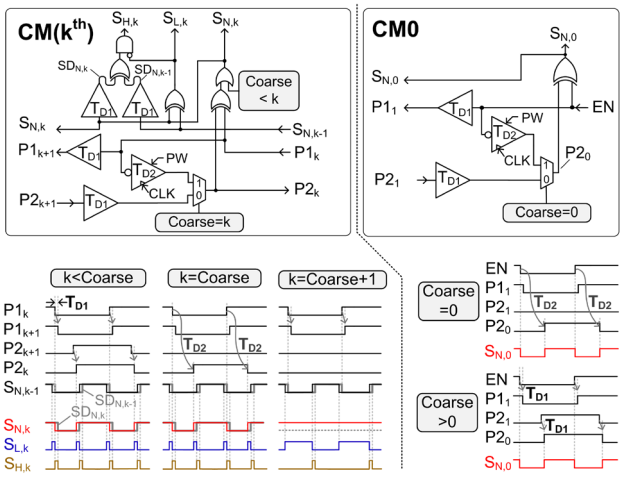

Fig. 5. Circuit diagram of the CMs and the timing diagram of the control signals. $S_{N,k}$, $S_{L,k}$, and $S_{H,k}$ are, respectively, $S_{N\_VDDI,k}$, $S_{L\_VDDI,k}$, $S_{H\_VDDI,k}$ after the level converter.

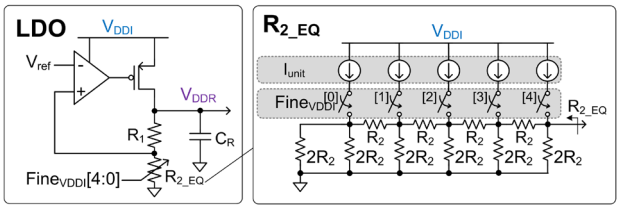

Fig. 6. Circuit diagram of the LDO

rises to $2\times V_{DDR}$. At this point, the S_{H_VDDI} signal is applied to set $S_{P,k}$ to V_{DDR}. Subsequently, when the $(k+1)^{th}$ module switches to the Φ1 phase, $V_{O,k+1}$ rises to $2\times V_{DDR}$, causing $V_{O,k}$ to reach $3\times V_{DDR}$. Meanwhile, V_H of SLSL also rises to $2\times V_{DDR}$, automatically increasing $S_{P,k}$ to $2\times V_{DDR}$. Therefore, with the proposed SLSL circuit, the key control signal $S_{P,k}$ is seamlessly self-level shifted during the supply multiplication process. It should be noted that previous supply-multiplying pulser required complex level-shifting circuits [9,10] or cascaded sub-driver circuits [11] for series-parallel switching control.

Figure 5 shows the circuit diagrams of CM0 and CM1–6 for pulse amplitude and pulse width control. All CMs are implemented with low-voltage logic transistors. Each CM includes two types of delay cells: T_{D1}, which determines the Φ1/Φ2 switching time, and T_{D2}, which determines the pulse width. T_{D1} is implemented with a current-starved delay line, while T_{D2} is implemented as a counter synchronized with the CLK signal to generate a delay of $PW\times T_{CLK}$. When Coarse=0, CM0 inverts the EN signal and then delays it using T_{D2} to produce the $P2_0$. The signal $S_{N,0}$, which controls the NMOS switch M_7 in the OM, is generated by XORing EN and $P2_0$. Consequently, if $S_{N,0}$=0, the OM is in the Φ1 phase; if $S_{N,0}$=1, the OM is in the Φ2 phase. Thus, the OM generates a pulse signal with an amplitude of V_{DDR} and a pulse width of T_{D2}. When Coarse=1, CM0 delays the EN signal by T_{D1} before passing it to CM1, producing the $P1_1$ signal. This means that after the OM switches from Φ2 to Φ1, SAM1 will switch to the Φ1 after a delay of T_{D1}. In CM1, the $P1_1$ is inverted and delayed by T_{D2} to generate $P2_1$. Here, $S_{N,1}$ is obtained by XORing $P1_1$ and $P2_1$. As a result, SAM1 remains in the Φ1 phase for a duration of T_{D2}, generating a pulse amplitude of $2\times V_{DDR}$ in T_{D2}. Then, $P2_1$ is delayed by

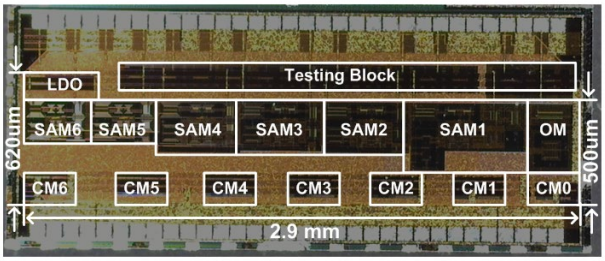

Fig. 7. Chip microphotograph.

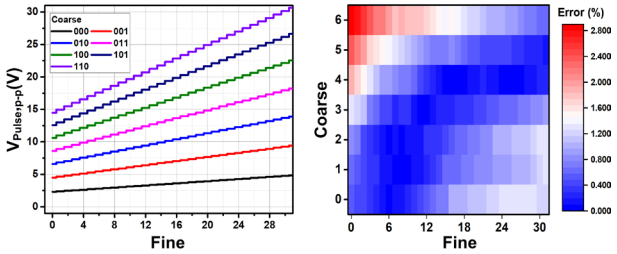

Fig. 8. Measured V_{Pulse} amplitude (left) and error (right) versus Coarse/Fine control code.

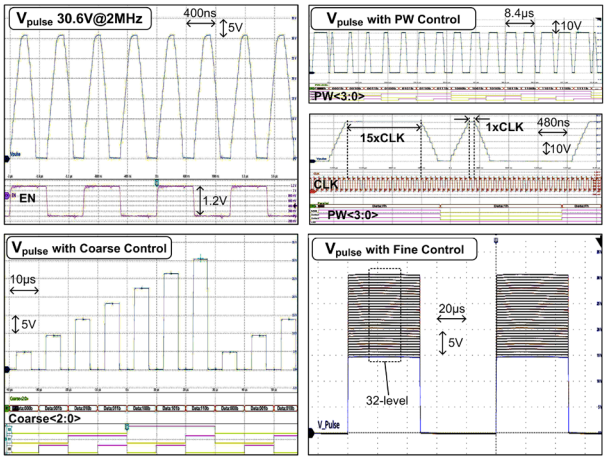

Fig. 9. Measured transient response with Coarse/Fine/PW control.

T_{D1} in CM0 before generating $P2_0$, causing the OM waits for T_{D1} before switching to the Φ2 phase after SAM1 transitions to Φ2. When the coarse value is 2 or higher, each CM module operates in the same manner. In summary, the proposed CM circuit enables simultaneous control of both pulse amplitude and pulse width. The detailed timing diagram for the OM/SAMs control signals is also shown in Figure 5.

Figure 6 shows the circuit diagram of the LDO for V_{DDR} control. An R-2R ladder structure, controlled by the Fine code, is used to determine equivalent resistance R_{2_EQ}, which generates $V_{DDR} = (1+R_1/R_{2\_EQ})\times V_{REF}$. Ideally, the final pulse amplitude should be (Coarse+1)×V_{DDR}. However, to accurately estimate the pulse amplitude, the charge sharing between the parasitic capacitor C_P at each SAM's output node ($V_{O,k}$) and C_S must be considered. Assuming that C_P is identical across all modules and that the Coarse value is N>0, the pulse amplitude A_N can be expressed in following equation (1): $A_N=[C_N\times V_{DDR}+(C_N+C_P+C_L)\times A_{N-1}]/(C_N+C_P+C_L)$ where $C_N=C_S//(C_{N-1}+C_P)$ when N>1 or $=C_S$ when N=1. The initial condition is $A_0 = V_{DDR}$.

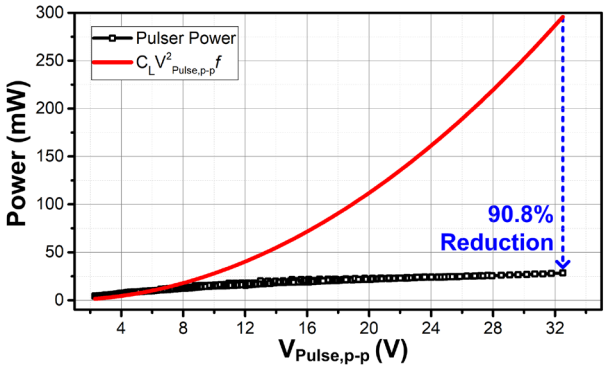

Fig. 10. Measured power consumption of the pulser with a 56 nF C_L and a 5kHz pulse frequency.

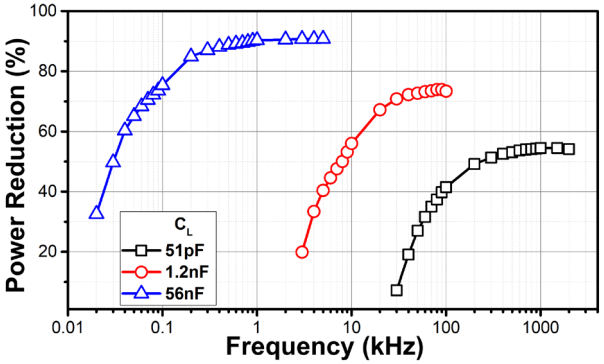

Fig. 11. Measured power reduction relative to $C_LV^2_{Pulse,\ p\text{-}p}f$.

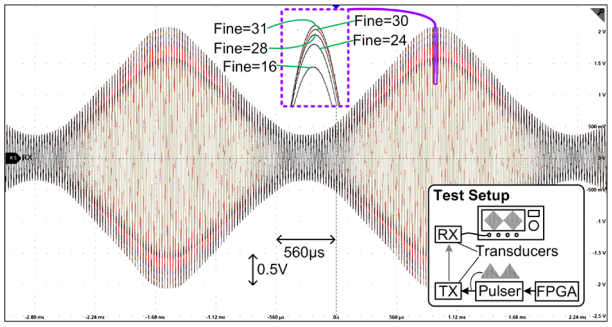

Fig. 12. Measured amplitude modulated RX signal at the transducer output.

III. Chip Measurements

The proposed pulser was fabricated using an 180nm BCD CMOS process (Fig.7). Figure 8 shows the measured pulse amplitude for each Coarse/Fine code and the maximum error between measured values and the theoretical values predicted by Equation (1). These results are based on measurements from nine chip samples bonded to a PCB with external passive components of 0402 size 2.7nF C_S with 10% capacitance tolerance. For theoretical value calculations, a post-layout extracted C_P=1.64pF was used. The supply voltages were set to V_{DDI}=5V and V_{DDL}=1.2V. The load capacitance is 51pF. The result clearly demonstrates fractional-N multiplication of the 5V V_{DDI} to 224-level (7 Coarse × 32 Fine) pulse amplitude ranging from 2.3V to 30.6V. Despite the open-loop control scheme and the large capacitance tolerance of the passive components, the maximum error was measured less than 3%. Figure 9 shows the measured transient response of the prototype driver for various amplitudes and pulse widths.

TABLE I
COMPARISON TO PRIOR WORKS.

	This Work	Choi TCAS-II'21[11]	Li ISSCC23'[10]	Lee ISSCC'19[8]	Choi ISSCC'21[7]	Pelgrims ESSCIRC'21[6]	Chen JSSC'13[5]
Process	180nm BCD	180nm BCD	180nm SOI BCD	180nm CMOS	180nm BCD	180nm BCD	180nm BCD
Supply Voltage	**1.2V, 5V**	1.2V, 5V	3.7V	13.2V	30V	36V	30V
Max Output Voltage	**32.5V**	28.7V	300V	13.2V	30V	36V	30V
Output Level	**224-level**	6-level	Fixed	8-level	Fixed	Fixed	Fixed
Max Output Freq.	**2MHz**	1MHz	30kHz	10MHz	1MHz	250kHz	5.2MHz
Load	0.051-56nF	0.055-1nF	0.1-15nF	N.A	820pF	30-240pF	40pF
Reactive Power Reduction Technique	Series Parallel Supply Multiplication	Series Parallel Supply Multiplication	Series Parallel Supply Multiplication	Charge Recycling	Energy-Replenishing	Step-wise Charging + Charge Recycling	Step-wise Charging
Power Reduction (vs. CV^2f)	90.8% @56nF&5kHz	75.4% @1nF&100kHz	92.2% @2nF&1.7kHz	32.8%	73.1%	80% @235pF&250kHz	38% @3.3MHz
Area	1.5mm^2	1.6mm^2	1.2mm^2	N.A.	5.43mm^2	0.16mm^2	N.A.
External Devices	Capacitor x 7 (C_S x 6 + C_R)	Capacitor x5	Inductor x2 + Capacitor x 16	No	Inductor x1	Capacitor x5	Capacitor x2

Figure 10 shows the measured power consumption of the pulser with a 56nF load and a 5kHz pulse frequency. The results indicate that the power reduction effect is achieved across most of the output range, with a peak reduction of 90.8% compared to $C_LV^2_{Pulse,p\text{-}p}f$ at a 32.5V output. When the output voltage falls below 6V, power loss in the LDO becomes the dominant factor, leading to higher power consumption than $C_LV^2_{Pulse,p\text{-}p}f$. In other words, power reduction is most effective when reactive power loss is the primary contributor. Figure 11 further demonstrates that power reduction is more significant at larger C_L and higher pulser frequencies.

The effectiveness of the proposed pulser in achieving precise and fine-grained amplitude control is demonstrated using ultrasound TRX transducers. The implemented pulser drives the TX transducer (Vurch, V40AN10T) at a 40 kHz pulse frequency with triangular amplitude modulation. The air-transmitted ultrasound signal is received by the RX transducer (Vurch, V40AN10R), and the measured RX signal at the transducer output is shown in Figure 12.

Table I shows the comparison to the recent transducer driver works [5–11]. This work is the only one demonstrating fractional-N input supply voltage to pulse amplitude multiplication. While offering 28× finer amplitude control than the previous state-of-the-art [8], the proposed pulser achieves a peak power reduction of 90.8% relative to $C_LV^2_{Pulse,p\text{-}p}f$ (@5kHz, C_L=56nF, C_s=10μF). Additionally, this work demonstrates the ability to generate high-voltage (>30V) pulses at the highest frequency of 2MHz without requiring a high-voltage supply.

IV. CONCLUSION

In this work, we introduced a fractional-N supply multiplying pulser architecture for high-efficiency, high-voltage, amplitude-controlled pulse generation using low voltage supply of 1.2V and 5V. The SLSL-based control signal generation eliminates the need for complex auxiliary circuits for switching control. The proposed pulser, implemented in an 180nm BCD process, achieves a peak 90.8% power reduction. It offers 28× finer amplitude control compared to the previous state-of-the-art, while maintaining an amplitude error below 3%.

ACKNOWLEDGMENT

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