

# TexCAC: A 22nm 4.8mm<sup>2</sup> 18pJ/cycle Direct-Textile-Attachable Microcontroller Integrating 2MB MRAM for the Command and Control of Advanced Smart Textiles

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**Abstract**—We present TexCAC, the world’s first direct-textile-attachable, NVM-based MCU for the command and control of advanced smart textiles. Fabricated in 22nm, it occupies merely 4.8mm<sup>2</sup> while integrating 2MB MRAM—offering a 4× ~ 114× increase in NVM capacity over state-of-the-art designs of comparable or larger area. Measured fully on-textile, TexCAC achieves an optimal active energy of 18pJ/cycle at 0.52V, rivaling the efficiency of leading MCU implementations.

**Index Terms**—advanced smart textile, command and control, direct die attachment, microcontroller, MRAM

## I. INTRODUCTION

Advanced smart textiles (AST) are textile-integrated electronic systems [1] that enable a wide range of applications, including health care, robotics, and IoT [1], [2]. Fig. 1 (top) shows a typical AST framework, with a command-and-control (CAC) module at its core that coordinates various textile components for cohesive operation. The AST operation flow in Fig. 1 (bottom-right) highlights the critical role of CAC—covering system firmware storage and boot, haptics control, system timing synchronization, and data retrieval. This central role underscores the need for an MCU optimized for ASTs. However, existing AST prototypes, such as the one in Fig. 1 (bottom-left) or [3], often rely on commercial off-the-shelf (COTS) or custom MCUs [4] that require large-footprint interposer boards unsuitable for low-profile, body-conforming, and frequently flexed scenarios. Moreover, most COTS MCUs include non-essential peripherals, inflating both area and power, which conflicts with the strict energy constraints typical of battery-powered ASTs. While the SoC in [5] is tailored for AST sensor control and supports *direct die attachment* (DDA) on textile to minimize footprint, it lacks non-volatile memory (NVM) and self-boot capability, rendering it unsuitable as the root CAC module of AST.

In this work, we present TexCAC, a compact MCU optimized for AST CAC and designed for DDA on textile. By employing MRAM as NVM, TexCAC gains significant advantages (Fig. 1, bottom-left) over the eFlash [6], [7] in most COTS MCUs, with the 2MB capacity enabling storage of complex system firmware as well as neural network weights for on-textile intelligence [8]. TexCAC introduces three key

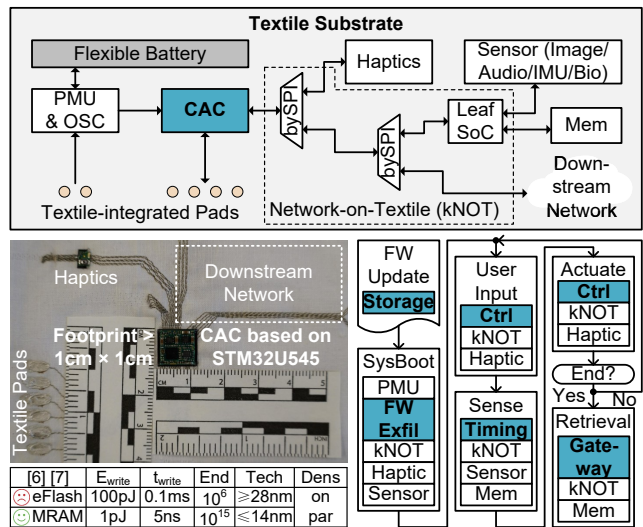


Fig. 1. AST framework (top); a realistic AST with CAC based on interposer-integrated COTS eFlash MCU (bottom-left); typical AST operation flow with CAC functions colored blue (bottom-right).

innovations: 1) I/O streamlining techniques that reduce bond pad (BP) count and die area by 60%, facilitating textile integration; 2) a fully autonomous boot loader supporting a novel MRAM-backed program context switching (CTXSW) scheme that boosts program size capacity by 16×; and 3) an optimization combining dynamic frequency scaling (DFS) with MRAM power gating (PG) to reduce data exfiltration energy by 40%. To the best of our knowledge, TexCAC is the world’s first direct-textile-attachable, NVM-based MCU.

## II. TEXCAC ARCHITECTURE

Fig. 2 shows the SoC architecture of TexCAC, interconnected through 32-bit ARM AHB. At its core is an ARM Cortex-M33 subsystem for programmable AST control, including 128kB IMEM and 128kB DMEM. A dedicated boot loader autonomously initializes TexCAC upon power-on and manages advanced features such as DFS and CTXSW. For external communication, an RX interface connects TexCAC to a host or off-AST devices, while a TX interface transmits

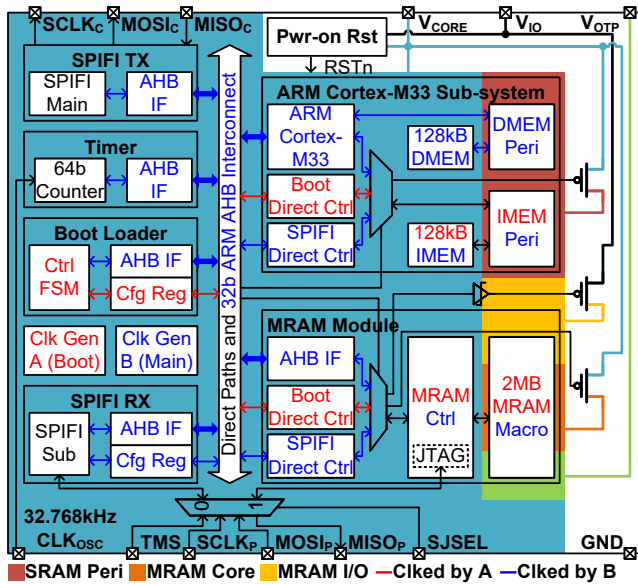


Fig. 2. SoC architecture of TexCAC.

data to downstream chiplets on the textile. The SoC integrates a 2MB MRAM macro for non-volatile firmware storage, taking advantage of MRAM’s high endurance, rapid write speeds, and low power consumption, as noted earlier. Lastly, a timer module distributes timing to other AST components for synchronized operation.

### III. DESIGN OPTIMIZATIONS

#### A. I/O Streamlining for Textile Attachment

DDA on textile requires large BPs with wide pitch along a single chip edge (Fig. 3, top-left), consuming excessive die area proportional to pad count. To address this, we employ SPI for fabric integration (SPIFI) [5] in place of conventional SPI (Fig. 3, top-right). SPIFI is a three-wire variant of bypass-SPI [9], designed to mitigate textile fanout challenges via network-on-textiles (kNOT) [5], effectively removing one pad per SPI interface. We further reduce I/O complexity by merging power domains and interfaces—such as SPIFI RX with MRAM JTAG—cutting pad count by two. A notable example is the reconfigurable SPIFI TX module (Fig. 3, bottom), which supports on-chip clock probing and M33 message printing (the *printf()* function via *chCLK* and *chDAT*), eliminating ten pads without compromising essential functionality. Altogether, these measures trim the total pad count from 32 to 13—a 60% die footprint reduction—and simplify direct die-to-yarn attachment, thereby significantly enhancing the robustness of TexCAC textile integration.

#### B. Boot Loading and Context Switching

As the root of an AST, TexCAC necessitates fully autonomous boot via its boot loading circuit (Fig. 4, top) and the flow depicted in Fig. 4 (bottom-left). A dual-clock scheme is employed: *clka* boots the chip and *clkb* drives the main program. This design avoids a clock modifying its own frequency, eliminating glitch-free clock generator requirements

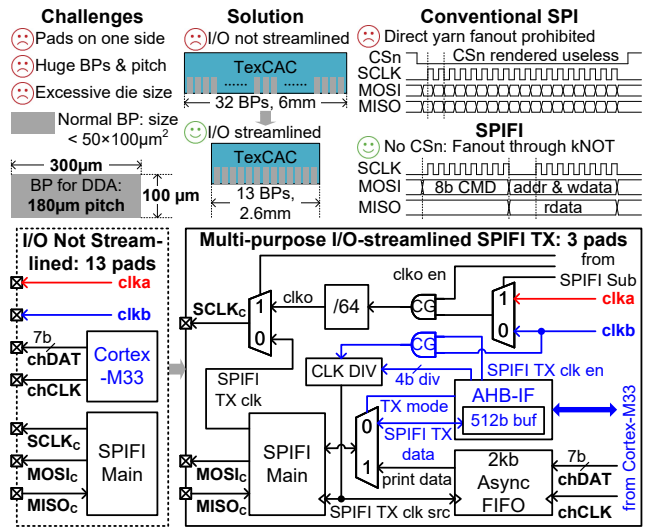


Fig. 3. Challenges of DDA on textile and solution (top-left); SPIFI vs. conventional SPI (top-right); TexCAC SPIFI TX module design (bottom).

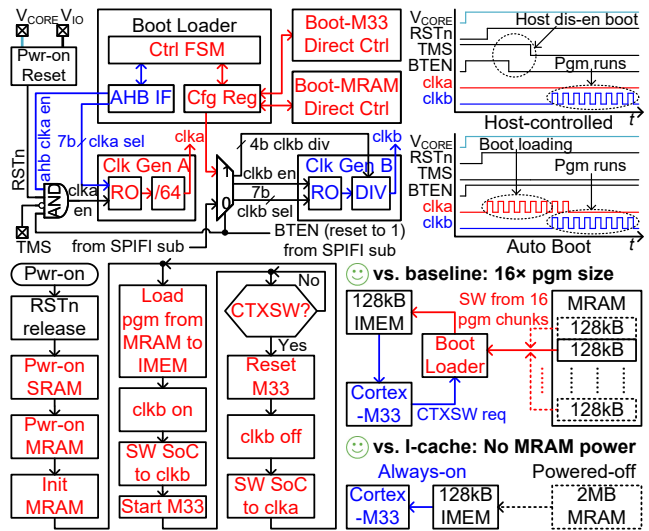


Fig. 4. Circuit for autonomous boot loading (top); operation flow for boot loading and CTXSW (bottom-left); advantages of CTXSW (bottom-right).

and ensuring a robust boot loader agnostic to clock sources. Once booting completes, M33 can turn *clka* off, removing its power overhead. The M33’s IMEM interface is incompatible with MRAM for direct use as IMEM. In a baseline design, only a single program is loaded from MRAM at boot-up, limiting program size capacity to 128kB. While instruction caching is possible, it requires MRAM to be always-on, incurring significant energy overhead. To address these, we propose a novel CTXSW scheme (Fig. 4, bottom-right) that reuses the boot loading flow, allowing M33 to switch among multiple 128kB program chunks. Compared to the baseline, this extends the usable code space to the full 2MB MRAM, achieving a 16× boost in M33 program size capacity. Compared to I-caching, it eliminates MRAM energy overhead via PG, while maintaining the same program size capacity.

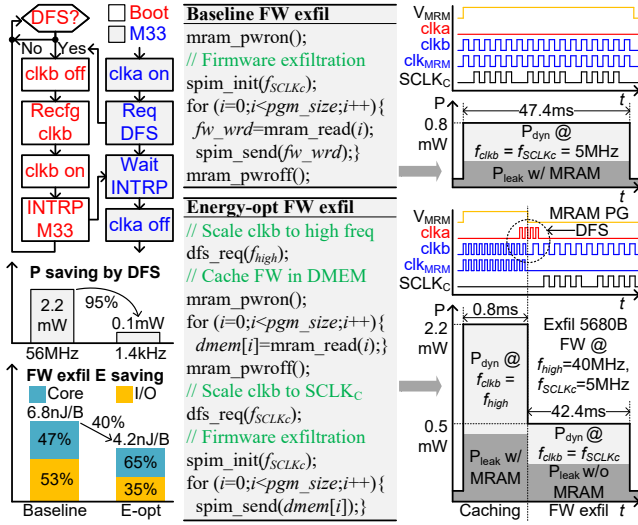


Fig. 5. DFS operation flow (left-top); baseline and energy-optimized firmware exfiltration schemes (right); measured power and energy reduction through DFS and MRAM PG (left-bottom).

### C. Data Exfiltration Energy Optimization

TexCAC supports DFS (Fig. 5 left-top) via the boot loader. As Fig. 5 (left-bottom) shows, lowering  $clk_b$  to minimal frequency for non-critical tasks reduces active power by 95% compared to running at maximum frequency. A major TexCAC workload is data exfiltration to downstream chiplets, where latency is constrained by the target  $SCLK_C$  frequency. In a firmware exfiltration scenario, a baseline scheme (Fig. 5, right-top) sets  $clk_b = SCLK_C$  to minimize active power but leaves MRAM on, causing unwanted leakage energy during SPIFI TX. To optimize exfiltration energy, we propose a novel approach (Fig. 5, right-bottom): First, firmware from MRAM is cached in DMEM at high frequency to minimize MRAM leakage overhead; then, MRAM is power gated to completely eliminate its leakage, and  $clk_b$  is scaled down to  $SCLK_C$  for the SPIFI TX phase. This combination of DFS and MRAM PG reduces exfiltration energy by 40% (Fig. 5, left-bottom).

## IV. TEXTILE INTEGRATION AND TESTING

TexCAC was fabricated in 22nm, and a TexCAC-only AST was built for validation, following the flow in Fig. 6 (left-top): First, insulated braided composite yarns are embroidered onto a textile substrate to form electrical buses; then, the insulation on the conductors is selectively ablated to expose connection points, allowing DDA using solder; finally, the devices are encapsulated to ensure reliability and durability. Fig. 6 (right) shows the testing setup, while Fig. 6 (left-bottom) highlights the flip-chip DDA. TexCAC operates fully on textile—all measurement results in this paper are taken from this textile-based testing.

## V. MEASUREMENT RESULTS

Fig. 7 shows the measured voltage-frequency-efficiency scaling across three representative low-level workloads that reflect the core functionalities of TexCAC: (A) M33 continuously reads timer value; (B) M33 continuously reads from

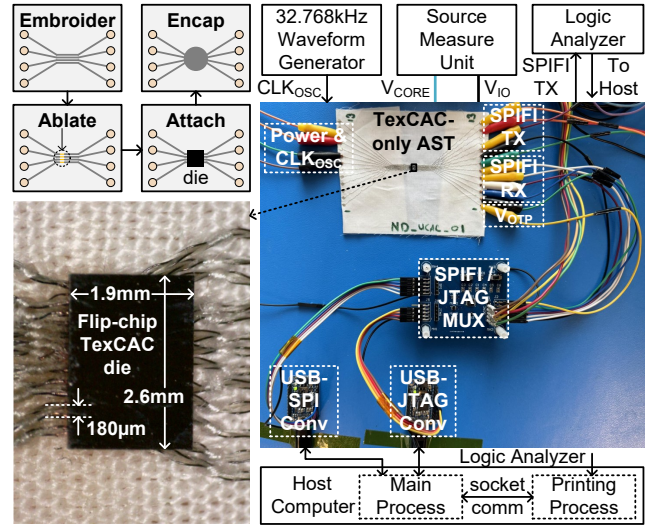


Fig. 6. Fabrication flow of AST with DDA (left-top); microphotograph of TexCAC attachment on textile (left-bottom); TexCAC testing setup (right).

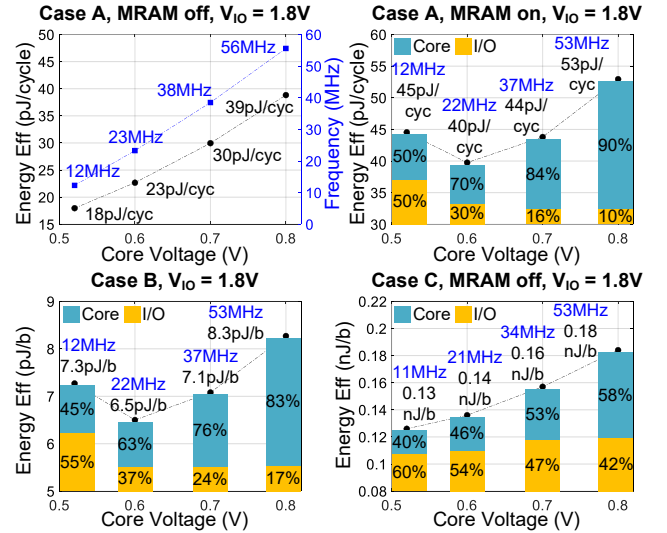


Fig. 7. Measured voltage-frequency-efficiency scaling.

MRAM; and (C) continuous SPIFI TX with  $SCLK_C$  at  $\frac{1}{4}$   $clk_b$  frequency. In Case A (Fig. 7, top), MRAM PG reduces active energy by up to 60% at 0.52V. TexCAC achieves 56MHz maximum frequency and 39pJ/cycle at 0.8V, and an optimal 18pJ/cycle active energy at 0.52V, both for Case A with MRAM off. Table I compares TexCAC with state-of-the-art NVM-based MCUs [10]–[12] and MCUs for textile applications [4], [5]. Compared to NVM-based designs, it offers a  $4\times \sim 114\times$  increase in NVM capacity under comparable or smaller area. Compared to textile-oriented MCUs, it delivers greater functional complexity and integration, including NVM-based program storage and fully autonomous boot. Across all designs, TexCAC maintains active energy on par with the best reported. Notably, it is the only NVM-based MCU that supports DDA on textile. Fig. 8 shows the die microphotograph and summary of TexCAC. The SPIFI TX operates up to 50MHz  $SCLK_C$  on textile without bit errors.

TABLE I  
COMPARISON WITH STATE-OF-THE-ART

	STM32U545	JSSC 2014 [10]	ISSCC 2019 [11]	ISSCC 2019 [12]	ISSCC 2023 [4], TBioCAS 2023 [13]	ISSCC 2025 [5]	TexCAC
<b>Technology</b>	Not reported	130nm	130nm	40nm	65nm	65nm	22nm
<b>DDA on Textile</b>	No	No	No	No	No	Yes	Yes
<sup>1</sup> <b>Autonomous Boot</b>	Yes	No	No	Not reported	Yes	No	Yes
<sup>2</sup> <b>Execution from SRAM</b>	No	Yes	No	No	Yes	Yes	Yes
<b>CPU</b>	Cortex-M33	Cortex-M0	16b MSP430	Cortex-M0	32b RISC-V	Cortex-M0	Cortex-M33
<b>Core Voltage</b>	0.9~1.2V	1.5V	0.71~1.2V	1.1~1.3V	0.4~0.9V	1.2V	0.52~0.8V
<b>I/O Voltage</b>	1.71~3.6V		3.2V	1.8/3.3V	1.0~1.2V	1.4~3.3V	1.8V
<b>SRAM</b>	274kB	8kB	8kB	No	6kB	32kB	256kB
<b>eNVM</b>	512kB eFlash	64kB FRAM	18kB RRAM	64kB MRAM	No	No	2048kB MRAM
<b>Area</b>	<sup>3</sup> 11.4mm <sup>2</sup>	4.4mm <sup>2</sup>	11.3mm <sup>2</sup>	<sup>4</sup> 22.1mm <sup>2</sup>	6.3mm <sup>2</sup>	1.3mm <sup>2</sup>	4.8mm <sup>2</sup>
<b>Max Frequency</b>	160MHz	8MHz	10MHz	200MHz	850Hz	50MHz	56MHz
<b>Dynamic V/F Scaling</b>	DVFS	No	No	No	DVFS	No	DFS
<b>Best Active Energy</b>	<sup>5</sup> 46pJ/cycle	<sup>6</sup> 113pJ/cycle	<sup>5</sup> 43pJ/cycle	<sup>5</sup> 27pJ/cycle	168pJ/cycle	41pJ/cycle	<sup>5</sup> 40pJ/cycle <sup>6</sup> 18pJ/cycle

<sup>1</sup>The ability of an MCU to boot itself fully autonomously upon power-on without depending on any external inputs.

<sup>2</sup>Allows powering-off NVM during program execution to reduce energy. <sup>3</sup>WLCSF area. <sup>4</sup>Half the area is eFPGA. <sup>5</sup>NVM on. <sup>6</sup>NVM off.

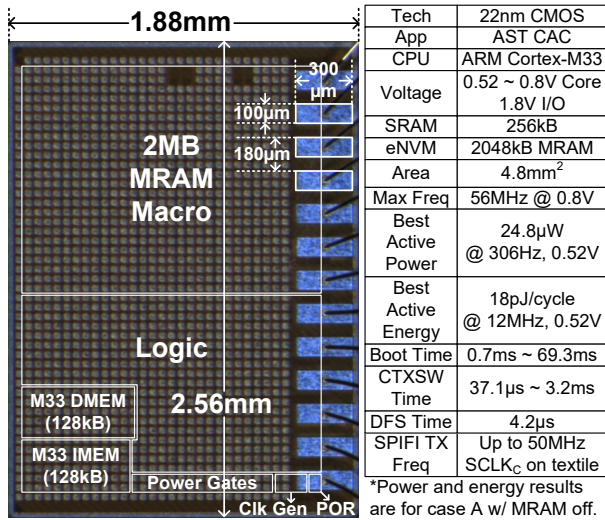


Fig. 8. Die microphotograph and summary of TexCAC.

## VI. CONCLUSION

We have presented TexCAC, the first direct-textile-attachable, NVM-based MCU designed specifically for AST CAC. TexCAC achieves significant improvements in footprint, flexibility, and energy efficiency through three key optimizations: I/O streamlining, program context switching, and energy-aware data exfiltration. Fabricated in 22nm and fully validated on textile, TexCAC delivers up to 114× greater NVM capacity than prior arts, using comparable or smaller area, while maintaining state-of-the-art energy efficiency. TexCAC sets a new benchmark for energy-efficient, fabric-integrated system control in emerging textile electronics.

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