A Reconfigurable 256×128 SPAD Imager with Gradient Gating for Single-Photon Counting, LiDAR, and Non-Line-of-Sight Imaging

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***Abstract*—A reconfigurable 256 x 128 SPAD sensor is proposed for single-photon counting (SPC), LiDAR, and non-line-of-sight (NLOS) imaging. It features gradient time-gate with 16 phases with 0.12ns to 3.8ns intervals and minimum gate window of 400ps. In SPC mode, the sensor reaches a frame rate of 42.24kfps with 9-bit intensity depth. In time-resolved mode, it reaches 39ps (LSB) time stamping. The sensor suitability is demonstrated through SPC, LiDAR, and NLOS experiments.**

I. Introduction

Single-photon avalanche diode (SPAD) detectors and SPAD image sensors are extensively are used in single-photon counting (SPC), light detection and ranging (LiDAR), and non line-of-sight (NLOS) imaging. In SPC, SPADs are used to detect photons under low illumination, while maintaining high detection speeds and/or low dead time. In LiDAR and NLOS imaging, in addition to high-resolution time stamping through direct time-of-flight, SPADs provide fast time gating, configurable with high granularity. In this work, we propose a reconfigurable 256 x 128 SPAD sensor fabricated in 55nm BCD process and equipped with single-gating and gradient-gating mechanisms, which can be configured to implement SPC or time-resolved imaging.

II. Sensor Architecture

In single-gating mode, a fast electronic shutter with fixed time length is applied to every pixel in the sensor synchronously, while in gradient-gating mode, a fast electronic shutter with different lengths is applied to clusters of pixels. Gradient gating is developed for NLOS imaging, where a light beam is pointed at a relay surface, generally a wall or floor, where it bounces for the first time. The beam hits the hidden object, which scatters the incoming light. A fraction of that light returns to the sensor through a third bounce on the same relay surface, as shown in Fig. 1. Gradient gating allows the sensor to capture a sufficient count of indirect photons from the hidden object under an overwhelming influx of early-arrival photons while maintaining the detection of the relay surface profile for successful NLOS imaging reconstruction. A time-to-digital converter (TDC) computes the time of flight at picosecond resolution for each reflected photon to enable accurate reconstruction. A large pixel array allows one to simultaneously collect light from a larger fraction of the relay surface, thus enhancing the speed of data acquisition [1]. A block diagram of the image sensor is shown in Fig. 2. The

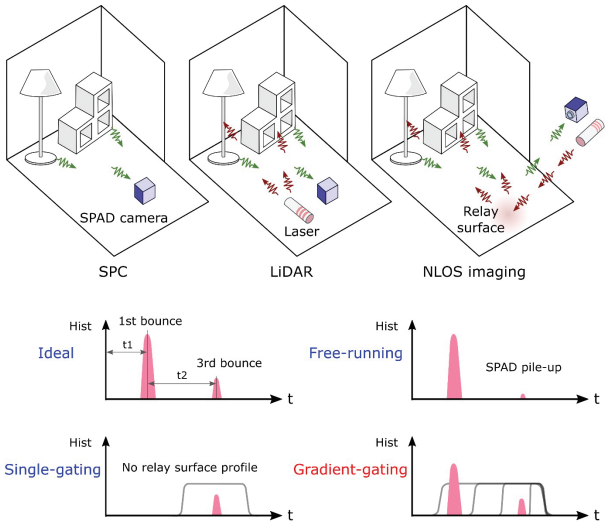

Figure 1. Applications of the reconfigurable SPAD imager.

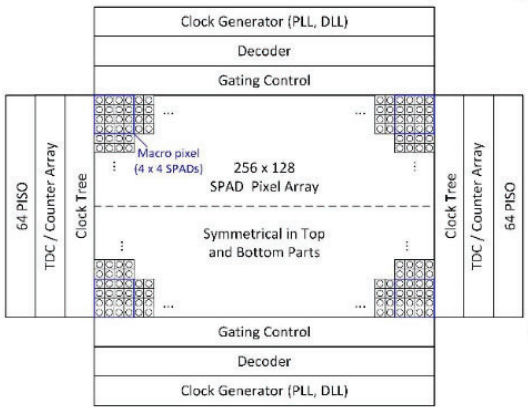

Figure 2. Block diagram of the SPAD imager.

pixel array comprises 256×128 SPADs and it can operate in SPC and in time-resolved modes simultaneously, whereas the top segment operates in SPC mode and the bottom operates in time-resolved mode. The two segments can operate in time-resolved mode but with different gating control methods. An embedded PLL produces high-frequency clock at 800 MHz, which is distributed to the TDCs via a balanced clock tree. For efficient delay control, three types of DLL blocks are implemented on chip. The first controls TDC delay, the others are designed for gating controls, compromising fine and coarse delay. The decoder activates the pixels in the corresponding columns while rolling the entire pixel array for exposure and readout purposes. The acquired time stamps or intensity data are streamed out via parallel-in-serial-out (PISO) interfaces, with a total of 128 160-Mbps PISO IO ports. An external commercial field-programmable gate array (FPGA) board is utilized to enable sensor control and data processing. In gradient-gating mode, clusters of 4 x 4 pixels are combined as macro pixels, which are turned on at different times and off simultaneously. In Fig. 3 the schematic of the pixel with gate generation is shown. The 16 gradient phases are generated

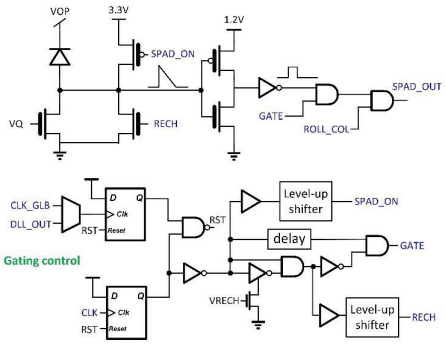

Figure 3. Pixel schematics with gating control, masking, and fast recharge.

by the DLL with a dynamic locking range determined by the phase difference between CLK_PD and CLK_VCDL. The three control signals for pixels are generated in a gating control block based on phase detection, which can configure the pixel to single-gating mode (select CLK_GLB) or gradient-gating mode (select DLL_OUT). The TDC can be configured for an LSB of 39 ps to 156 ps by adjusting the PLL clock from 200 MHz to 800 MHz. This matches the requirements for both LiDAR and NLOS imaging. VBIAS from a replica DLL is distributed to the entire TDC array. All control signals are generated by the FPGA with a minimum phase shift step of 28 ps. The TDC schematic is shown in Fig. 4. Fig. 5 shows the readout architecture and overall timing diagram. The readout architecture is based on rolling control and OR-tree. The rolling control function featured in the proposed architecture exhibits symmetrical behavior in the top and bottom sections, whereas the readout logic is symmetrically arranged in the left and right portions. During each rolling stage, four columns in each quadrant are simultaneously exposed and subsequently streamed out to either the TDC or the intensity counter.

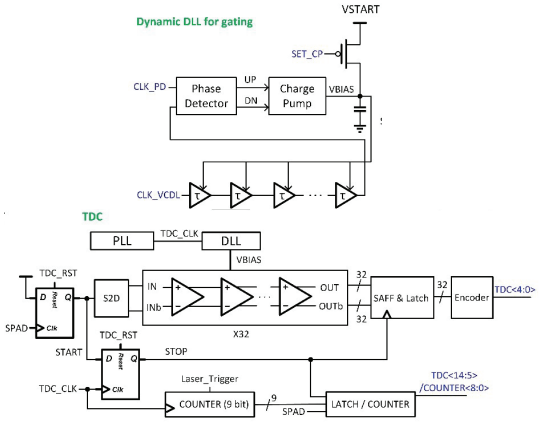

Figure 4. TDC architecture with PLL for control and the DLL replica for the fine codes.

Accordingly, there are 256 TDCs or Counters arranged for

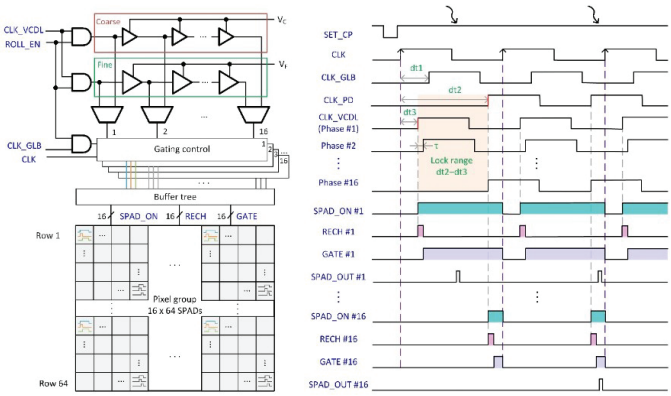

Figure 5. Timing diagram of the SPAD array readout.

each quadrant for a total of 1024 TDCs/counters. Each PISO line is used to stream out data for 8 pixels at each rolling stage. To complete the exposure and readout process for the entire array of pixels, a total of 32 rolling times are required. In SPC mode, the measured frame rate is up to 21.338 kfps with 9-bit intensity depth, with a maximum theoretical of 42.24 kfps. The rolling pattern can be configured through the decoder (5 bits to 32 bits) utilizing a flexible sequence, while a unit control module is comprised of 16 x 64 pixels. There are 64 x 32 macro pixels across the entire pixel array when running in gradient-gating mode. In order to ensure high adjustable range for the gradient step when operating in the gradient-gating mode, a coarse delay line and a fine delay line are utilized to generate gating signals. Additionally, two DLLs with the replica coarse and fine delay lines are implemented outside the pixel array and the voltage control signals VC and VF are connected to the delay line array. Within each control module, 16 gate generator blocks are employed to generate the SPAD_ON, RECH and GATE signals, which are distributed across the 16 x 64 pixel array by a buffer tree. To save power, a ROLL_EN signal is employed to turn on the only 16 x 64 SPADs in each quarter based on the rolling logic. As shown

in the timing diagram, the late arrival photons can be detected by all SPADs, while the early arrival photons can only be detected by the SPAD with large time-gate windows.

III. Results

The results of the gating profiles are shown in Figs. 6, 7. In the measurement, a uniform 780 nm pulse laser with repetition frequency of 10MHz is shined over the pixel array. The laser pulse is shifted over the full 100 ns range with a step of 28 ps. In single-gating mode, the time-gate window can be configured with a rise time of less than 200 ps. The minimum measured time-gate window is 400 ps at full-width-at-half-maximum (FWHM). In gradient-gating mode, the interval times can be configured from 120 ps to 3.8ns thanks to the implemented fine and coarse delay lines. The gradient-gate windows can be enlarged and squeezed according to different application requirements. An indoor ranging characterization with the camera was performed. In Fig. 8 the setup and the ranging results are shown with precision and accuracy. To characterize the timing histogram under different gating modes for NLOS imaging, a square hidden object is place around the corner and a collimated pulse laser (780nm, 10MHz, avg. 20mW and 50 ps pulse width) is illuminated on the relay wall. The hidden object tracking results are shown in Fig. 9. In free-running mode, a large number of photons is received from the 1st bounce (relay surface), while almost no photons are detected from the 3rd bounce (hidden object) due to pile-up. In single gating mode, a relatively large photon count can be detected from the 3rd bounce, while there are no photons received from the 1st bounce. In gradient-gating mode, significant photon counts are received from the 3rd bounce, meanwhile the range information of the relay surface is also acquired. The LiDAR experiment is implemented with a scene ranging from 1.7m to 2.6m. Its results are shown together with a NLOS reconstruction in Fig. 10. Fast SPC is demonstrated using a rotating fan under standard indoor illumination condition. The results are shown in Fig. 11.

Table I summarizes the specifications of the proposed sensor in comparison with the state-of-the-art.

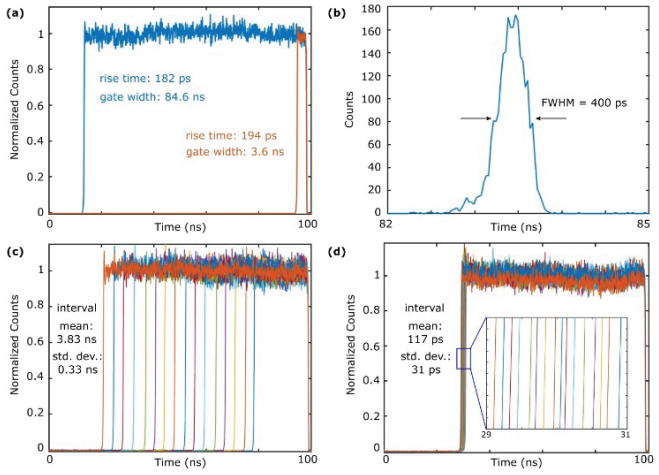

Figure 6. Gating characterization.

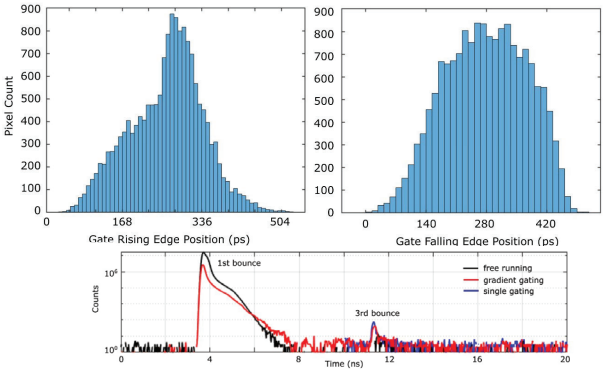

Figure 7. Rising and falling gate edges characterization over the pixel array.

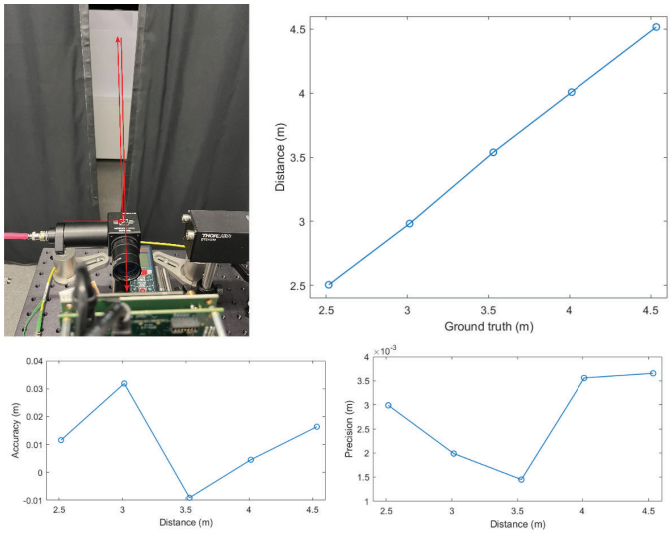

Figure 8. Single point ranging performed indoor with the Chameleon system.

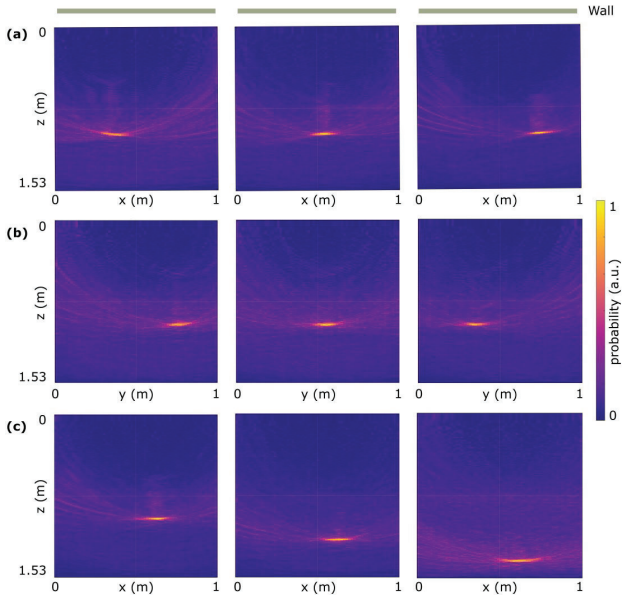

Figure 9. Tracking of an object in the hidden scene in the NLOS setup.

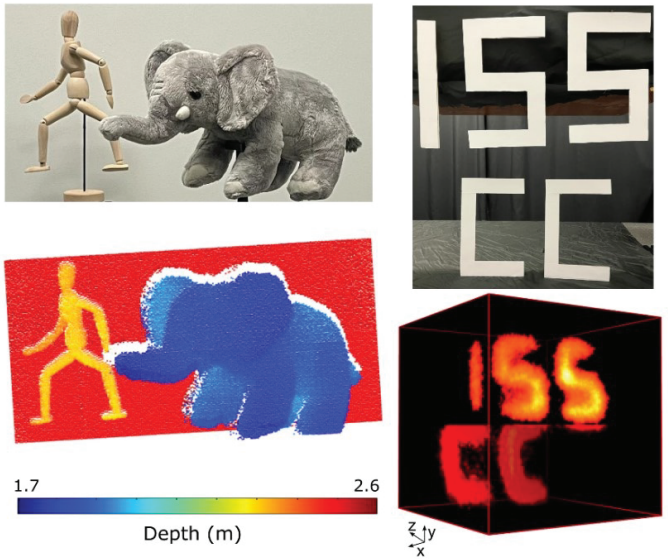

Figure 10. Characterization results for fast LiDAR imaging, including the distance bar. NLOS reconstruction with the gated sensor is also shown.

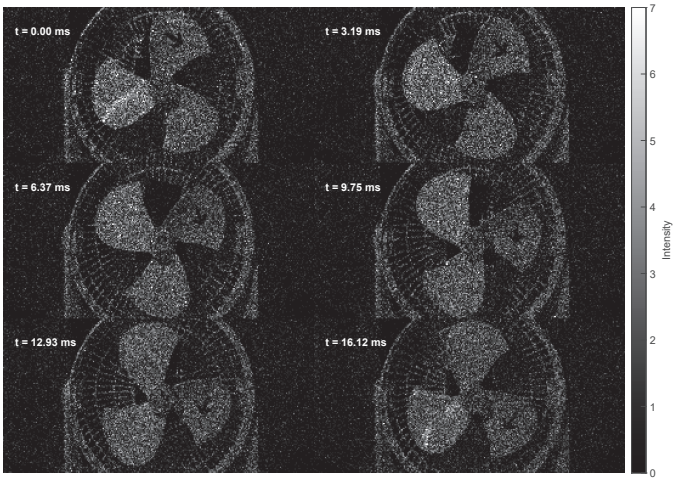

Figure 11. Raw photon-counts of a rotating fan captured at 10,669 fps with 9-bit depth. The data has not been post-processed.

Fig. 12 shows a photomicrograph of the chip, which measures 7.6 x 5.1 mm^2.

IV. Conclusions

A SPAD sensor is proposed incorporating programmable time gates and TDCs for non-line-of-sight applications. A variable gate length controls the path of light as it bounces from the source to the target and back through two bounces on a wall. The suitability of the approach is shown through real-life 3D reconstruction as compared to the ground truth.

Table I
State-of-the-art in time-resolved and NLOS sensors.

Parameter	**This work**	[2]	[3]	[4]	[5]
Tech.[nm]	**55**	350	40/90	160	45
Pixels	**256×128**	160×120	256×256† 64 ×64*	16x16	256×128
FF[%]	**20**	21	51	9.6	N/A
PDP[%]	**51**	N/A	23	55	N/A
Jitter[ps]	**52**	N/A	136	30	N/A
Frame rate[fps]	**21,338**	486	760	N/A	N/A
Bit depth[bit]	**9**	8	14/28	N/A	N/A
TDC Depth[bit]	**14**	N/A	14/4	10	14
LSB[ps]	**39-156**	N/A	35/560	6	60
DNL/INL p-p[LSB]	**1.2/2.77**	N/A	0.1/0.18	0.042/3.59	0.1/2.2
N° TDCs	**1024**	N/A	4096	16	N/A
Gate type	**Single & Gradient**	Single	Single	Single	Single
Min. time-gate[ps]	**400**	750	N/A	N/A	N/A
Gate rise-time[ps]	**200**	200	N/A	400	N/A
Time interval[ns]	**0.12-3.8**	N/A	N/A	N/A	N/A
Power[mW]	**121**	156.7	77.6	500	52

† Intensity mode. *time-of-flight mode.

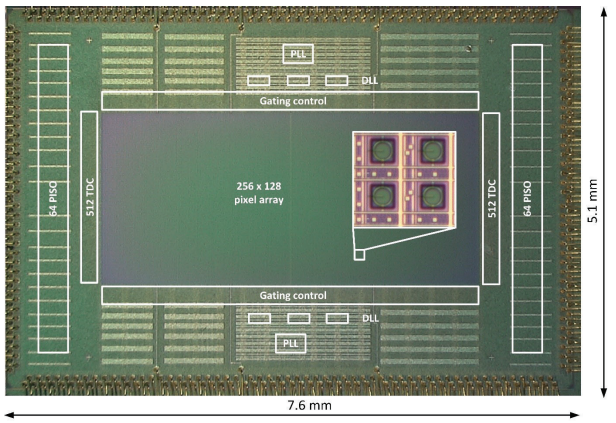

Figure 12. IC photomicrograph.

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