A Deep sub-micron 14nm Fin-FET Digital Power Amplifier Based on Quad-Stacking Switch Capacitor Topology

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***Abstract*— This work presents a novel switch-capacitor digital power amplifier (SC-DPA) topology with a quad-stacking transistor and capacitive feedback driver, enabling reliable operation at up to four times the maximum voltage allowed by the process node. A 3.3V Watt-level DPA, implemented in the 5-7 GHz Wi-Fi band using 14-nm FinFET CMOS technology, achieves 28.8 dBm of output power and 20.7% power efficiency at 5.7 GHz. Reliability testing shows minimal power degradation over extended operation. Measurements confirming the design, integrated into a polar digital transmitter (PDTX), support 320M/4096-QAM (MCS13) modulation for Wi-Fi 7.**

***Keywords*—WiFi-7, Digital Power Amplifier, DTX.**

I. Introduction

The power amplifier (PA) is an essential part of modern communication systems for boosting signal power, enabling long-distance transmission. The efficiency, linearity, and reliability of PAs directly affect signal integrity, system performance, and energy consumption, making their optimization crucial for reliable communication.

Recently, digital transmitters (DTXs) based on Switched Capacitors Digital Power Amplifiers (SC-DPAs) have gained popularity due to their advantages in nanoscale CMOS technology, offering reduced die area and high efficiency [1]. However, lower supply voltages in advanced CMOS nodes complicate achieving higher output power.

One way to address this limitation is by using multicore DPAs, with configurations up to 8 cores [1-6,11]. However, adding more cores can reduce power efficiency (PE) due to lower load resistance and increased parasitic losses. Alternatively, device stacking allows increasing the supply voltage above the maximum voltage rating (V_{DM}) across transistor terminals [2-5], enabling higher load resistance without necessarily degrading PE. Two and triple stack topologies have been previously proposed and allow to work with supply voltages ~2-3×V_{DM} [2-5, 9-10]. However, using further advanced digital oriented CMOS process with lower V_{DM}, results in limiting the supply voltage and the output power.

To this end, this work presents a novel SC-DPA topology based on a quad device stacking with multiple capacitive feedback and bias keepers that maintain the stress between the transistor terminals at ~1/4×V_{DD}, allowing for lower V_{DM} and improves the reliability of the DPA over the expected lifetime. Based on this technique, a Watt level SC-DPA, working at the 5-7GHz WiFi band and supporting 320MHz BW and MCS13 (4096-QAM) at 9dB back off (dBBO) is demonstrated in 14nm Fin-FET digital process technology, with the quad device stacking working directly from a 3.3V supply. Accelerated aging tests of a triple and quad stacking DPAs are performed and presented.

II. Design Considerations

A. The Quad Stacking 3.3V Digital PA Topology

The triple-stacked topology (3×PMOS + 3×NMOS) for an SC-DPA driver, based on the capacitive feedback concept, was proposed by Shay et. al in [9-10]. Figure 1a illustrates the required signal at the gates of MP_3 and MN_3, such that the stress between the transistor terminals maintained at ~1/3 of the driver supply voltage. Nevertheless, in process nodes where V_{DM} is less than 1/3 of the required V_{DD} this still can set limit on V_{DD} value and P_{MAX}.

To this end, figure 1b shows an extension of the stacking concept to a quad-transistor stack (4×PMOS + 4×NMOS) topology for an SC-DPA driver. For simplicity, a single-ended driver is depicted, though the full design includes a complementary differential driver cell (labeled 'n' and 'p'). The gates of transistors N_1 and P_1 are driven by a V_{DM} amplitude (0-V_{DM} and 3×V_{DM}-4×V_{DM}, respectively), while the gates of N2 and P2 are fixed at V_{DM} and 3×V_{DM}, respectively. Since the expected output voltage swings range from 0-4×V_{DM}, the gate voltages of N_4&P_4 cannot remain fixed, as this would exceed the allowable voltage range between transistor terminals. Hence, the gates of N_4 and P_4 should be driven by a signal 1×V_{DM}-3×V_{DM}, in phase with the output signal (i.e. out of phase with N_1&P_1 gate signals) ensuring the stress on N_4 and P_4 stays below V_{DM} (~1/4×V_{DD}).

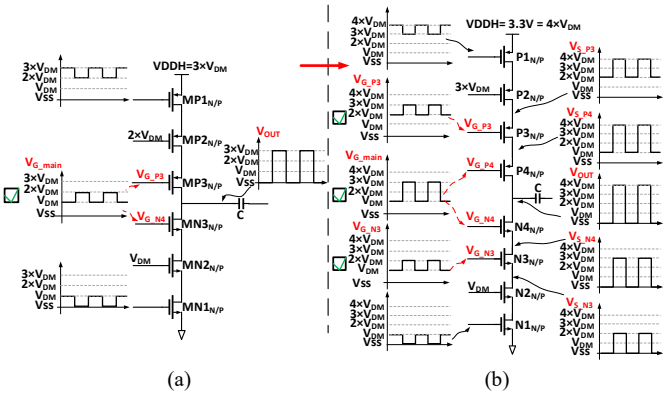


Figure 1. Output stage triple to quad stack topology (for sake of simplicity shown as single-ended N/P, i.e. N or P side), (a) triple stack suggested in [9-10], and (b) the extension challenge to quad stack topology.

Furthermore, in the quad-stacking N_3&P_3 gates also cannot stay at fixed voltage to avoid over-stress. Following the expected voltages at the drain/source of the transistors in the stack, N_3 gate should be driven with a V_{DM} signal between $1\times V_{DM}$ and $2\times V_{DM}$, and P_3 gate with a signal between $2\times V_{DM}$ and $3\times V_{DM}$, as shown in the figure.

Following the approach taken by Shay et. al in [9-10] in a triple stacking DPA using capacitive feedback to avoid the need for additional active drivers, we propose the following modification. First, a capacitive divider feedback, using transistors P_FB1 & N_FB1 (shown in figure 2b), is used to generate the required N_3 & P_3 gate signal. The ratio of the feedback voltage $V_{FB,2}$ and the output swing V_{OUT}, Assuming $C_{GD}\approx C_{GS}$, the gate-drain and gate-source capacitances of the transistors, respectively, and the gate width of the stacked devices is identical (i.e. W_Pi=W_Ni=Wi), can be approximated by

$$\frac{V_{FB}}{V_{OUT}} \approx \frac{5}{8} \times \frac{W_3}{W_{FB}+W_3} \quad (1)$$

Next, transistors P_FB2 & N_FB2 (shown in figure 1b) generate the required gate signal for N_4 & P_4. The capacitive divider feedback can be approximated by

$$\frac{V_{FB,main}}{V_{OUT}} \approx \frac{14}{16} \times \frac{W_4}{W_{FB2}+W_4} \quad (2)$$

The sizing of the capacitive feedback transistors for N_3 & P_3 or N_4 & P_4 is selected to establish a capacitive divider voltage ratio, as required by the drain-to-gate voltage swing ratio for these transistors, as discussed above.

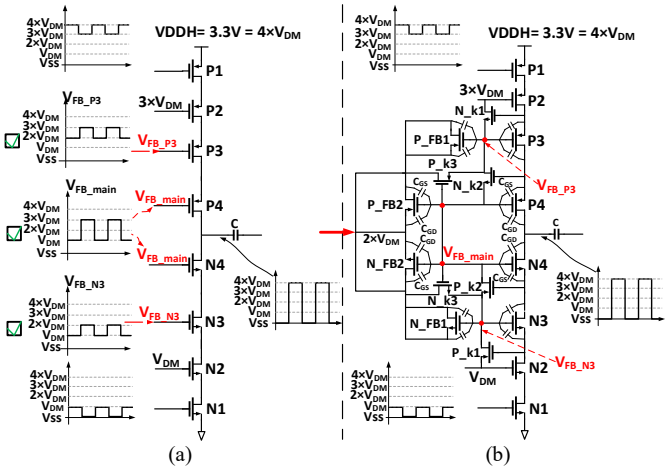


Figure 2. Output stage stack topology (for sake of simplicity shown as single ended, i.e. N or P side), (a) the options of biasing/driving P3/4 and N3/4, and (b) the proposed implementation of feedback-generated biasing.

Finally, the capacitive feedback shown in Figure 2b can face two potential issues: the floating DC level of the generated signal and device sizing inaccuracies due to layout and process mismatches. To stabilize the feedback, remove the DC voltage ambiguity, and minimize layout and device dependency, transistor bias keepers $N\_k_{1,2,3}$ & $P\_k_{1,2,3}$ are added. When the output goes high, $N\_k_{1,2,3}$ activates, pulling the feedback nodes V_FB_P3, V_FB_main, and V_FB_N3 to $3\times V_{DM}$, $3\times V_{DM}$, and $2\times V_{DM}$, respectively, thus supporting the capacitive feedback. When the output goes low, $P\_k_{1,2,3}$ activates, pulling V_FB_N3, V_FB_main, and V_FB_P3 to $1\times V_{DM}$, $1\times V_{DM}$ and $2\times V_{DM}$, respectively, further supporting the feedback.

B. Incorporating the SC-DPA into a Digital Polar Transmitter

Figure 3 presents the block diagram of a Digital transmitter employing the proposed SC-DPA topology. The positioning of the Local Oscillator (LO) signal can be adjusted either by modifying the instantaneous frequency or via a Digital-to-Time Converter (DTC), which generates the Modulated LO (MOLO) signal [1]. This MOLO signal drives the SC-DPA cells, which overlay the amplitude information provided by the modem's Digital Signal Processor (DSP) generated modulated signal commands.

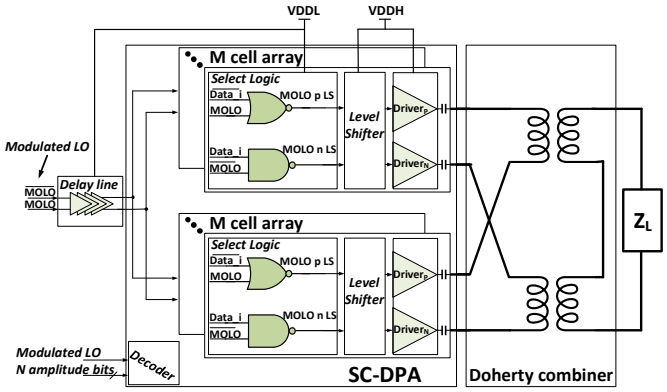


Figure 3. The proposed SC digital PAs block diagram shows the SC-DPA supplies voltages connections, where VDDH=3.3V, VDDL=1V.

The cells are organized into two arrays, and their outputs are combined by a transformer-combiner, which adjusts the load impedance between 1:1 and 1:2 in a digital Doherty-like manner [1-3]. Within the SC-DPA, the MOLO distribution and control logic operate in a low supply voltage domain (VDDL = V_{DM}), transitioning to a higher supply voltage domain (VDDH = $4\times V_{DM}$) to drive the output stages effectively. The amplitude control bits are synchronized with the MOLO signal to ensure proper phase and amplitude alignment, preserving signal fidelity.

A data control signal is used to activate or deactivate each cell in the array. When a cell is activated, the logic cells drive the low voltage ($0\div V_{DM}$) MOLO signal to the gates of a fast level shifter [9-10] and the DPA driver $N1_N$/$N1_P$ transistors.

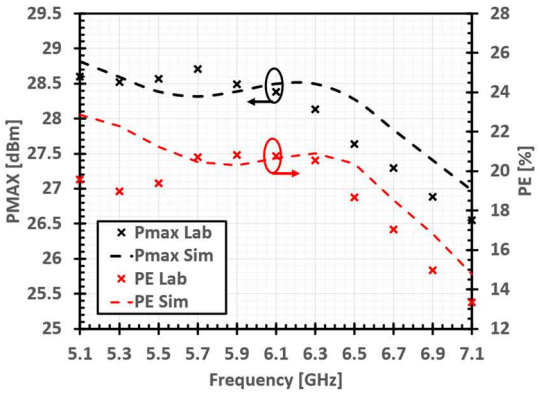
III. Measurement Results

The proposed SC-DPA is fabricated in a 14nm Fin-FET technology and occupies ~0.43mm^2. All transistors used in the design are 14nm Fin-FET (a.k.a. thin gate core device) transistors and supply voltages are VDDL=1V and VDDH=3.3V. Each array is constructed from a 7-bit thermometric cell-array and additional 5-bit binary weighted cells.

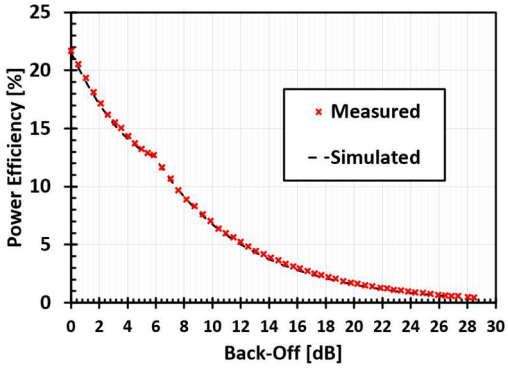
A. Continuous Wave Characterization

Figure 4a exhibits simulated and measured performance results of the proposed 3.3V quad-stacked SC-DPA. Peak

power at maximum code (P_{MAX}) and respective power efficiency (PE) of 28.8dBm/21.2% is measured at 5.7GHz, while the minimum P_{MAX} and PE measured across the WiFi band are 26.6dBm and 13.8%, respectively, at 7.1GHz. The measured results show a good correlation to simulated results with a 0.2GHz shift in frequency and some excess insertion loss of <0.4dB at the higher frequencies, which evolve from some inaccuracy in modelling the test board loading and the CMOS process variations. The measured PE vs. power back-off from Pmax at a representative frequency is also measured (figure 4b) and shows a good correlation to simulated results. The PE enhancement at 6dBBO due to the switched transformer combining, Doherty-like operation [1-3] is observed.



(a)



(b)

Figure 4. Measured vs. simulated CW results: (a) P_{MAX} and PE over frequency, (b) PE vs Back-Off at 6.1GHz.

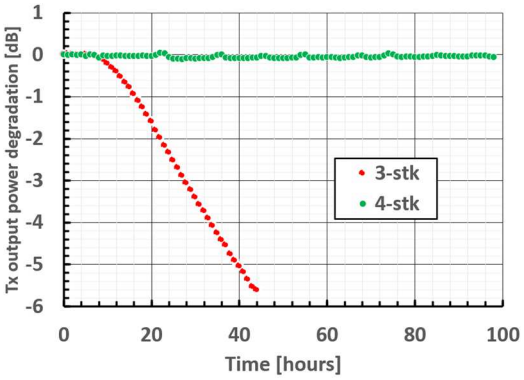
B. Reliability Characterization

To confirm the superiority of the quad-stack topology in the current 14nm process, two SC-DPAs, triple-stack and quad-stack were designed, fabricated and tested. Figure 5a compares their output power degradation over time under nominal 3.3V supply voltage at room temperature. It is clearly shown that while the triple-stack power rapidly drops, the quad-stack maintains stable performance.

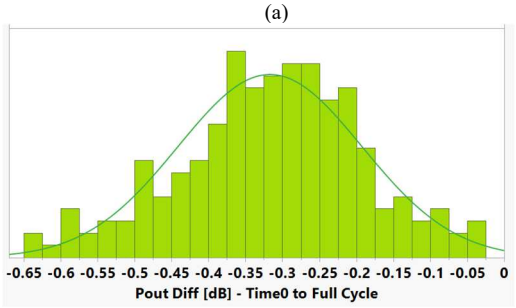
To further confirm the robustness of the quad-stack, an accelerated aging design of experiment (DOE), based on [11], was conducted, alternating between MAX and MIN codes to trigger a variety of damage mechanisms (e.g., BTI, hot carriers, oxide breakdown). Figure 5b shows a minor output power degradation of up to 0.7 dB over the device's expected lifetime.

C. Modulated Signal Characterization

The response of the polar DTX with the proposed 3.3V SC-DPA to a modulated Wi-Fi OFDM signal, focusing on the 160MHz & 320MHz bandwidths, is measured and shown in Fig. 6. A digital memory pre-distortion based on Volterra series model is used for the measurements [7]. An EVM of -35dB, required for Wi-Fi MCS10/11 (1024QAM), is achieved at 7.6dBBO/8.2dBBO and an EVM of -38dB, required for WiFi MCS12/13 (4096QAM), is achieved at 8.2dBBO/9dBBO for 160MHz/320MHz, respectively (figure 6a). The 160MHz signal shows only ~0.5dB degradation vs. an ideal linear and memoryless transmitter.



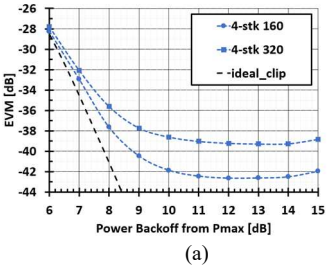
(a)



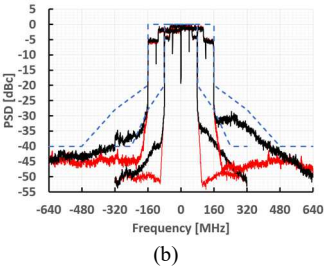
(b)

Figure 5. Reliability Testing results: (a) comparing triple stack design and quad-stack design in 14nm process and (b) The full lifetime stressed unit output power degradation histogram of the suggested quad stacking topology.

For a 320MHz OFDM signal at 6.1GHz and 9dBBO (~19.5dBm) the measured current consumption was 268mA/190mA from the 3.3V/1V supplies, respectively. While for 160MHz OFDM signal at 5.2GHz and 8dBBO (~20.5dBm), a 287mA/172mA from 3.3V/1V supplies, respectively, was measured.



(a)



(b)

Figure 6. Measured modulated signal results: (a) EVM vs Back-off and (b) Spectral Response at 8dBBO for 160MHz and 320MHz OFDM signals, without (black) and with (red) pre-distortion, vs. WiFi mask (blue).

The spectral response of the WiFi MCS13 OFDM signal, at 8dBBO for the 160MHz and 320MHz signals, was measured and is shown in figure 6b, with (red line) and without (black line) operating the pre-distortion algorithm, showing healthy margins from the WiFi mask (blue line). The testchip die photograph, highlighting the 3.3V quad stacked SC-DPA with area of <0.44mm^2, is presented in Fig. 7.

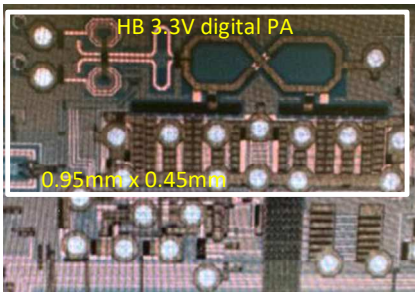


Figure 7. Die micrograph.

IV. Conclusion

An SC-DPA featuring a novel 3.3V quad-stacked transistor with multiple capacitive feedback, offering enhanced reliability, is demonstrated in the 5-7 GHz band. Table 1 compares the performance of the DPA integrated into a PDTX with respect to prior art. The new design is the first PA implemented in 14-nm FinFET using 3.3V supply, demonstrating state of the art performance.

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Table 1. Performance comparison table.

	This work		RFIC 2024 [9]		ISSCC 2022 [1]		ISSCC 2020 [8]	JSSC 2023 [6]	JSSC 2019 [5]
Technology	**14nm**		16nm		16nm		55nm	40nm	65nm
Modulation signal	**Wi-Fi 7 (802.11be)**		Wi-Fi 7 (802.11be)		Wi-Fi 6E (802.11ax)		Wi-Fi 11abgn/ac/ax	1024-QAM OFDM 5MHz	16QAM 5MHz
TX technology	**2-cores Polar DTX 4-stack SC-DPA**		2-cores Polar DTX 3-stack SC-DPA		4-core Polar DTX 1-stack SC-DPA		Analog I/Q PA	Digital I/Q PA	Multi-SHS/Class G + three-way combiner
Integration (TRSW & RX)	**Yes**		Yes		Yes		Yes	No	No
Supply [V]	**1/3.3**		1.1/3.3		1.2		3.3	0.95	1.2/2.4/3.3
Freq. [GHz]	**5-6**	**6-7.1**	5-6	6-7.1	5-6	6-7	5-6	2.4-2.5	1.65-2.2
P_{MAX} (dBm)	**28.8**	**28.4**	30.15	29	27.8	26.6	29	23.18	30
Peak PE [%]	**20.7**	**21.2**	36	31	26	25	N.A.	52.5	46.5
OFDM BW (MHz)	**160**	**320**	160	320	160	160	160	200	5
Pout (dBBO) @ EVM=-35/-38 [dB]	**7.5/8.4**	**7.9/9.1**	7.6/8.2	8.2/9	9.8/N.A.	12.6/N.A.	9/11	13.2/18.2	N.A/N.A
PA P_{DC} (mW) @ Pout=20dBm	**1050**	**1120**	710	830	691	813	858 [c]	NA	400 [d]

[a] Extracted from EVM/PAE graph. [b] no TX/RX SW or Rx loading. [c] Improved efficiency due to high supply . [d] Extracted from DE graph