Design and Analysis of Voltage Regulators for Retimer Latches in RF NRZ DACs

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***Abstract*—This paper presents the design of voltage regulators, particularly for the re-timer latches in RF NRZ DACs. The prototype regulator designed in TSMC 65nm LP simultaneously achieves higher DC gain and unity gain loop bandwidth using analog techniques. Although the prototype design bootstraps the source follower's gate, the resultant spur measured at the output is -99dBm. The design achieves maximum output impedance $<$ 1Ω for the entire frequency range with 150 pF load capacitance, power supply ratio better than -19.2 dB at all frequencies, and noise spectral density of 10 µV/$\sqrt{(Hz)}$ at 1Hz while delivering 15 mA to re-timer latches at 1.2V.**

***Index Terms*—Regulator, DAC, NRZ, Self-bias.**

I. Introduction

RF NRZ DACs [1]–[3] are becoming popular, especially for software-defined radios, due to flexibility in digital and reduced analog/RF complexity. Fig.1 shows a typical block diagram of RF DAC that uses NRZ DAC. The equal arrival of all digital data to the DAC core is done using re-timer latches. Digital blocks, clock drivers, and re-timer latches typically have different regulators for noise isolation. The regulator that supplies current [4] to re-timer latches is critical among all other regulators as it modulates the data edges, creating spurs and harmonics at DAC output. The re-timer latches and buffers draw current from this regulator at every data transition, resulting in a $2f_{BW}$ component at its output where f_{BW} is the signal bandwidth. The $2f_{BW}$ component which depends on the regulator output impedance at those frequencies mixes with the input signal, resulting in undesired IM_3 components. Fig.1b) shows a regulator's typical output impedance, with a peak near the Unity Gain Bandwidth (UGB). Fig.1c) shows the IM_3 simulation of an RF current steering DAC by varying the spacing between the two tones. The two-tone spacing represents the IF bandwidth of the signal. The IM_3 reaches a minimum when the tone spacing is at the peak of the regulator's output impedance. The regulator's maximum output impedance and the frequency at which impedance reaches a maximum is represented as Z_{OUT} and f_{max} as shown in Fig.1. Therefore, the regulator's maximum output impedance frequency (f_{max}) limits the tone spacing or the IF bandwidth of an RF DAC.

Additionally, the low-frequency noise on the regulator output gets upconverted to the signal frequency, affecting the Adjacent Carrier Leakage Ratio (ACLR) of the transmitted signal. Hence, the regulator for the re-timer latches should

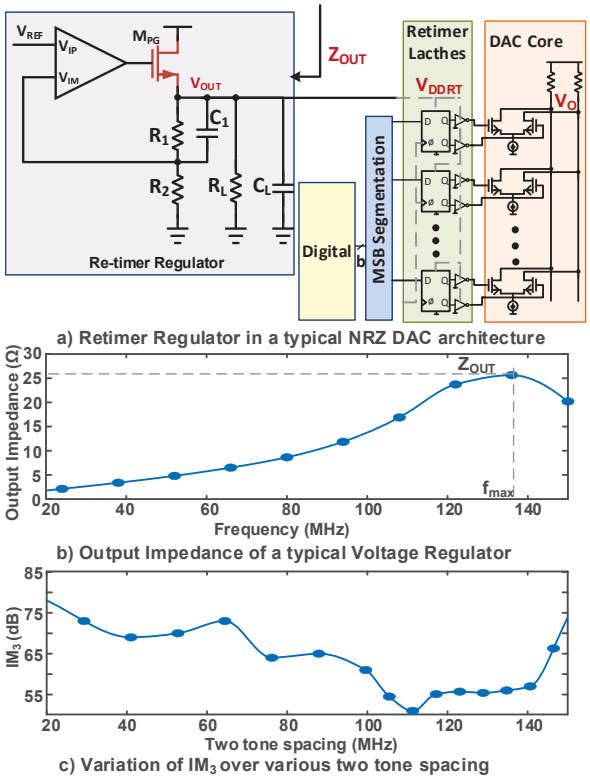

Fig. 1: Impact of Retimer Regulator Output Impedance on the IF Bandwidth of RF NRZ DACs

have extremely low, low-frequency noise and have maximum f_{max} and minimum Z_{OUT} with no spurs at the output.
Higher f_{max} and lower Z_{out} demand higher UGB and DC gain of the loop while driving a larger decoupling capacitor. Higher f_{max} and lower noise demand higher first-stage opamp current. Higher first-stage current results in a lower output impedance of the first stage. Conventional voltage regulators [5] using NMOS pass gates for lower output impedance use multiple supplies or charge pumps to avoid a threshold drop. Further, the charge pump results in undesired clock spurs at the output. The attainable UGB of the loop is limited with the filters that reduce the clock spurs. Multiple loops are used in a low bandwidth mode to control the PSR and the load transients [6]. Recently, there has been a lot of traction towards digitally assisted LDOs [7], [8], but they suffer from large

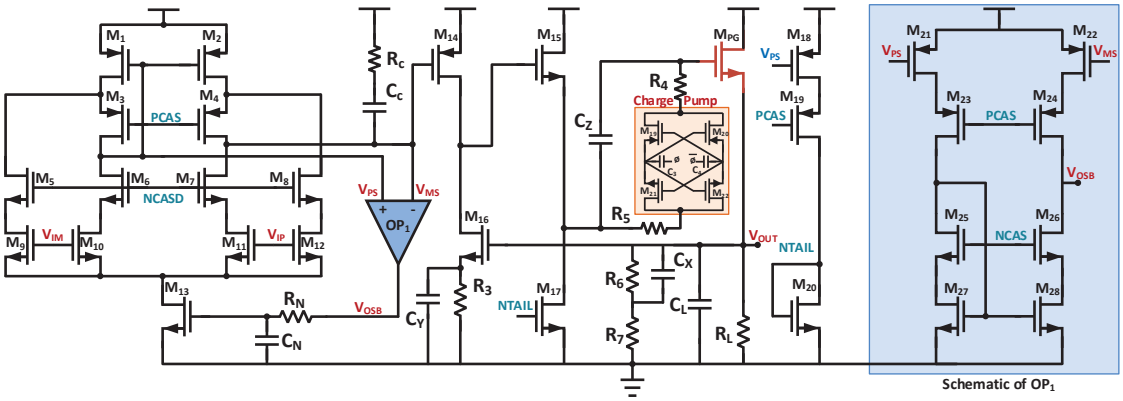

Fig. 2: Schematic of proposed low impedance regulator

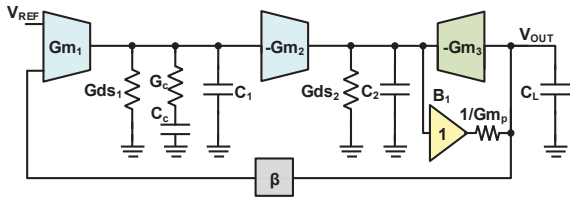

Fig. 3: Block diagram of proposed low impedance regulator

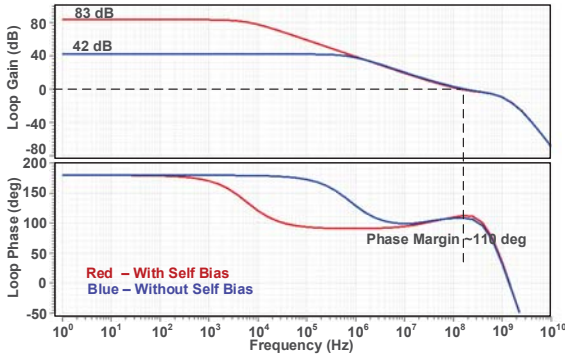

Fig. 4: Bode plot of the loop gain

ripples and spurs at the output and hence are unsuitable for re-timer latches. Self-bias is a known technique used in regulators with PMOS pass gates for reducing systematic offsets with load currents [9]. The bias current for the error amplifier is derived from the PMOS pass gate regulators to improve the accuracy by maintaining the same current densities across all PMOS load transistors. Self-bias is seldom used in regulators that have NMOS pass gate due to the following reasons. It is difficult to derive the opamp bias current from the load current due to the non-grounded source node of the pass gate.

To mitigate the above problems, we have designed a voltage regulator with the following three techniques in this work. Firstly, self-bias is used in the first stage to increase the DC gain without affecting the opamp's UGB [10]. Secondly, the gm boosting technique on an NMOS pass gate increases the UGB of the opamp without creating any high-impedance node in the loop and lowers its output impedance at higher frequencies. Thirdly, a Nakagome charge pump [11] is used at the high impedance pass transistor gate with a heavy filter only for the clock spur path.

II. Proposed Regulator for Re-timer Latches

Fig.2 shows the proposed voltage regulator architecture. The differential pair $M_{10,11}$ and cascode $M_{6,7}$ form the telescopic cascode part and the differential pair $M_{9,12}$ and cascode $M_{5,8}$ form the folded cascode part of the first stage. This hybrid architecture gives two advantages: a) the cascode transistors $M_{3,4}$ and $M_{6,7}$ carry a lower current, increasing the first stage's output impedance b) It increases the swing limits at the first stage output. For example, the first stage output voltage will decrease, pushing transistors $M_{10,11}$ to the triode region's verge while the regulator delivers large currents. However, even in this extreme case, the folded cascode part (M_{12}) of the amplifier provides non-zero first-stage gain. The transistor M_{14} forms the second stage of the regulator followed by transistor M_{15} which acts like a buffer to drive the pass gate NMOS transistor M_{PG}.The pass gate (M_{PG}) is a core transistor with its source and bulk connected. The transistor M_{16} forms a gm boosting stage to lower the regulator output impedance at higher frequencies. The output of the second stage has a Nakagome charge pump to increase the gate voltage of M_{PG} more than the power supply to avoid the threshold drop. The charge pump has an input clock of 1 GHz and uses small fly capacitors as it does not deliver any current. The resistor $R_{4,5}$ and the capacitor C_Z filter the clock spurs from the charge pump. Furthermore, C_X acts like a bypass capacitor for the high-frequency, enabling higher UGB of the loop. The re-timer latches dictate the regulator's load capacitor to be 150 pF. The loop is compensated with the zero created using R_C, C_C network at the first stage output. The loop dynamics of the regulator are studied with the help of a block diagram as shown in Fig.3. The Gds_1 and Gds_2 represent the output conductances, Gm_1, Gm_2 and Gm_3 represent the transconductances of the first, second and gm boosting stage of the regulator and G_c,C_c represents the compensation conductance and capacitance respectively. The last stage (B_1) combines the buffer (M_{15}) along with the pass gate and is represented with the unity gain stage with output impedance ($1/Gm_p$) and β is the feedback factor. The loop

gain is derived as in (1).

$$LG = \frac{-\beta Gm_1 Gm_2 Gm_p}{Y_1(Gm_3 Gm_p + Y_2(Gm_p + sC_L))} \quad (1)$$

where Y_1 and Y_2 represent the conductances at the output of the first and second stage and are given by

$$Y_1 = Gds_1 + sC_1 + \frac{sC_c G_c}{sC_c + G_c}, Y_2 = Gds_2 + sC_2 \quad (2)$$

The UGB and DC gain of the loop are given by

$$LG_{DC} = \frac{Gm_1 Gm_2}{Gds_1 Gm_3} \quad UGB = \frac{Gm_1 Gm_2}{G_c C_2} \quad (3)$$

Unity Gain Bandwidth of 200 MHz dictates that the first stage current is 1 mA and limits the DC gain to 42 dB as shown in Fig.4. The DC gain is increased with the help of self-bias [10], [12]. Self-bias is a popular technique used in circuits [12] to reduce the systematic offset. The negative feedback adjusts the first stage output voltage V_{MS} to equalize the virtual nodes V_{IP} and V_{IM}. However, in the absence of self-bias loop voltage V_{MS} need not equal the diode voltage V_{PS} as it depends on the first stage current resulting in a finite input DC error or systematic offset. In the presence of a self-bias loop the opamp (OP_1) equalizes the V_{PS} and V_{MS} nodes by adjusting the tail transistor M_{13} current thereby reducing this error. The DC error reduction can also be seen as an increase in the DC gain due to self-bias as seen in Fig. 4. One other way to increase the DC gain in literature is by cascode gm boosting. However, the unity gain bandwidth of the gm boosting loops should be at higher frequencies as it will appear as the poles on the negative feedback loop gain (1). On the other hand, self-bias should have a lower bandwidth to avoid the interaction of this main loop and is limited with R_N and C_N to avoid stability issues [12]. The opamp OP_1 is telescopic in architecture with pseudo-differential pair $M_{21,22}$, which is of the same size as $M_{1,2}$. The current in M_{14} is derived from the output voltage (V_{OUT}) and is approximately given by

$$I = \frac{(V_{OUT} - V_T)K_n R_3 + 1 \pm \sqrt{2(V_{OUT} - V_T)K_n R_3 + 1}}{K_n R_3^2} \quad (4)$$

where K_n is given as $\mu_n C_{ox} W/L$. The self-bias ensures the first stage current to be (4) as the size of PMOS transistors $M_{1,2}$ and M_{14} are identical. The startup circuit is similar to that used in [10] and is not shown here for simplicity. The output impedance Z_{OUT} of the regulator is derived by injecting current at the output and evaluating the voltage as

$$Z_{OUT} = \frac{1}{sC_L + \frac{Gm_p Gm_3}{Y_2} + Gm_p(1 + \frac{Gm_1 Gm_2 \beta}{Y_1 Y_2})} \quad (5)$$

The higher low-frequency conductance is obtained with a self-bias loop as it increases the DC gain. The higher high-frequency conductance is obtained with higher decoupling capacitance (C_L), and the conductance near UGB is increased by the gm boosting transistor Gm_3. The output impedance

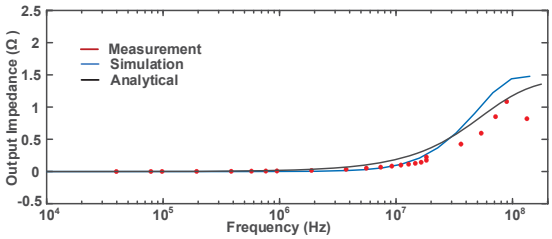

Fig. 5: Measured Output Impedance of the Proposed Regulator

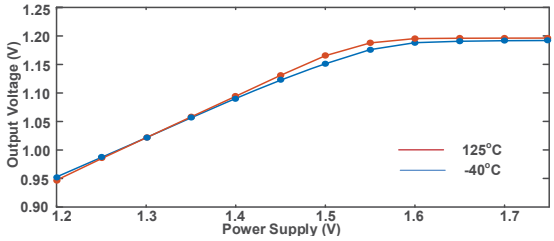

Fig. 6: Measured Line Regulation of the Proposed Regulator

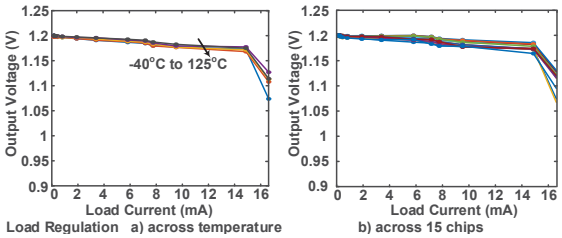

Fig. 7: Measured Load Regulation of the Proposed Regulator

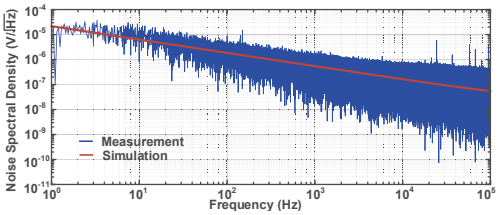

Fig. 8: Measured Noise Spectral Density of the Regulator

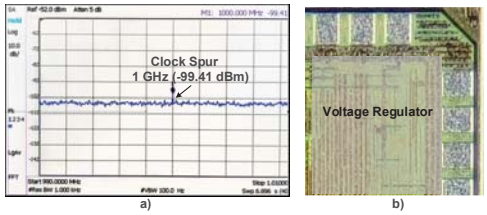

Fig. 9: a) Measured clock spur b) die photo

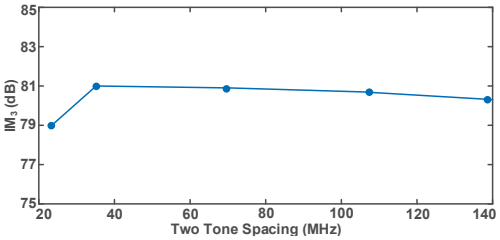

Fig. 10: IM3 simulation of RF DAC with proposed regulator

TABLE I: Specifications and Comparison with Prior Arts

	This Work	[13] JSSC'20	[14] JSSC'20
Process(nm)	65	65	40
Supply (V)	1.5	0.5-1	1.25-1.4
Output (V)	1.2	0.45-0.95	1.1-1.25
Temp.(°C)	[-40,125]	NR	NR
$Z_{OUT}(\Omega)$	<1	NR	NR
Frequency (MHz)	1000	1	500
Technique	Analog	Event	Hybrid
Clock Spur (dBm)	-99	NR	NR
Samples	15	1	1
Output Ripple (mV)	0	<15	0
Noise ($\mu V/\sqrt{Hz}$)	10@1Hz	NR	NR
Area(mm^2)	0.0237	0.04	0.0345
Load Capacitor	150 pF	400 pF	20 nF
PSR (dB)	-19.2 @100MHz	NR	-43dB @1MHz
Quiescent Power	4 mW	4.9 μW	0.42 mW
Min drop out (V)	0.3	0.05	0.15

NR-Not Reported NA -Not Applicable

of the regulator is derived, measured, simulated, and plotted in Fig. 5. The output impedance is found to be less than 1Ω across frequencies thereby making the IM_3 of the DAC (Fig.1) almost flat across the two-tone spacing.

III. Measurement Results

The prototype is designed in TSMC 65nm LP technology (Fig.9b)) and is packaged in a 6x6 48-pin QFN package. The total area occupied by design is 0.0237 mm^2, including 0.009 mm^2 of the opamp and compensation capacitance and 0.0147 mm^2 of load capacitance. The regulator regulates the output voltage to 1.2V from 1.5V supply with a bias current of 1.8mA. The first stage consumes about 1mA current to realize the unity gain bandwidth of about 200MHz while driving 150pF. Fig.6 shows the line regulation across temperature. The minimum power supply needed for the regulator is about 1.5V resulting in a regulation of 0.03%. Fig.7 shows the measured load regulation across temperature and 15 chips. The regulator, designed for a 15mA output current, has a load regulation of 0.17%. The noise is measured by capturing the output data with Rohde Schwarz (RTO6). The measured noise spectral density is 10 μV/$\sqrt{Hz}$ at 1Hz, as shown in Fig.8, and it closely matches the simulation results. The design uses a boot-strapped NMOS transistor as the pass gate using a standard Nakagome charge pump with a 1GHz clock. Hence, to understand the effectiveness of the filter (R_4 and C_3), the clock spurs are measured at the output. The measured clock spurs at the regulator's output are about -99.4 dBm, as shown in Fig. 9a). Fig. 10 shows the simulation of IM_3 of the RF DAC with the proposed regulator and the IM_3 is flat at ≈80dB across the two-tone spacing at the input, thanks to the low output impedance of the regulator.

Table 1 shows the performance summary and its comparison with state-of-the-art. Since there are no regulators designed specifically for re-timer latches in the literature, the comparison is made with stand-alone regulators. Recently, most stand-alone regulators aim to reduce the load transients and increase efficiency, and they adopt digital and hybrid techniques, but they result in output spurs. Hence, these regulators cannot be used in context to re-timer latches as they demand higher spectral purity and lower output impedance for achieving higher IF bandwidth. Further, the output impedance of the regulator is not measured or reported in the literature. The proposed regulator achieves an output impedance of less than one Ω for the entire frequency band with the clock spur of -99dBm while delivering 15mA current to re-timer latches.

IV. Conclusion

An ultra-low-output impedance voltage regulator particularly suited for re-timer latches in NRZ RF DAC is proposed and implemented in TSMC 65nm LP CMOS technology. The regulator achieves the output impedance of less than 1 Ω across the entire frequency band, resulting in almost flat IM_3 across the two-tone spacing in an NRZ RF DAC. Although the circuit used gate boot strapping at the pass gate spur, measured at the output of the regulator is -99 dBm.

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