A 0.193A/mm^3 89.8% 24V-1V Dual-path Hybrid Dickson Converter with Fully Integrated Dynamic Charge Transfer Bootstrapped Gate Drivers

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***Abstract*—To meet the growing power demands of large-scale data centers, high-voltage point-of-load converters are essential for achieving high current density and compact passive components, particularly switched inductors. This paper presents a 0.193A/mm^3 GaN/Si-based dual-path hybrid Dickson (DPHD) converter that enables 24V-to-1V direct conversion with 89.8% peak efficiency and a 6A output load using 6mm^3 inductors. This design features fully integrated bootstrap (BST) drivers with only 5.3nF of on-chip BST capacitance.**

***Index Terms*—High conversion ratio, small inductor, dual-path, fully integrated bootstrap capacitors, passive reduction.**

I. Introduction

Data center power management units (PMUs) are adopting multilevel, multiphase, single-stage hybrid, and capacitor-assisted converters [1]-[6] to minimize losses in high-voltage down conversion. A compact footprint is crucial, with the reduction of inductor area being a key focus of design. This paper introduces a DPHD 24:1V converter, featuring (1) on-chip Si and off-chip GaN integration for high conversion, (2) significant inductor current reduction for improved efficiency, and (3) fully integrated BST drivers eliminating all passive bootstrap capacitors and additional high voltage (HV) rails.

II. Dual-path Hybrid Dickson (DPHD) Topology

As shown in Fig. 1, small SMD inductors reduce volume by 16× compared to large inductors but suffer from 8× higher DC resistance (DCR) and 5× lower current rating, limiting efficiency and output current (I_O). To enable their use, reducing inductor current (I_L) is critical. An always dual-path (ADP) topology [7] splits 50% of output current across two capacitors, halving total inductor current, but its limited voltage conversion ratio (VCR) restricts high-voltage applications. Inspired by the (one) dual-path hybrid Dickson converter, the merged DPHD converter structure integrates the dual-path technique into a hybrid Dickson structure. The high-side Dickson stage reduces voltage stress by 4× and quadruples the duty ratio [1]. The low-side dual-path stage includes three switches (S_{CH1}, S_{CH2}, S_{CL}) and one capacitor (C_L) to reduce 30% in I_L at a 28.6% duty ratio for 24:1V conversion. To further minimize inductor current, the proposed (double) DPHD converter incorporates two parallel dual-path

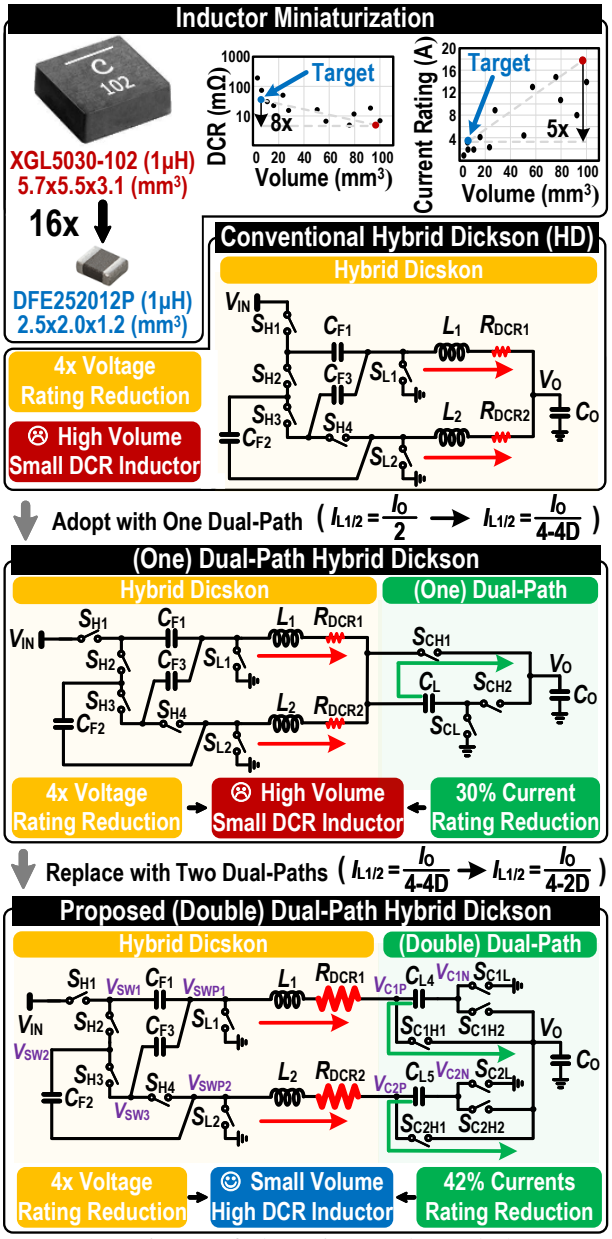


Fig. 1. Comparisons of the prior works and the proposed DPHD converter.

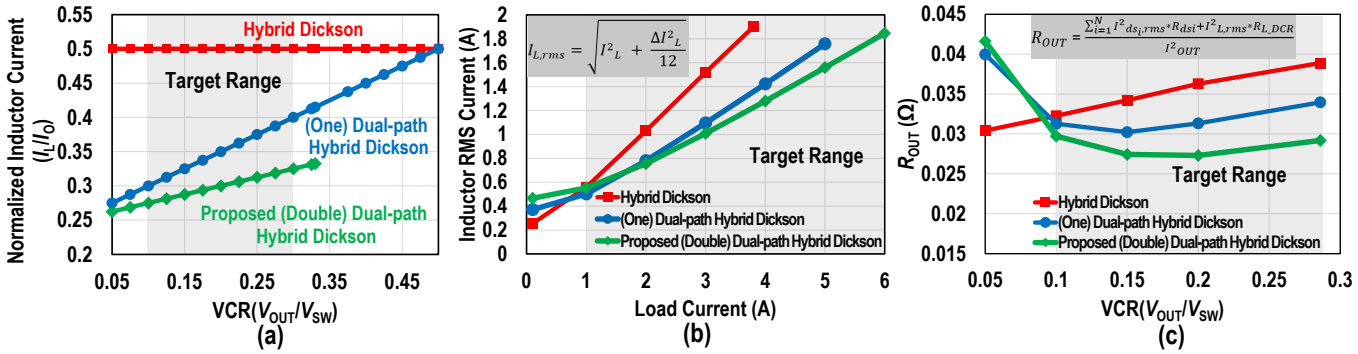


Fig. 2. Comparison of (a) normalized inductor current, (b) inductor RMS current, and (c) equivalent R_{OUT}.

circuits, achieving the lowest normalized inductor current, inductor RMS current, and equivalent output resistance (R_{OUT}) among compared topologies, as shown in Fig. 2. This proposed structure enables a large VCR ratio with 42% less inductor current at the same duty ratio. Fig. 3 illustrates the proposed DPHD operation: In Φ_1: C_{F1}, C_{F3}, C_{L5}, and L_1 charge, while C_{F2}, C_{L4}, and L_2 discharge. An auxiliary path (S_{C1L}-C_{L4}-S_{C1H1}) assists in reducing I_L. In Φ_2: C_{L4} and C_{L5} charge, while L_1 and L_2 discharge. In Φ_3: C_{F2}, C_{L4}, and L_2 charge, while C_{F1}, C_{F3}, C_{L5}, and L_1 discharge. One another current path (S_{C2L}-C_{L5}-S_{C2H1}) form to further reduce I_L. In Φ_4: Repeats Φ_2. This interleaved, symmetrical structure ensures balanced capacitor voltages and inductor currents naturally across all phases.

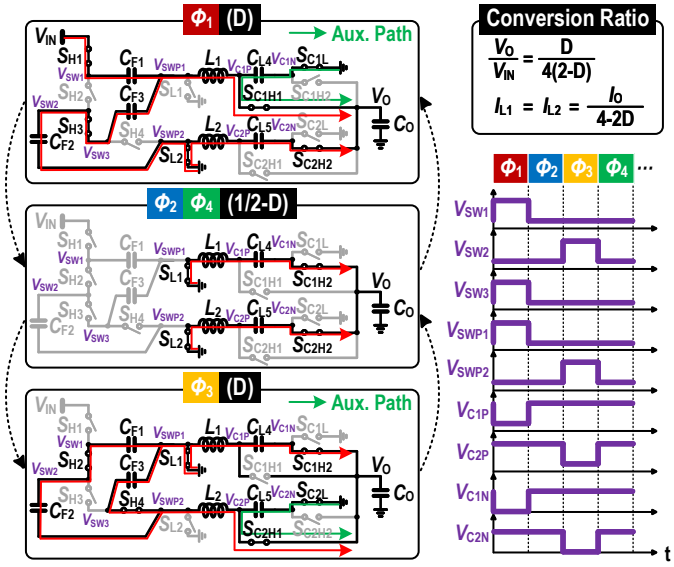


Fig. 3. Operating sequence of the proposed DPHD converter.

III. Architecture of the Proposed Digitally Controlled DPHD Converter System

Fig. 4 illustrates the converter system architecture, highlighting on-chip components. The design incorporates four GaN FETs and eight on-chip silicon power FETs. Fully integrated BST circuits with a DCT controller eliminate all off-chip BST capacitors. An 11-bit, 312ps resolution programmable digital PWM controller generates the reliable gate signals and dedicated deadtimes for soft switching. Low-side

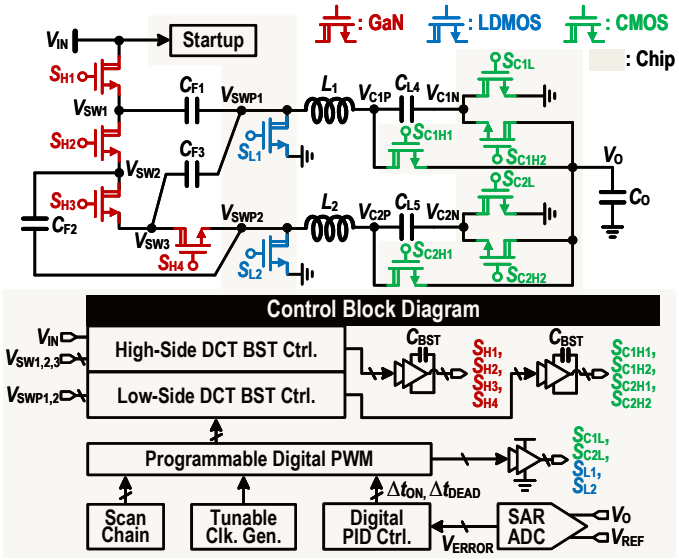
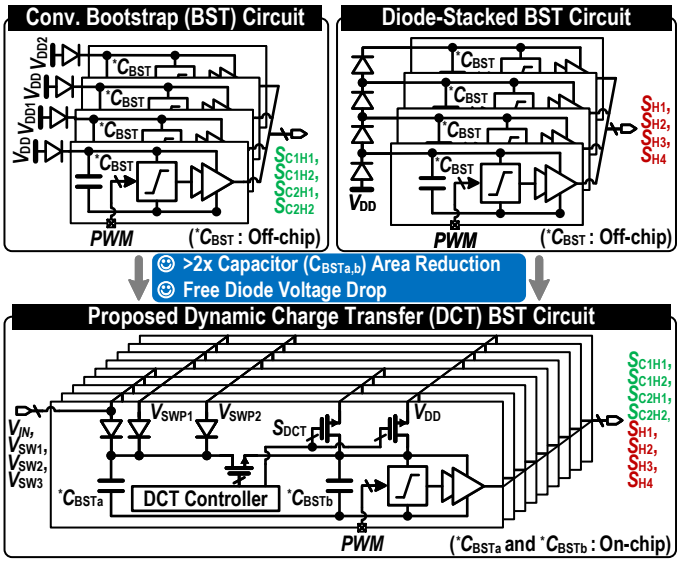


Fig. 4. Overall architecture of the proposed DPHD converter.

switch gate signals (S_{L1}, S_{L2}, S_{C1L}, and S_{C2L}) are sent directly to gate drivers, while high-side DCT BST gate drivers power GaNs, and low-side DCT BST drivers enable the floating silicon power FETs. To maintain stability during load transient, a 6-bit SAR ADC senses and samples V_O, and a digital PID compensator ensures tight regulation.

IV. On-chip BST with DCT Controller

In Fig. 5, a conventional BST circuit requires a capacitor C_{BST} at least 10x larger than an input capacitance (C_G) of the power switch to limit voltage drop to 10%. To avoid additional HV VDD rails, conventional diode-stacked BST circuits use a single VDD, but multiple diode voltage drops weaken high-side power switches turn-on, increasing conduction loss and limiting peak current. The proposed BST circuits integrate a dynamic charge transfer (DCT) controller to minimize total C_{BST} and eliminate gate drive voltage drop. Fig. 6 illustrates of the circuit driving power switch $S_{H<i>}$, which includes two C_{BST} capacitors ($C_{BSTa<i>}$, $C_{BSTb<i>}$) and a DCT-controlled charge transfer switch $S_{DCT<i>}$. For example, to turn on S_{H2}, the DCT controller operates as follows: ① high-voltage precharge: When S_{H3} is on, C_{BSTa2} charges to $V_{IN}/2$ via V_{SW1}, while C_{BSTb2} charges to 5V from V_{BST3}. A dummy capacitor



Bootstrap (BST)	C_{BST} Value	V_{BST}	Parasitic
Conv. BST	C_{BST} >10 x $^*C_G$	4.4V	Board and Package
Diode-Stacked BST	C_{BST} >10 x $^*C_G$	2.6-4.4V	Board and Package
Proposed DCT BST	C_{BSTa}+ C_{BSTb} = <5 x $^*C_G$	5V	N/A (On-chip)

($^*C_G$: Input Capacitance of the power switch)

Fig. 5. Comparison of conv. vs. proposed BST circuits.

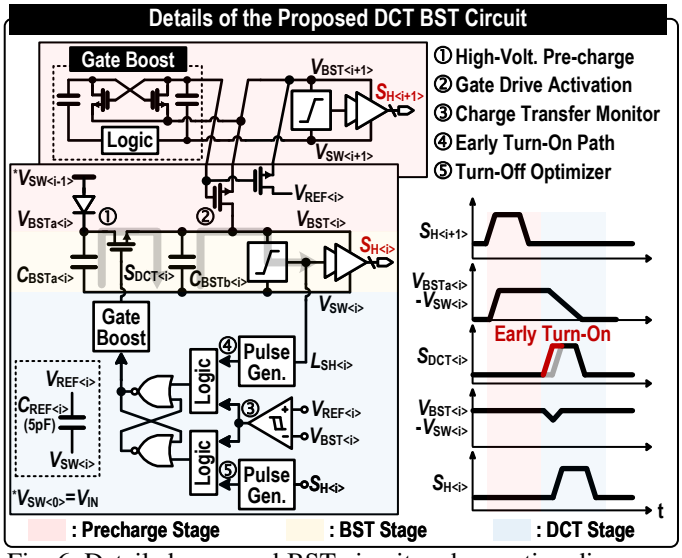
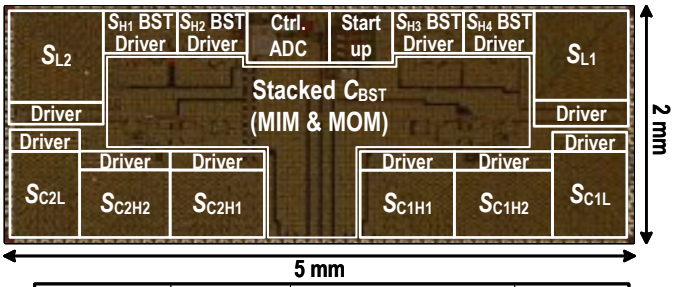


Fig. 6. Detailed proposed BST circuit and operation diagrams.

C_{REF2} (5pF) sets the reference voltage V_{REF2}. A gate boost circuit replaces the diode for lower voltage drop. ② gate drive activation: When L_{SH2} is high, input capacitance of S_{H2} is charged from C_{BSTb2}. ③ charge transfer monitoring: A dynamic charge detector monitors V_{BST2}. If it falls below V_{REF2}, S_{DCT2} turns on, initiating charge transfer. ④ early turn-on: To mitigate loop delay and voltage drop, S_{DCT2} is activated immediately when L_{SH2} goes high. Charge transfer stops when V_{BST2} equals V_{REF2}. ⑤ turn-off optimization: An off-detector mode minimizes turn-off delays, ensuring fast switching. The proposed DCT controllers improve the speed and efficiency of BST, reducing the capacitance of the low side of BST by 60% and the capacitance of the high side of BST by 50%, allowing full integration of the chip.



Process	Chip Area	Total C_{BST} Value / Area	Core V_{DD}
0.18μm BCD	10mm²	5.3nF / 2.9mm²	5V

Device	S_{H1}-S_{H4}	L_1, L_2	C_{H1}, C_{H2}	C_{H3}	C_{L4}, C_{L5}
Value	40V GaN	1μH (1008)	1μF (0603)	1μF (0402)	1μF (0402)

Fig. 7. Photo of chip and PCB prototype.

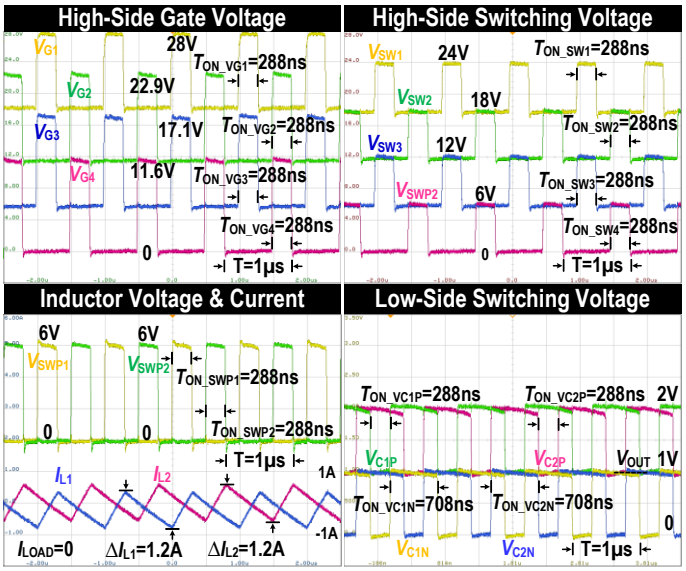


Fig. 8. Measured steady-state waveforms of the DPHD converter for 24V-1V conversion at 1MHz.

V. Measurement Results

A 5×2 mm², 0.18μm BCD prototype chip and a completed board are shown in Fig. 7. The chip and two inductors are on the front, while four GaNs and five capacitors are on the back, within a 13 x 8.5mm² area. Fig. 8 illustrates sufficient gate voltages, balanced switching node voltages, and balanced inductor currents at 1MHz. Four high-side GaNs (S_{H1}-S_{H4}) fully turn on, and the DPHD converter steps 24V V_{IN} down to 1V V_{OUT}. Fig. 9(a) shows efficiency from 0.5–1.6MHz, peaking at 89.8% at 1MHz. The inductor current reduction ratio remains around 58% up to 6A load. The transient response shows recovery within 165μs for 3A/4A load steps, with a maximum droop of 160mV, as shown in Fig. 9(b). Fig. 9(c) shows estimated loss breakdown, which indicates inductor DCR loss savings increase from 20.8% to 34.4% as

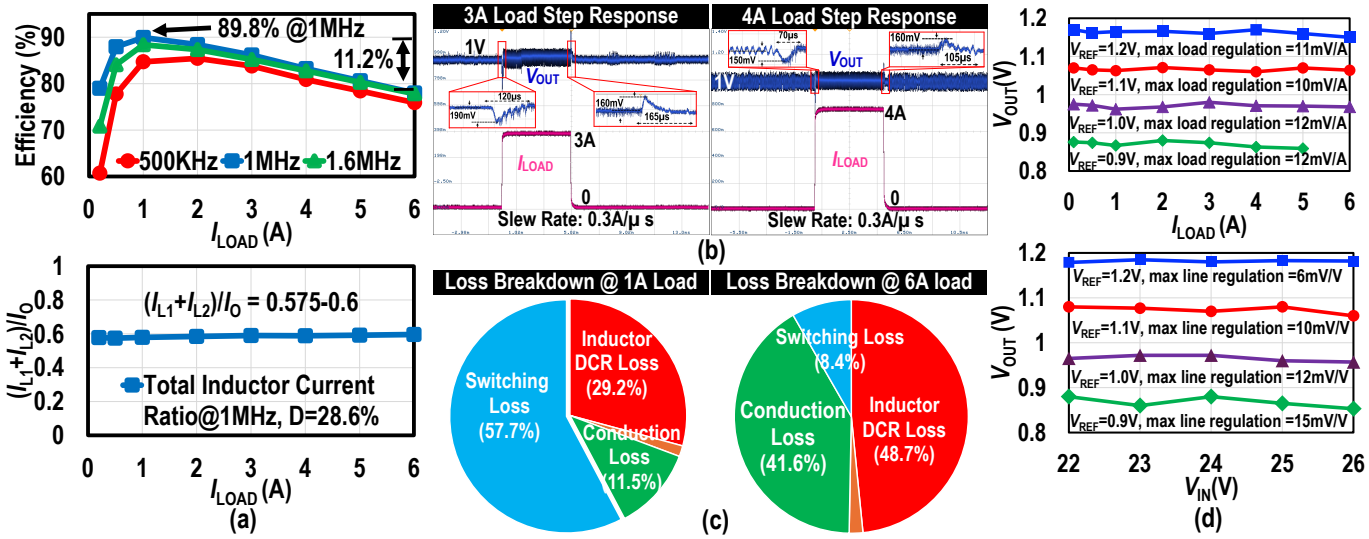


Fig. 9. Measured results of the DPHD converter for 24V-1V conversion at 1MHz: (a) efficiency curves and normalized total inductor current ratio, (b) load step responses, (c) estimated loss breakdown, and (d) load and line regulation characteristics.

TABLE I
COMPARISON WITH STATE-OF-THE ART CONVERTERS

	APEC 2019 [1]	JSSC 2020 [2]	ISSCC 2020 [3]	ISSCC 2021 [4]	ISSCC 2023 [5]	Proposed
Technology	Discrete	180nm BCD	180nm BCD	180nm BCD	180nm BCD	180nm BCD
Topology	Dual-phase Multi-inductor	Double Step Down (DSD)	Tri-state Double Step Down	12-level series-capacitor	Dual-path SC	Hybrid Dickson Dual-path
Input Voltage V_{IN}	48V	48V	12-24V	36-60V	9-16V	12-24V
Output Voltage V_O	1-5V	1V	1V	0.5-1V	0.6-1.6V	1V
Max Load Current I_{OUT}	100A	1.5A	3A	8A	5A	6A
Power Switches	GaN	GaN	Si	Si/GaN	Si	Si/GaN
# of Flying Capacitors	3	1	2	11	4	5
Voltage Reduction (V_{IN}/V_{SW})	4x	2x	4x	12x	3.6x	4x
Inductor	4x1μH	2x0.9μH	2x0.56μH	2x0.1μH	1x0.68μH	2x1μH
Inductor Volume (%)	79%	74%	82%	84%	76.9%	38.6%
I_L/I_{OUT} Ratio	1	1	1	1	0.6-1	0.25-0.5
C_{BST} Integration	Off-Chip	Off-Chip	Off-Chip	Off-Chip	Off-Chip	Fully On-Chip
Peak Efficiency	90.9%@48-1V, 333kHz	85.4%@48-1V, 100kHz	88.3%@24-1V, 100kHz	90.2%@48-1V, 2.5MHz	94.5%@9-1.2V, 1MHz	*89.8%@24-1V, 1MHz
Peak Current Density (A/mm^3)	*0.027	*0.015	*0.025	0.012(*0.061)	*0.036	0.027(*0.193)

*Power efficiency and current density for power stage area only (estimate from graph).

load rises from 1A to 6A. Fig. 9(d) presents load and line regulation, with maximum values of 12mV/A and 15mV/V, respectively. Table I compares performance with state-of-the-art designs. The peak current density is 0.193A/mm^3 with only 38.6% inductor area. The DPHD converter achieves significant inductor current reduction by 25-50%, while DCT BST circuits minimize BST capacitor sizes by 50-60%.

VI. Conclusions

This paper proposes a 24:1V dual-path hybrid Dickson converter achieving 89.8% peak efficiency and 0.193A/mm^3 current density. The proposed fully integrated bootstrap drivers with a dynamic charge transfer controller replace all passive bootstrap capacitors with just 5.3nF on-chip capacitors.

Acknowledgment

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