A 12-bit 1-GS/s 5.1-mW Pipelined ADC Using an Open-Loop Floating Inverter Amplifier with Residue-Dependent Integration Time Compensation

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***Abstract*—A 12-bit 1-GS/s three-stage pipelined analog-to-digital converter (ADC) using a new analog compensation technique to improve residue amplifier (RA) gain linearity is presented. The proposed residue-dependent integration time compensation (RITC) technique utilizes the time residue from the time-domain sub-ADC to track the variation of the voltage residue at the input of RA. The type of RA is an open-loop integrating floating inverter amplifier (FIA), and its compressive nonlinearity is well compensated by generating the input-dependent amplification time with the time residue. The prototype ADC fabricated in 28-nm CMOS occupies a core area of 0.014 mm^2. Benefitting from the proposed techniques, the prototype ADC achieves high linearity and consumes 5.1 mW from a 1-V power supply running at 1 GS/s. The SNDR and SFDR are 61.3 dB and 75.7 dB with a Nyquist input, respectively, leading to a 171.2-dB Schreier FoM and 5.4-fJ/conversion-step Walden FoM.**

Keywords—Pipelined ADC, floating inverter amplifier (FIA), residue amplifier, linearity compensation

I. INTRODUCTION

Pipelined/Pipelined-SAR ADC has become the main choice for the next-generation wireless standard because it can balance accuracy and speed [1]. The residue amplifier (RA) is one of the most critical components in a pipelined ADC since it reduces the noise requirement of the backend stages. However, the RA often dominates the significant power budget to meet the demand for fast and accurate amplification, degrading the overall energy efficiency. Compared to traditional closed-loop amplifiers, open-loop integrating amplifiers feature low power consumption and a simple architecture, making them widely adopted in applications [2], [3]. However, open-loop amplifiers also suffer from poor linearity under large signal swings, which has led previous works to employ sub-ADCs with higher resolutions. Nevertheless, sub-ADCs with more than 5-bit resolution ([2], [3]) inherently limit the overall conversion speed of the ADC.

This work proposes an analog time-assisted compensation method to address the linearity problem. We utilize the time residue (T_{res}) of the time-domain (TD) sub-ADC (3.5-bit) to compensate for the amplification time of the integrating FIA: since the T_{res} of sub-ADC has similar information to the voltage residue (V_{res}) in a CDAC, it allows the residue-dependent amplification time to track the variation of the input. The TD Flash sub-ADC completes the fast quantization, while the generation of T_{res} parallels the amplification. Thus, this technique improves the linearity of RA without additional time budget. To verify this technique, we implemented a 12-bit three-stage pipelined ADC in 28-nm CMOS; that exhibits an SNDR of 61.3 dB near Nyquist when running at 1 GS/s with 5.1-mW power consumption, contributing to a 171.2-dB Schreier FoM (FOM_S) and 5.4-fJ/conv.-step Walden FoM (FOM_W).

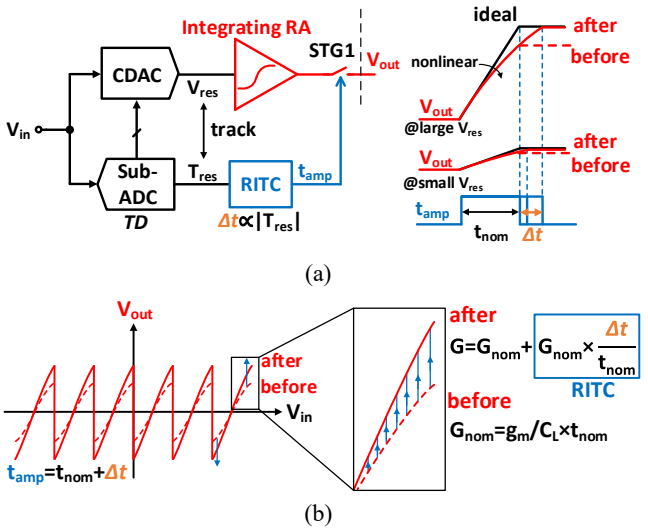

Fig. 1. (a) Block diagram of the first stage in the pipelined ADC and the principle of residue-dependent integration time compensation; (b) transfer function of RA output voltage V_{out} and ADC input voltage V_{in} before and after compensation.

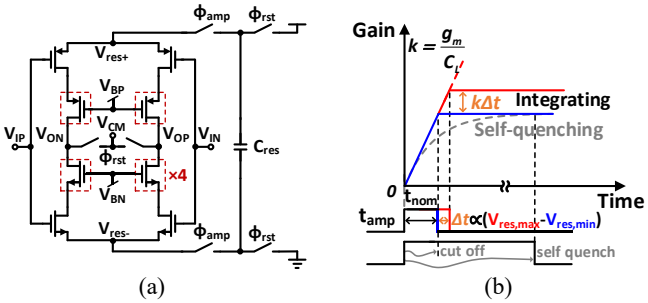

Fig. 2. (a) Circuit implementation of the cascaded FIA; (b) comparison between integrating FIA and self-quenching FIA.

II. PROPOSED LINEARITY IMPROVEMENT TECHNIQUE

Fig. 1(a) depicts the block diagram of the proposed residue-dependent integration time (RITC) technique. In the first stage of a SHA-less pipelined ADC, input voltage (V_{in}) is sampled and then folded in CDAC according to various digital outputs of the sub-ADC. After capacitor switching, voltage

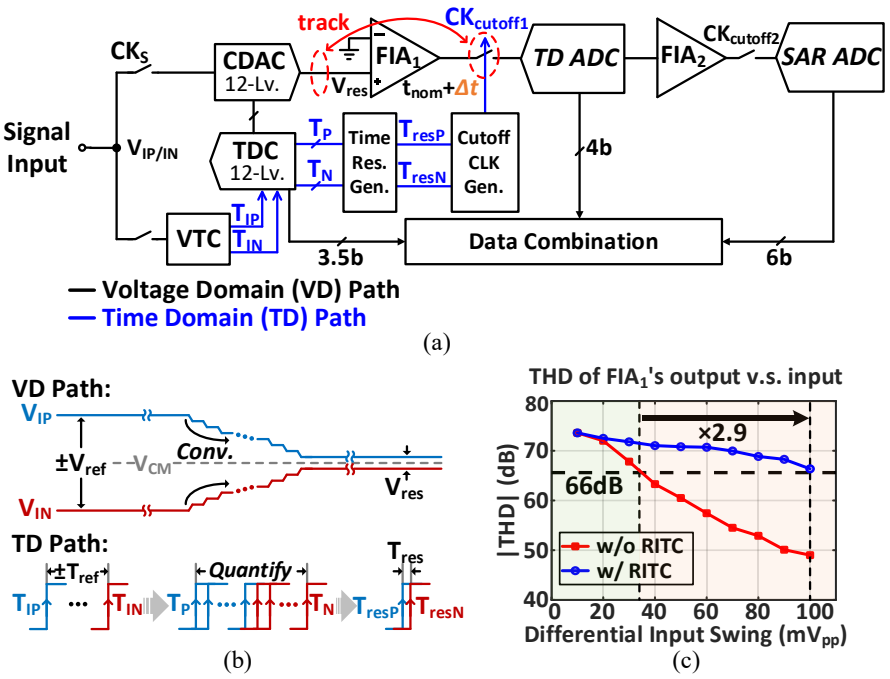

Fig. 3. (a) Block diagram of the 12-bit pipelined ADC; (b) the relationship between VD and TD path; (c) simulated THD of the output of FIA_1 with and without RITC technique.

residue V_{res} is held in CDAC as the input of integrating RA. We choose the TD Flash ADC to quantify the MSB of the first stage as the sub-ADC, due to its small kickback problem, excellent comparator offset performance, and fast quantization speed [4], [5]. While inheriting the above advantages, we further utilize the time residue T_{res} in the TD Flash ADC to generate the Δt through the RITC block, compensating for the amplification time (t_{amp}) of the RA.

The principle can be observed on the right of Fig. 1(a). The effective amplification (or integration) time t_{amp} is given by

$$t_{amp} = t_{nom} + \Delta t \tag{1}$$

where t_{nom} is the nominal integration time and Δt is the time quantity, respectively. The signal-dependent Δt is generated by the RITC block and proportional to the absolute value of T_{res}, which can be expressed as

$$\Delta t \propto |T_{res}| \tag{2}$$

As shown in Fig. 1(a), the ideal voltage curve increases linearly with the integration time (black line). However, compressive nonlinearity in actual practice makes the gain smaller at a larger input (red line). The principle of the proposed technique is to expand the integration process with the increase of RA's input (i.e. V_{res}). Unlike voltage-domain Flash sub-ADCs, the residue information can be extracted from TD sub-ADCs [6]. Time residue in TD sub-ADC and voltage residue in CDAC share the same residue information and track each other. As a result, we can get a longer Δt (thus t_{amp}) at a larger V_{res} according to (1) and (2). After the extension of the integration time, a voltage compensation is achieved to make the output voltage (V_{out}) close to its ideal value. That means Δt is added to provide additional gain on the basis of t_{nom}, after the process of RITC (discussed later in Section III). Compared to V_{out} before compensation with a nominal gain G_{nom}, the linearity of V_{out} after compensation can be improved by reflecting the variation of the input in the scale of integration time (Fig. 1(b)).

In this design, integrating FIA serves as the RA, offering CMFB-free operation and high power efficiency due to its floating capacitor supply and current reusing. Fig. 2(a) illustrates the adopted FIA with cascoded structure. The cascoded FIA is implemented by cascoded transistors scaled ×4 than the input transistors. Unlike the self-quenching amplification of the open-loop FIA in [7], integrating-based amplification is employed in our work, as shown in Fig. 2(b).

III. ADC Architecture and Implementation

This section details the implementation of our 1GS/s 12-bit three-stage pipelined ADC: a 3.5-bit TD Flash ADC with RITC technique in the first stage, a 4-bit TD Flash ADC in the second stage, a 6-bit SAR ADC with a ping-pong comparator topology in the third stage, two integrating FIAs employed between the neighboring stages, a data combination for alignment and a clock generator.

In the first stage, after the TDC quantizing the converted time signals (T_{IP} and T_{IN}) produced by VTC, the digital codes are feedback to CDAC for subtraction and then the voltage residue V_{res} is obtained in the main CDAC. Simultaneously, the time residue T_{resP} and T_{resN} are produced by the time residue generator (TRG) through the blue-highlighted TD path. Then, the differential time residue T_{resP} and T_{resN} are converted to the residue-dependent $CK_{cutoff1}$ (single-ended) by the cut-off CLK generator to truncate the integration process. The cut-off CLK generator is composed of a differential-to-single-ended block, a time-to-voltage converter (TVC) and a VTC, which is employed to scale the Δt with different current ratios [5]. It is worth noting that the generation of T_{resP}, T_{resN} and subsequent $CK_{cutoff1}$ performs in parallel with the integration, preventing extra and unnecessary phase. The relationship between the voltage-domain (VD) path and TD path can also be observed in the Fig. 3(b).

$CK_{cutoff1}$ tracks the variation of V_{res} over time, and imposes that the practical t_{amp} of FIA_1 becomes $t_{amp} = t_{nom} + \Delta t$, where Δt only depends on the T_{res}. t_{nom} has a fixed

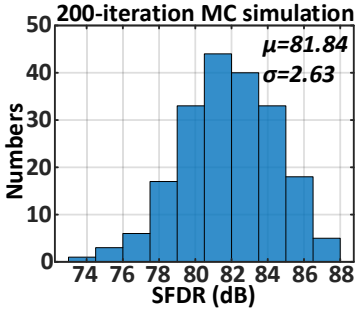

Fig. 4. Monte Carlo simulation results of the overall ADC SFDR, considering the mismatch in TD path.

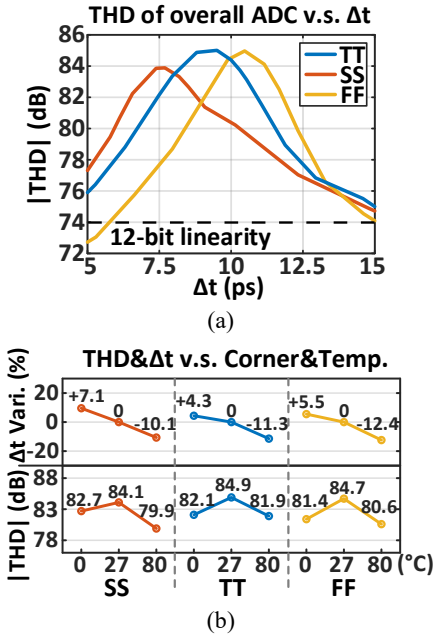

Fig. 5. Simulated THD of overall ADC with (a) the variation of Δt, and (b) variation in various corners and temperatures.

time length and is designed as around 250 ps at 1 GS/s. Fig. 3(c) compares the simulated THD of FIA_1's output with and without RITC. To ensure a >12-bit linearity of the overall ADC, the target linearity of FIA_1's output is supposed to be higher than 9-bit (55 dB). The |THD| of FIA_1 without RITC significantly decreases with the growth of input swing, which finally falls below 50 dB. In contrast, the |THD| of FIA_1 with RITC can achieve >66 dB within a 100-mV_{pp} input, expanding the input swing by 2.9× and leaving enough margin for high-linearity amplification. In Fig. 9 (top right), the measured FFT spectrum at 1GS/s implies a 13.5dB improvement of the third-order harmonic (HD3).

The SFDR of overall ADC remains higher than 74 dB in the 200-iteration Monte Carlo simulations as indicated in Fig. 4. The time delays in the TD path (refer to the blue-highlighted path in Fig. 3(a)) are biased by current sources and all use the same or proportional sizes for inner tracking [5]. The typical corner shown in Fig. 5(a) achieves over-12-bit linearity of the overall ADC with Δt changing from 5 to 15 ps. Furthermore, Fig. 5(b) also illustrates that the variation of Δt (SS-FF corner, 0-80°C temperature) is limited to <13% (~1ps variation), leading to a safe margin to maintain a near 80-dB linearity under process and temperature variation.

Fig. 6(a) illustrate the circuit implementation of TDC and TRG. We adopt a 3.5-bit Flash TDC with the unit delay (i.e.

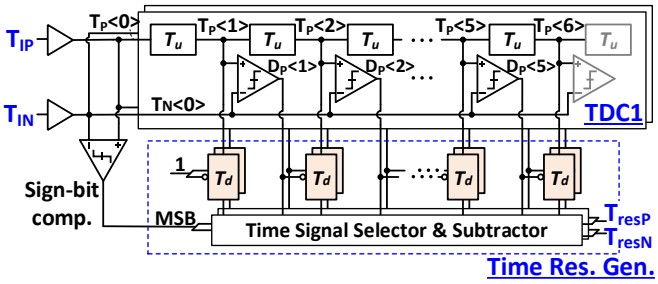

Fig. 6. Circuit implementation of TDC and TRG.

time LSB) T_u=20 ps. The comparison of the input time signals T_{IP} and T_{IN} (converted by VTC) produces a sign bit (MSB) first, then delayed by a series of T_u and cross-compared by time comparators to complete a total 12-level quantization. In the TRG, the closest time signals in T_P<1:6> and T_N<1:6> are selected by the time signal selectors according to the bubble signals, which are generated by the comparison results D_P<1:5> and D_N<1:5>. Then the residue time range is further subtracted by $T_u/2$ and converted to $[-T_u/2,+T_u/2]$ to match the range of V_{res}. To further improve energy efficiency, terminable delays (T_d) are employed to block the transmission of time signals that are useless for TRG, based on the decisions of the former comparators.

IV. Measurement Results

The prototype ADC fabricated in 28-nm CMOS occupies a core area of 0.014 mm^2 (Fig. 7). One-time trimming is completed on chip for the VTC and the ratio of Δt, while the foreground calibration is performed for the capacitor weight and gain error. Fig. 9 displays the measured static performance, where the DNL and INL are +0.47/-0.34 LSB and +0.82/-0.84 LSB, respectively. Fig. 9 also illustrates the measured dynamic performance at a low input frequency and near the Nyquist frequency. The effect of RITC technique is verified in the measurement (top right). The FFT spectrum (decimated by 25) at 1 GS/s implies a 6.4-dB and 13.5-dB improvement of the THD and HD3, respectively, for an input signal of 118.4 MHz. The input and sampling frequency sweep and the performance variation under ± 5% supply and 0-80°C temperature are shown in Fig. 10. Fig. 7 also shows the power breakdown. With a 1-V power supply, the power consumption is 5.1 mW, resulting in a 5.4-fJ/conv.-step FoM_W and 171.2-dB FoM_S. TABLE I and Fig. 8 summarize and compare the ADC performance with state-of-the-art.

V. Conclusion

This paper presents a scheme that utilizes the time residue generated by a time-domain sub-ADC to realize residue-dependent integration time compensation (RITC), thereby achieving large-swing and high-linearity open-loop integrating amplification. A 12-bit three-stage pipelined ADC is implemented with this technique, and a 13.5-dB improvement of HD3 has been verified from measurement. It obtained one of the best power efficiencies (5.4 fJ/conv.-step FoM_W) in reported high-speed pipelined ADCs, providing a competitive candidate for the new generation of wireless communication technologies.

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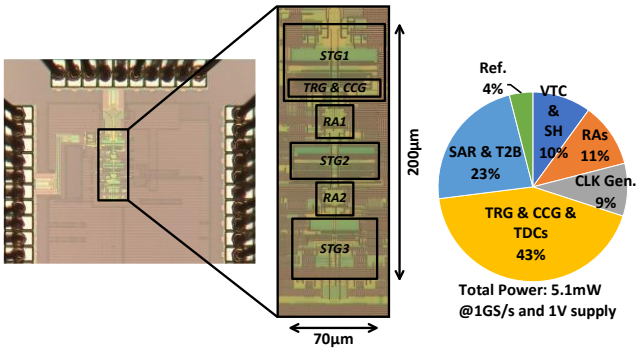

Fig. 7. Die micrograph and power breakdown.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work	ISSCC'19 W. Jiang	VLSI'20 B. Hershberg	ISSCC'23 M. Zhan	JSSC'23 W. Jiang
Process (nm)	28	28	16	28	28
Architecture	Pipe., TD, SAR	Pipe., SAR	Pipe.	Pipe., TI-SAR	Pipe., SAR
RA Type	Open-loop FIA	Gm-R	Ring Amp.	Ring Amp.	Closed-loop FIA
Area (mm^2)	0.014	0.009	0.095	0.016	0.018
Resolution (bits)	12	12	11	12	14
Sample Rate (MS/s)	1000	1000	1000	1000	500
SNDR @Nyq. (dB)	61.3	60.02	59.5	62.5	64.2
SFDR @Nyq. (dB)	75.7	74.56	75.9	80.5	80.55
Power (mW)	5.1	7.6	10.9	6.9	6.34
$FoM_{Schreier}$ (dB)	171.2	168.2	166.1	171.1	170.2
FoM_{Walden} (fJ/step)	5.4	9.3	14.1	6.3	9.6

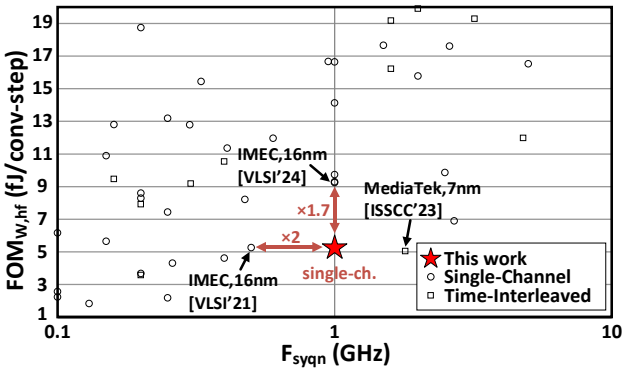

Fig. 8. The comparison of FoM_W between this work (single-channel) and other similar Nyquist ADCs [8].

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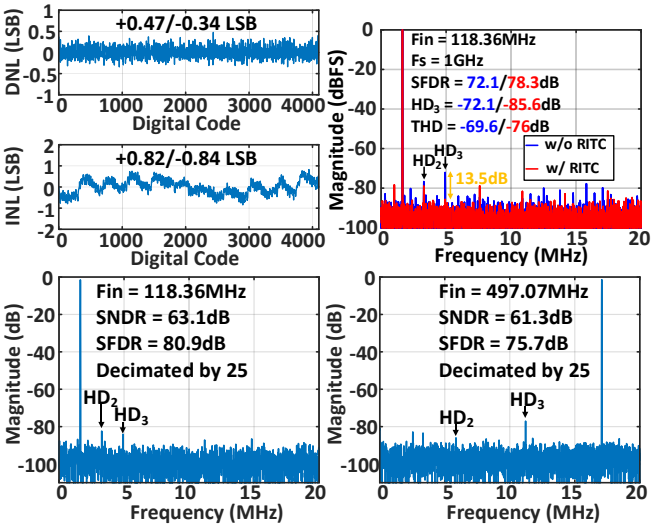

Fig. 9. Measured DNL/INL, measured FFT spectrum with/without RITC technique and measured dynamic performance (8192 points) running at 1 GS/s.

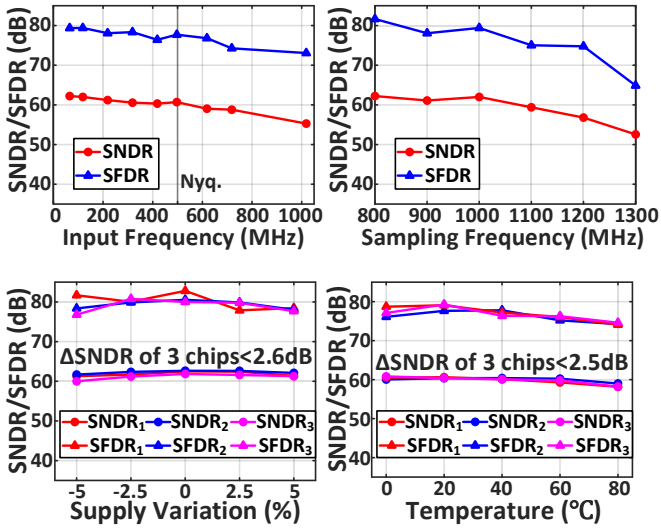

Fig. 10. Measured SNDR/SFDR versus input frequency and sampling frequency, and measured SNDR/SFDR of 3 chips versus supply and temperature variation.

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