A 16 MHz RC Frequency Reference With ±450 ppm Inaccuracy from -45ºC to 85ºC after Accelerated Aging

Karimeldeen Mohamed, Nandor G. Toth, Hui Jiang, Çağrı Gürleyük and Kofi A. A. Makinwa
Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands
Email:k.m.a.mohamed@tudelft.nl

***Abstract*— This paper presents a high-accuracy, low-drift 16 MHz RC frequency reference. It is based on a Wien bridge filter that incorporates silicided n-poly resistors and MIM capacitors, whose temperature coefficient is compensated by a PNP-based temperature sensor. After a 2-point trim, it achieves ±350 ppm inaccuracy from −45°C to 85°C, which increases to only ±450 ppm after accelerated aging. This represents competitive accuracy and state-of-the-art stability for RC-based frequency references, approaching that of their LC-based counterparts while dissipating lower power and occupying less area.**

Keywords*— *RC frequency reference, FLL, aging robust.

I. Introduction

RC frequency references are widely used in system-on-chip (SoC) applications due to their compactness, low power, and wide frequency range [1-6]. Several designs based on p-poly resistors have been proposed [1-3], due to their high sheet resistance and low-temperature coefficient (TC), resulting in excellent frequency inaccuracy (~100 ppm) after a 2-point trim. However, polysilicon resistors are highly susceptible to aging, leading to significant frequency drift (over 5000 ppm) after accelerated aging [4][7]. Lower drift (~1000 ppm) has been reported for designs based on (combinations of) metal, via, n-poly, and diffusion resistors [4,5]. However, the large TCs of these resistors (> 1000 ppm/°C) result in significant inaccuracy over temperature. In [4], a temperature and aging-compensated RC oscillator (TACO) is presented, which reduces long-term drift by synchronizing a main oscillator to an aging-robust reference oscillator that employs switched dual RC branches and duty cycling techniques. This approach slows down the aging of the reference oscillator and achieves ±1030 ppm inaccuracy after 500 hours of accelerated aging at 125 °C. However, the need for two oscillators increases system complexity. In [5], a 32-MHz RC frequency reference based on n-diff resistors, MIM capacitors, and a BJT-based temperature-compensation scheme is presented. It achieved ±900 ppm inaccuracy from −40 °C to 125 °C and ±1600 ppm after accelerated aging, benefiting from the stability of the n-diff resistors and the BJTs. Although LC-based frequency references can achieve lower drift (~100 ppm), they occupy more area and dissipate significantly more power [8].

In this work, an accurate and stable PNP-based temperature sensor is used to temperature-compensate a frequency-locked loop (FLL) that incorporates a Wien-bridge (WB) filter based on stable silicided n-poly resistors and MIM capacitors. The resulting frequency reference achieves competitive inaccuracy (±350 ppm) over temperature and state-of-the-art drift (~100 ppm), approaching that of LC-based frequency references, while dissipating significantly lower power.

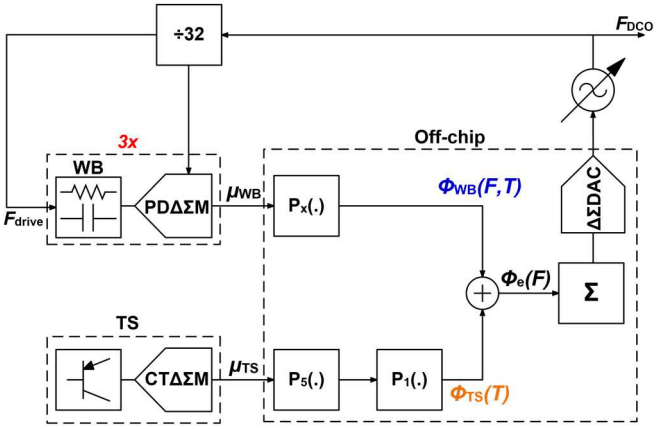

Fig. 1. Block diagram of the proposed RC references

II. Proposed Architecture

A simplified block diagram of the proposed frequency reference is shown in Fig. 1. It consists of an FLL in which the frequency (F_{DCO}) of a digitally-controlled oscillator (DCO) is locked to the phase shift of a WB filter. As in [1], the WB is driven at $F_{drive} = F_{DCO}/32$ by a rail-to-rail square wave, and its output phase shift is digitized by a phase-domain delta-sigma modulator (PDΔΣM). Due to the non-zero TC of the WB resistors, the modulator's digital output (μ_{WB}) will be a function of F_{DCO} and also of temperature. To compare their aging robustness, three WB filters were realized in this work, each based on a different type of resistor (metal, sn-poly, and via) as metal and via demonstrated good stability performance [4]. In addition, [9] illustrated the low drift characteristics of sn-diff. However, sn-diff parasitics hinder AC drive implying the usage of sn-poly instead. For accurate temperature compensation, a fixed Xth-order polynomial (P_X) is used to map μ_{WB} of each resistor type to a linear function of temperature, resulting in a pseudo-phase $\Phi_{WB}(F,T)$. For the metal and sn-poly WBs, $X = 4$, and for the via WB, $X = 2$. Similarly, a fixed 5th-order polynomial (P_5) is used to linearize the digital output (μ_{TS}) of a PNP-based temperature sensor (TS), resulting in a frequency-independent pseudo-phase $\Phi_{TS}(T)$. After scaling with a 1st-order polynomial, whose coefficients are determined by a two-point temperature trim, the two pseudo-phases are added to obtain a temperature-independent error signal $\Phi_e(F)$. This drives a digital integrator, whose output then adjusts the DCO's output frequency F_{DCO} such that at steady-state $\Phi_e(F) = 0$, thus locking F_{DCO} to a temperature-compensated point on the WB filter's phase characteristic. The loop update rate is ~500 Hz and has a closed-loop bandwidth of ~25 Hz.

A. PDΔΣM

As shown in Fig. 2 (bottom), the phase shift of each WB is digitized by a 1st order PDΔΣM, whose phase references ($\Phi_{0,1}$) and sampling frequency (F_{drive}) are derived from F_{DCO} by on-chip logic. Since the chosen resistor types have low sheet resistance, the sizing of the WB (R = 32 kΩ, C = 10 pF) involves a trade-off between power consumption and area. To further minimize power consumption, the PDΔΣM is based on a Gm-C integrator. Compared to the active-RC integrator used in [1], this choice allows the integrator's bias current to be decoupled from the WB current.

As shown in Fig. 3, the Gm-C integrator consists of a telescopic OTA with embedded phase-demodulating choppers that drive an integration capacitor (C_{int} = 8 pF) [10]. To accommodate the limited linear input range of the Gm-C integrator, the WB's output is attenuated by a factor of 1/16. Furthermore, resistive degeneration is used to enhance its linearity and to reduce power-supply sensitivity caused by the supply-dependent amplitude of the WB output. Gain-boosters provide sufficient loop gain (A_{OL} > 90 dB) to suppress quantization noise and ensure that the modulator is thermal noise-limited. They also create virtual grounds at the chopper inputs, thus suppressing error currents created due to the output impedance of the input pair and the offset of the cascodes [10], further improving the PSS. The small integrator swing (~50 mVpp) enables the use of triode-mode devices for common-mode feedback (CMFB).

B. BJT-based Temperature Sensor

To ensure accurate and aging-robust temperature compensation, a PNP-based temperature sensor is employed. As shown in (Fig. 2, top), two identical BJTs operated at a current density ratio of 7 are used to generate temperature-dependent voltages, ΔV_{BE} and V_{BE}, with PTAT and CTAT characteristics, respectively. Two resistors then convert these voltages into currents I_{PTAT} and I_{CTAT}, respectively, whose ratio is digitized by a 2nd-order ΔΣM. As in [11], the latter consists of a continuous time 1st integrator and an area-efficient switched capacitor 2nd integrator. The currents are integrated on C_{int}, with the flow of I_{PTAT} regulated by the output of the modulator's quantizer to balance the constantly flowing I_{CTAT}.

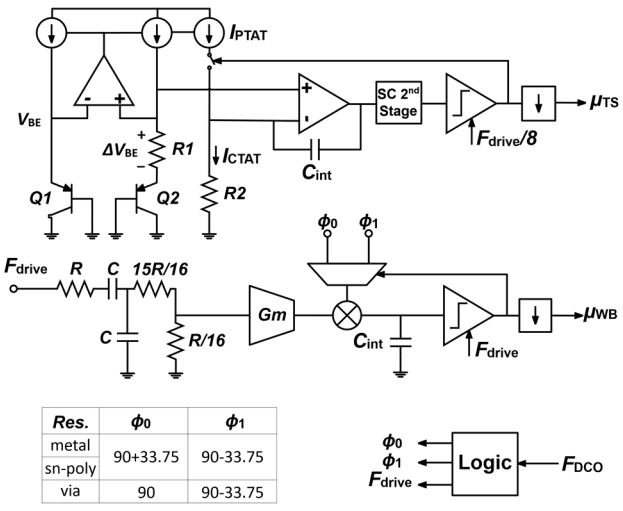

Fig. 2. Simplified single-ended circuit diagram of one of the three WB filters, its BJT TS (top), and the PDΔΣM (bottom).

As a result, the modulator's bitstream average (μ_{TS}) is proportional to I_{CTAT}/I_{PTAT}, which is a well-defined function of temperature [11]. Chopping and dynamic-element-matching (DEM) are used to mitigate component mismatch and the 1/f noise.

C. DCO

Fig. 4 shows the DCO, which consists of a 3-stage inverter-based ring oscillator. To reduce the spread in its output frequency over PVT, each stage is loaded by a tunable RC delay [2]. A fixed coarse trim is provided by a 4-bit tunable capacitor C_{coarse}, while fine-tuning across temperature is provided by varactors C_{fine}, which are driven by a 2nd order ΔΣ-DAC. To attenuate the modulator's quantization noise, its 1-bit output is filtered by a 3rd-order cascaded RC low-pass filter. For flexibility, the digital integrator, the ΔΣ modulator, and the linearization polynomials are implemented in an off-chip FPGA.

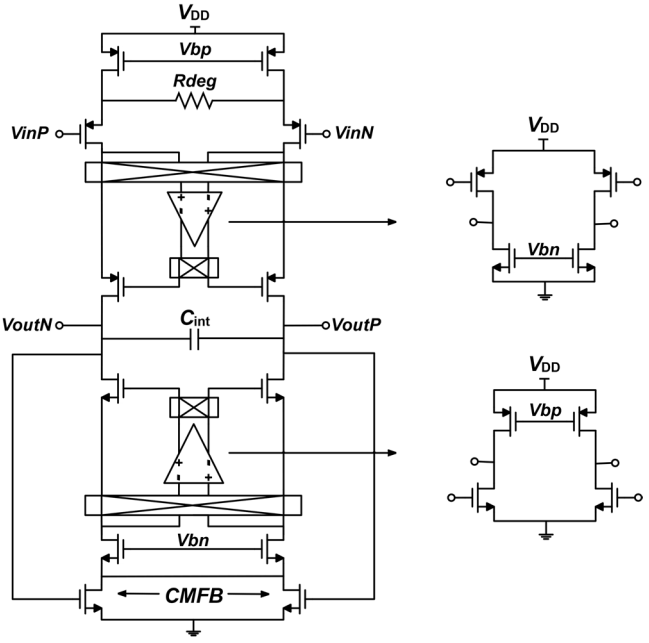

Fig. 3. Circuit diagram of the Gm-C integrator of the PDΔΣM.

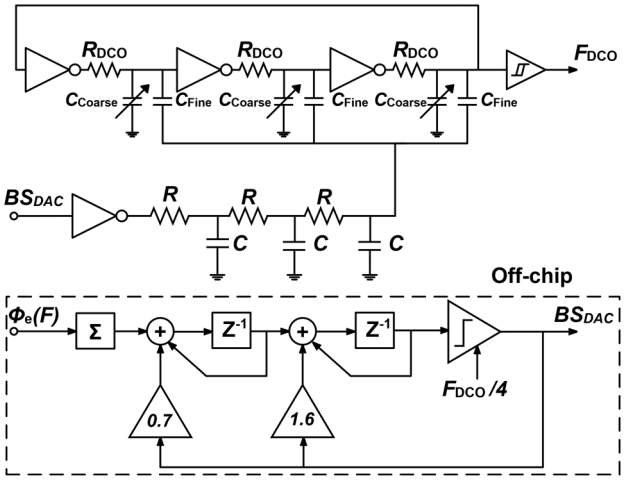

Fig. 4. Circuit diagram of the ΔΣDCO

III. MEASUREMENT RESULTS

The proposed frequency reference is implemented in a TSMC 180nm CMOS process. As shown in Fig. 10, each chip consists of three WBs and their identical PDΔΣMs, a DCO, and a TS. Neglecting the area of the unused blocks, the metal, sn-poly, and via FLLs occupy 0.25 mm^2, 0.22 mm^2, and 0.19 mm^2, respectively, and consume 87 µA from a 1.8 V supply. The power and area breakdown of the sn-poly FLL are shown in Fig. 10.

Sixteen samples packaged in ceramic DIL were characterized from -45°C to 85°C in a temperature-controlled oven and their exact temperature was determined with the help of a Pt-100 reference resistor. Fig. 5 shows the open-loop decimated bitstream output of the three WBs and the TS over temperature. The metal, sn-poly, and via WBs exhibit TCs of 3400 ppm/°C, 3100 ppm/°C, and 900 ppm/°C, respectively. After a 2-point trim, the corresponding FLLs achieve inaccuracies of ±300 ppm, ±350 ppm, and ±600 ppm, respectively (Fig. 6). In the case of the sn-poly WB, the ±0.025 °C inaccuracy of the TS translates into a frequency error of only 80 ppm and so it does not significantly limit the overall inaccuracy of the FLL.

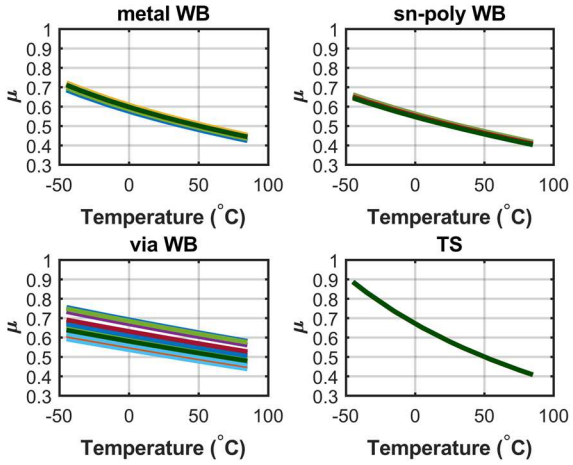

Fig. 5. Measured bitstream averages from -45 ºC to 85 ºC (16 samples) of the metal WB (top left), sn-poly WB (top right), via WB (bottom left), and BJT TS (bottom right).

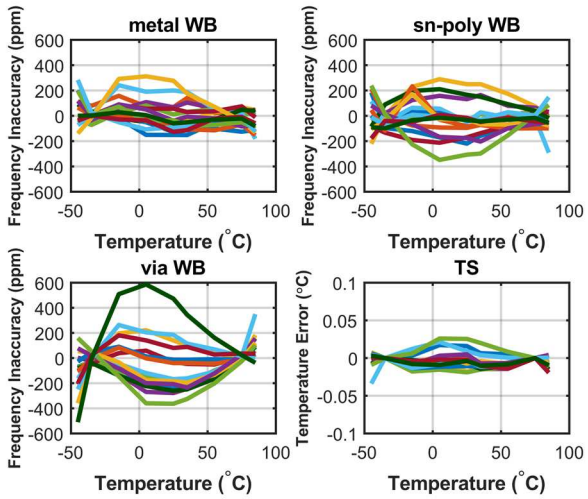

Fig. 6. Measured frequency inaccuracy from -45 ºC to 85 ºC before aging (16 samples), metal (top left), sn-poly (top right) and via (bottom left), and BJT TS inaccuracy (bottom right).

After accelerated aging for 168 hours at 150°C [5,7], the inaccuracy of the sn-poly FLL increases to just ±450 ppm (Fig. 7, top left), which corresponds to state-of-the-art drift performance. In contrast, the metal and via FLLs drift by 3% and 0.3%, respectively. This is significantly worse than prior art [4], which, however, describes a design fabricated in a different (65nm) process where the interconnects are implemented in copper rather than aluminium. The average inaccuracy shift of the FLL and the TS are shown in (Fig. 7, top right) and (Fig. 7, bottom right), respectively, and implies that the drift is mainly contributed by the BJT TS.

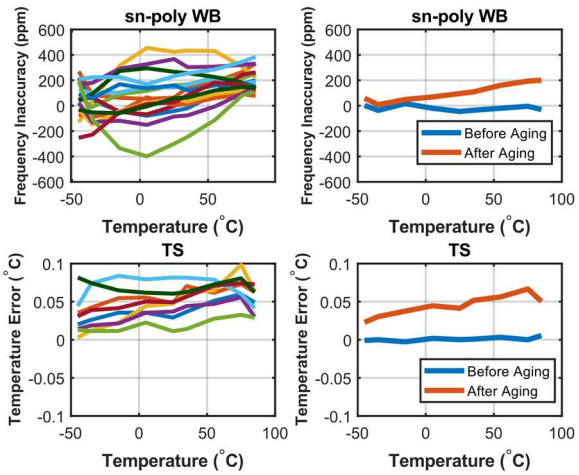

Fig. 7. Measured frequency inaccuracy from -45 ºC to 85 ºC after accelerated aging, sn-poly (16 samples, top left), and TS (8 samples, bottom left). Average inaccuracy shift, sn-poly (top right), and TS (bottom right).

Supply sensitivity characterization is shown in Fig. 8, where the voltage supply was varied from 1.6V to 2V. The worst-case samples show a variation of 600 ppm, which translates to a PSS of ~1500 ppm/V, mainly dominated by the WB. The sn-poly FLL achieves a closed loop period jitter of 21 ps and Allan deviation floor of 2 ppm at 10s stride (Fig. 9).

In Table I, the performance of the proposed RC frequency reference is summarized and compared to the state of the art. It achieves state-of-the-art drift without using any extra aging compensation overhead circuitry and competitive accuracy (±450 ppm) while maintaining comparable jitter, PSS, and power consumption.

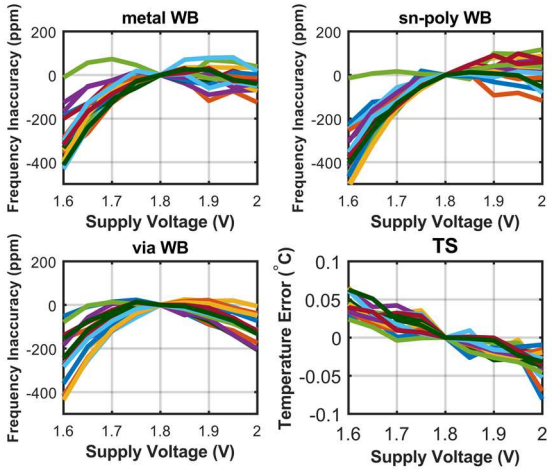

Fig. 8. Measured frequency inaccuracy vs. supply voltage before aging (16 samples), metal (top left), sn-poly (top right), via (bottom left), and TS (bottom right).

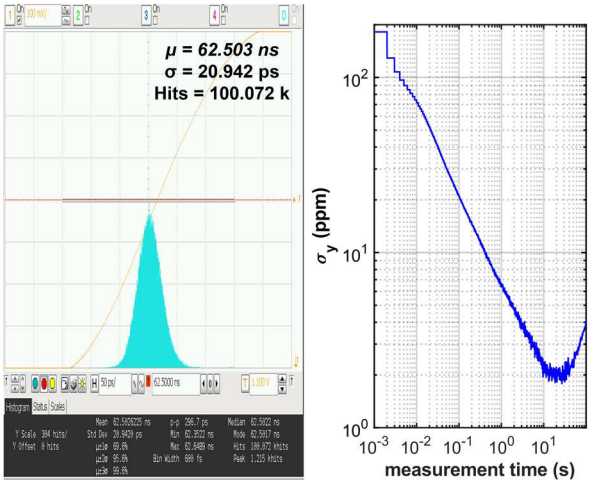

Fig. 9. Measured closed-loop period jitter (left) and closed-loop Allan deviation (right) of the sn-poly FLL.

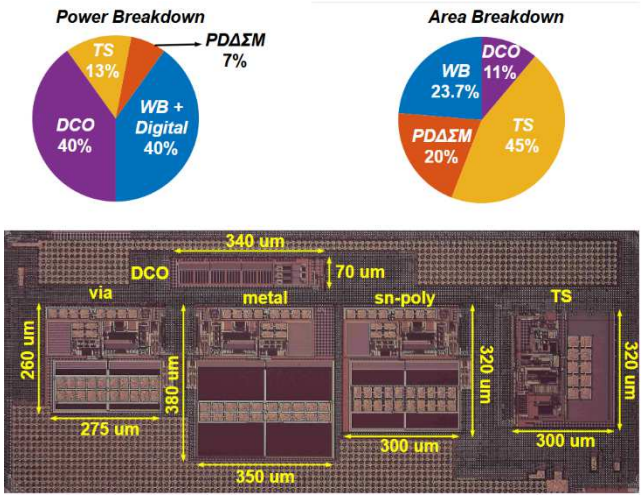

Fig. 10. Power breakdown (top left), area breakdown (top right), and chip micrograph (bottom).

TABLE I. PERFORMANCE SUMMARY AND COMPARISON TO THE PRIOR ART

Specifications	This work	ISSCC 2024 [5]	JSSC 2023 [4]	JSSC 2022 [1]	JSSC 2022 [3]	JSSC 2022 [6]	ISSCC 2021 [2]
Technology	**180 nm**	180 nm	65 nm	180 nm	65 nm	65 nm	180 nm
Main Resistor	**sn-poly**	n-diff	n-poly	p-poly	p-poly	p-poly	p-poly
Compensation device	**BJT**	BJT	via	s-diff	sp-poly	s+n-poly	s-diff
Frequency [Hz]	**16 M**	32 M	100 M	16 M	28 M	32 M	16 M
Freq. Error [ppm]	**±350**	±900	±770	±90	±200	±530	±400
Freq. Error After Aging [ppm]	**±450**	+1600 / −1400	±1030	-	-	-	-
Temp. Coefficient [ppm/°C]*	**4.9**	10.6	12.3	1.3	2.6	8.4	5.2
Trimming points	**2**	2	2	2	2	2	1
Area [mm^2]	**0.22**	0.028	0.22	0.3	0.06	0.18	0.14
Power [μW]	**157**	131	142	220	142	34	158
Temp. Range [°C]	**−45~85**	−40~125	−40~85	−45~85	−40~85	−40~85	−45~85
Supply Range [V]	**1.6~2**	1.7~2	1.1~1.3	1.6~2	0.85~1.05	1.1~2.3	1.6~2
Supply Sensitivity [ppm/V]	**1500**	3000	1400	1200	2900	80**	2000
Jitter [pS]	**21**	18.7	5.1	40	7	22.3	10.2
Allan Deviation Floor [ppm]	**2**	18.8	8.1	0.32	2	2.5	0.35
No. Of Samples	**16**	28	14	20	16	6	18

* Box method.

** On-chip LDO.

IV. CONCLUSION

This paper introduces a 16 MHz RC frequency reference implemented in a 180nm CMOS process, utilizing a digitally assisted frequency-locked loop (FLL). The temperature-dependent phase characteristic of an sn-poly-based WB filter, driven by a DCO, is compensated by an accurate and aging-robust PNP-based TS. The resulting error signal is integrated and used to control the DCO, locking it to the point on the WB filter's phase-frequency characteristic where the phase shift is 0°. The frequency reference achieves ±350 ppm inaccuracy from −45°C to 85°C, which increases to just ±450 ppm after accelerated aging. This represents competitive accuracy and state-of-the-art stability for RC-based frequency references, rivalling that of their LC-based counterparts while dissipating lower power and occupying less area.

REFERENCES

[1] Ç. Gürleyük, S. Pan, and K. A. A. Makinwa, "A 16 MHz CMOS RC Frequency Reference With ±90 ppm Inaccuracy From −45 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2429-2437, Aug. 2022.

[2] H. Jiang, S. Pan, Ç. Gürleyük, and K. A. A. Makinwa, "31.3 A 0.14mm2 16MHz CMOS RC Frequency Reference with a 1-Point Trimmed Inaccuracy of ±400ppm from -45°C to 85°C," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021.

[3] W. Choi, J. Angevare, I. Park, K. A. A. Makinwa, and Y. Chae, "A 0.9-V 28-MHz Highly Digital CMOS Dual-RC Frequency Reference With ±200 ppm Inaccuracy From −40 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2418-2428, Aug. 2022.

[4] K. -S. Park et al., "A Temperature- and Aging-Compensated RC Oscillator With ±1030-ppm Inaccuracy From40 °C to 85 °C After Accelerated Aging for 500 h at 125 °C," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3459-3469, Dec. 2023

[5] S. Pan, Y. Cheng, G. Wu, Z. Wang, K. A. A. Makinwa and H. Wu, "3.2 A 0.028mm² 32MHz RC Frequency Reference in 0.18µm CMOS with ±900ppm Inaccuracy from −40°C to 125°C and ±1600ppm Inaccuracy After Accelerated Aging," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024.

[6] A. Khashaba, J. Zhu, N. Pal, M. G. Ahmed, and P. K. Hanumolu, "A 32-MHz, 34-µW Temperature-Compensated RC Oscillator Using Pulse Density Modulated Resistors," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 5, pp. 1470-1479, May 2022.

[7] S. Pan, X. An, Z. Yu, H. Jiang, and K. A. A. Makinwa, "A Compact 10-MHz RC Frequency Reference With a Versatile Temperature Compensation Scheme," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 12, pp. 3450-3458, Dec. 2023.

[8] A. S. Delke, A. -J. Annema, M. S. O. Alink, Y. Jin, J. Verlinden and B. Nauta, "A Single-Trim Frequency Reference Achieving ±120 ppm Accuracy From −50 °C to 170 °C," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3434-3444, Nov. 2021.

[9] Z. Tang, N. G. Toth, R. Zamparette, T. Nezuka, Y. Furuta and K. A. A. Makinwa, "23.2 A 40A Shunt-Based Current Sensor with ±0.2% Gain Error from −40°C to 125°C and Self-Calibration," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023.

[10] S. M. Kashmiri, S. Xia, and K. A. A. Makinwa, "A Temperature-to-Digital Converter Based on an Optimized Electrothermal Filter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 7, pp. 2026-2035, July 2009.

[11] N. G. Toth, Z. Tang, T. Someya, S. Pan, and K. A. A. Makinwa, "A PNP-Based Temperature Sensor With Continuous-Time Readout and ±0.1 ∘C (3σ) Inaccuracy From -55 ∘C to 125 ∘C," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 2, pp. 593-602, Feb. 2025.