An Ultra-Low Power 8-PSK Receiver with Phase-Frequency Error Cancellation using DSB Modulation

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***Abstract*—This paper presents a 2.4GHz ultra-low power receiver that can receive 8-PSK data. Through a novel circuit architecture and signaling, the receiver is able to perform phase-frequency error cancellation. This allows for relaxed requirements on the local oscillator, helping to reduce power. Through phase-frequency error cancellation, the CFO error is eliminated, phase noise is cancelled, and the impact of frequency drift is removed. This allows support for quadrature phase-based modulation at low power consumption. System considerations are made by utilizing a signal that can be produced with high transmit efficiency, improving overall wireless link power consumption for applications such as wireless sensor networks. The receiver achieves a data rate of 1Mbps at 419µW. The receiver has a normalized sensitivity of -104.5dBm and an energy per bit of 0.419nJ/bit. It is the lowest power GHz receiver that supports quadrature data. It is also the lowest energy per bit GHz receiver below 1mW that can support quadrature data.**

Keywords— ULP, Receiver, PSK, Phase Noise, Frequency Drift, CFO, Wireless Sensor Nodes, Higher Order Modulation, Phase-Frequency Error Cancellation.

I. Introduction

Wireless communication for Internet-of-Things (IoT) is most commonly deployed in the 2.4GHz ISM band where the demand for ultra-low power (ULP) receivers is growing. Often, ULP receivers utilize simple modulation such as OOK or FSK, which limits data rate [10]. This leads to longer time-on-air, resulting in increased wireless congestion and higher system power consumption. Furthermore, applications such as Cellular IoT necessitate the usage of higher order modulation, such as QPSK, to be deployed using existing infrastructure [11]. These concerns emphasize the need for low power receivers that can support higher order modulation and operate with higher data rates.

This work presents a 2.4GHz ULP receiver supporting 8-PSK modulation. The receiver performs phase-frequency error (PFE) cancellation, relaxing performance requirements and thereby reducing power. The receiver consumes 419µW at a data rate of 1Mbps.

II. Phase-Frequency Error Cancellation

The proposed receiver utilizes a modulation supported by a system shown in Fig. 1. An unsuppressed carrier double sideband (DSB-USC) modulation is transmitted. The upper and lower sideband phase data exhibit odd symmetry. Phase and frequency errors will be common to all output terms and exhibit even symmetry.

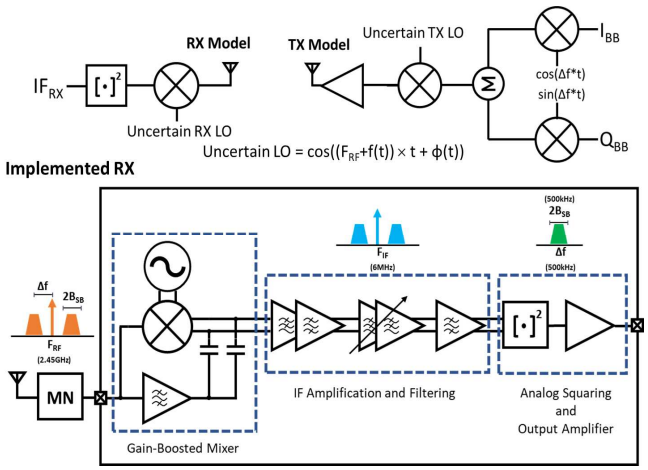

Fig. 1. Conceptual model of wireless link and implemented reciever block diagram with signal evolution

Through a squaring operation, the data can be downconverted and recovered exactly at the sideband spacing (Δf) with the phase-frequency errors cancelled. Examples of such errors include phase noise and frequency drift. These specifications are a function of local oscillator (LO) performance and can be relaxed as a result of PFE cancellation. There is also no center-frequency offset error, removing the need for a phase-locked loop to receive phase-encoded data. The effects of signal nonlinearity (due to either the transmitter or receiver) are suppressed as nearby nonlinear output terms also exhibit PFE cancellation, preventing them from destructively overlapping with the output data.

The output of the squaring operation also produces additional spurious terms. In order to prevent the desired data from overlapping with these spurious terms $3B_{SB} \leq \Delta f$, where B_{SB} is the sideband bandwidth (center-to-null). This limit comes from the self-mixing of the input signal terms that downconvert to DC. If the transmitted signal is

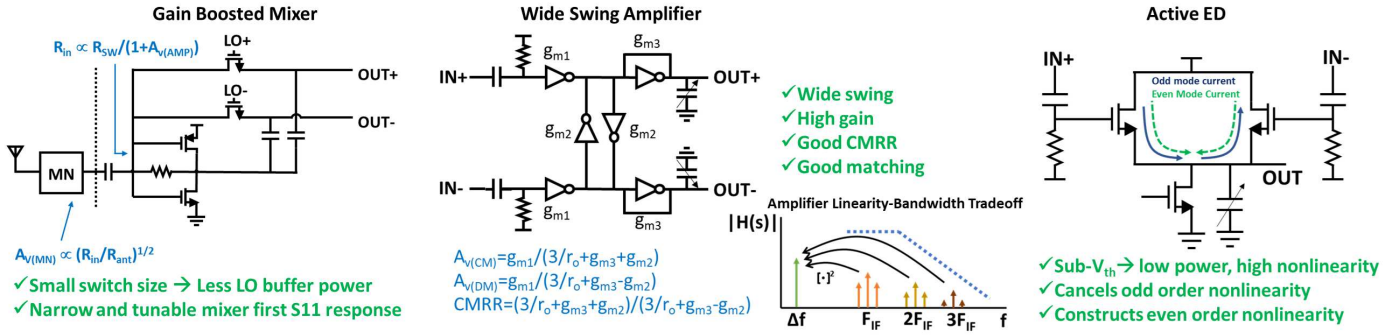

Fig. 2. Circuit diagrams of the gain boosted mixer, wide swing amplifier, and active ED and concept of amplifier linearity versus bandwidth tradeoff

downconverted to a low intermediate frequency (IF) before the squaring operation an additional constraint is present: $\Delta f \leq (2/3)F_{IF} - B_{SB} - 2.05 f_0^{1/2} f * 10^{L(f)/20}$. F_{IF} is the receiver low IF frequency, f_0 is the RF center frequency, L(f) is the total phase noise in dBc/Hz and f is the offset frequency of the measured phase noise. This constraint comes from the fact that the squaring operation will also upconvert the input signal and these outputs will have double the PFE.

The DSB-USC signal not only benefits the receiver through PFE cancellation, but also alleviates requirements on the transmitter. A transmitter model capable of producing a DSB-USC is shown in Fig. 1. Such signaling removes the need for both I and Q paths at RF. PFE induced by the transmitter is also cancelled at the squaring output. As a result, the transmitters efficiency can be improved. This improves the overall efficiency of a wireless sensor network by allowing the entire transmit and receive link to be low power while supporting higher order modulation.

The implemented signal has a symbol rate of 333kHz and a sideband spacing (Δf) of 500kHz. Usage of root raised cosine pulse shaping of the sideband data results in a 250kHz center-to-null sideband bandwidth (B_{SB}). The sideband spacing is chosen to be slightly less than the lower bound for spurious term overlap as a tradeoff with signal bandwidth and spurious-interference, as will be discussed in Section IIID. The signal is downconverted to an IF frequency of 6MHz.

III. Circuit Implementation

The proposed receiver circuit can be seen in Fig. 1. A gain boosted mixer is used to downconvert the signal to a low-IF where additional gain and filtering is performed. Subsequently, an ultra-low power energy-detector (ED) is used to perform the squaring operation.

A. Gain Boosted Mixer

ULP receivers for IoT do not typically require very low noise figures [6-9]. Often, the power of an LNA is limited by matching requirements, e.g., $1/g_m$, rather than noise figure in sub-500μW receivers. Mixer-first based architectures eliminate the LNA power entirely but require switch resistances to be very small in order to perform input matching. This requires large LO buffer power consumption to drive the switches. This work implements a gain-boosted mixer, where a mixer is placed in feedback to an RF amplifier (Fig. 2). The RF amplifier is meant to provide gain that makes the mixer switches appear smaller at the input due to the miller effect. Consequently, a larger switch resistance can be used for input matching, alleviating the drive burden of the LO buffers.

A matching network is utilized to provide passive gain as well as further increase the required switch resistance required for matching. If the loaded-Q of the matching network is much less than the effective-Q of the passive mixer, high-Q mixer-first matching can be performed, benefitting out-of-band interference tolerance. A plot of the S11 can be seen in Fig. 4.

The RF amplifier is implemented through a self-biased inverter amplifier. The mixer switches are sized to be 2.5kOhm and the gain-boosted mixer provides a total gain of 14dB. A common drain amplifier stage succeeds the gain-boosted mixer and is DC coupled to isolate any ac coupled baseband amplifier loading onto the RF stage. The RF amplifier consumes 88.5μW.

B. Local Oscillator

An on-chip current reuse CMOS LC oscillator is used in open loop as an LO. The oscillator is fed into an inverter buffer utilizing a larger VDD to enable stronger driving of the mixer switches. To have control of the buffer output's duty cycle, a passive level shifter is used between the LO and buffer. Enough oscillation swing is achieved as to minimize the short circuit current of the buffer. The duty cycle of the buffers is set to be slightly less than 50% to avoid mixer switching overlap which can lead to input matching issues and conversion gain reduction. The phase noise of the oscillator is -110dBc/Hz at 1MHz offset. The local oscillator consumes 140μW and the buffers consume a total of only 37.5μW due thanks to the gain boosted mixer. This is a significant power savings compared to traditional passive mixer-first receivers, where the buffer power is closer to the power of the LO.

C. Baseband Amplification and Squaring

Downconversion is being performed in this receiver to improve filtering quality factor and allow gain to be provided

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with low power. This helps improve receiver sensitivity and interference tolerance. ED's are wideband and their conversion gain is a function of input amplitude. Therefore, providing enough gain before the ED and sufficient filtering will enhance the performance significantly. Fully differential programmable gain amplifiers are utilized for gain control. Their gain can be varied a total of 32dB. Pseudo-differential Nauta transconductors [5], as seen in Fig. 2, are used to provide high gain and wide swing amplification with less than 0dB of common mode gain. The pseudo-differential structure allows for wide swing by only having a maximum of two devices stacked between VDD and GND. Cross coupling between the pseudo-differential paths is used to set the common mode and differential mode gains, allowing improved CMRR performance compared to single ended paths, while exhibiting comparable headroom and improved gain performance.

Wide swing is necessary to provide enough headroom for a large signal necessary at the ED input, whose conversion gain is a function of input amplitude. Depicted in Fig. 2, an active differential input common drain ED [12] is operated in subthreshold to enhance its 2nd order nonlinearity conversion gain. The output is taken at its differential "virtual ground", which cancels odd order currents and constructs even order currents. The ED consumes only 3.6µW. A measured constellation before and after squaring can be seen in Fig. 3. This demonstrates how the double sideband PSK signal with PFE (left), when passed through the ED, cancels the PFE- to result is a clean PSK constellation (right).

D. Performance Tradeoffs

A tradeoff exists between filter bandwidth and amplifier linearity with respect to output SNR. Due to the need for large swing before the ED, the likelihood of the signal compressing from amplification and producing nonlinear components increases. These nonlinear components, when squared, will also produce the desired signal at the ED output (adding constructively). Therefore, the nonlinear components do not corrupt the output signal. In fact, they help to improve output SNR. However, before the ED, even order nonlinear components will be located at multiples of the IF frequency, which may fall outside of the filter bandwidth. The filtering of these components will result in reduced conversion gain of these components at the output. Therefore, in the face of high non-linear amplification a widened bandwidth can improve output SNR the most, but requires a significant increase in power consumption.

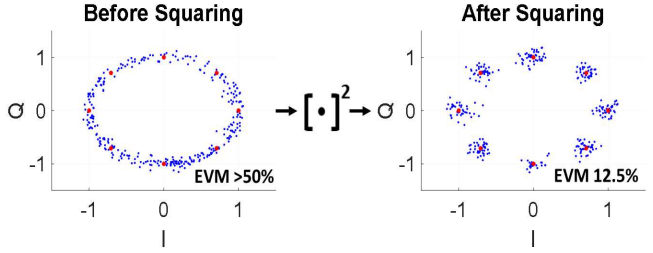

Fig. 3. Measured 8-PSK constellation before and after squaring showing phase-frequency error cancellation

An IF frequency of 6MHz is chosen to avoid flicker noise, push away any upconversion spurious terms after squaring, and increase receiver tolerance to frequency drift. An IF bandwidth of 11MHz is selected as a balance between interference tolerance and sensitivity. A sideband spacing of 500kHz is selected to reduce the signal bandwidth, which results in less SNR reduction compared to marginal overlap with the direct conversion spurious term. This is because, near sensitivity, the direct conversion spurious term is below the noise floor. A plot of relative EVM vs packet frequency drift can be seen in Fig. 4, measured 2dB above sensitivity. Packet drift of less than ±2MHz results in less than 0.5dB of EVM error. This reduces the effect of sensitivity degradation due to the potential of frequency drift between the receiver and transmitter, alleviating the need or eliminating entirely the usage of an FLL or PLL. Low side drift EVM is limited by flicker noise and high side drift EVM is limited by nonlinear signal filtering.

IV. Measurement Results

The receiver was fabricated in 65nm CMOS. The transmitted signal power is composed of double sideband data that is 6dB below the carrier power. The sidebands contain PRBS 8-PSK data. The symbol rate of the data is 333kHz. The transmitted baseband data is pulse shaped with a root raised cosine filter of span 16 and roll off factor of 0.5, resulting in a sideband null-to-null bandwidth of around 500kHz. The sideband spacing is selected to be 500kHz. The receiver output is captured on a Tektronix MDO4024C oscilloscope and demodulated using MATLAB communication toolbox. Fig. 4 shows the measured S11,

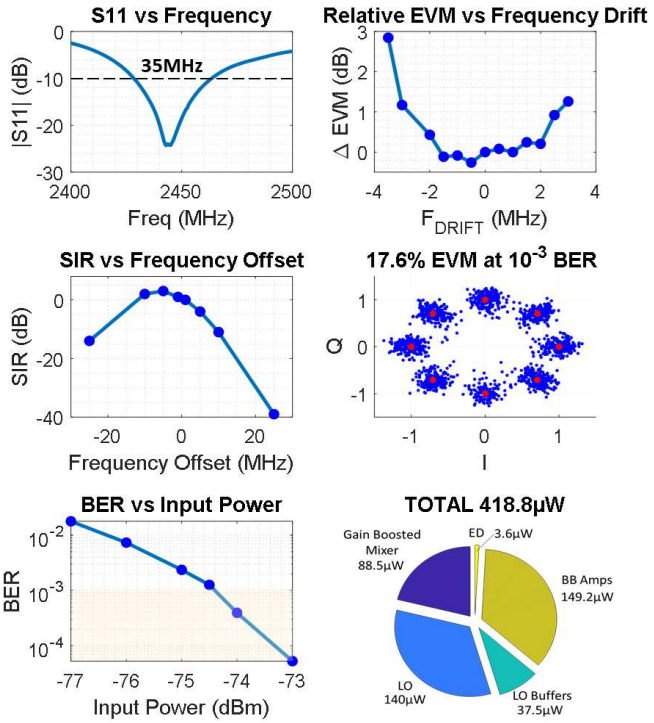

Fig. 4. Measured S11, relative EVM vs frequency drift, sensitivity, EVM at sensitivity, SIR vs frequency offset, and power breakdown

TABLE I. COMPARISON WITH STATE-OF-THE-ART

	This Work	[1]	[2]	[3]	[4]
Technology (nm)	65	65	22	65	65
Frequency (MHz)	2400	950	950	2400	915
Modulation	DSB-USC 8-PSK	QPSK with Pilot Tone	Two-Tone SS-BPSK	CE-OOK	Transmitted Reference SS-BPSK
Power (µW)	419	612	149 (excludes LO power)	20.9[5]	150
Data Rate (kbps)	1000	208	100	0.819	10
Energy per bit (nJ/bit)	0.419	2.94	N/A (excludes LO power)	25.5	15
Sensitivity (dBm)	-74.5[3]	-80[3]	-83	-91.5[6]	-70
Normalized Sensitivity (dBm)[1]	-104.5	-103	-103	-91	-87
CW SIR (dB)[2]	-4/-39 @5/25MHz	-7/-40 @3/25MHz	-18/43 @2/25MHz[4]	-22/-47 @5/20MHz	-26/-27 @1/5MHz[4]
Active Area (mm^2)	0.33	0.62	0.5	2.24	0.6

[1]Normalized Sensitivity=Sensitivity[dBm]-10log(Data Rate[kbps]) [2]3dB desensitization. Best reported for all
[3]Demodulated using MATLAB communication toolbox [4]uses spreading code [5]10ms latency [6]MDR=10^{-3}

sensitivity, signal-to-interference ratio (SIR), EVM, frequency drift tolerance, and power breakdown. A spreading code (not implemented in this work) can be added to the signal, as done in [2] and [4], to further improve SIR.

The receiver consumes 419µW at a data rate of 1Mbps, achieving an energy per bit of 0.419nJ/bit. An SIR of -4dB/-39dB at +5MHz/+25MHz offset is measured. It has a sensitivity of -74.5dBm at a bit error rate of 0.1%. At sensitivity, the 8-PSK constellation has an EVM of 17.6%. A die photo can be seen in Fig. 5. A comparison to state-of-the-art is shown in Table 1. This work achieves the highest data rate, lowest energy per bit, and lowest normalized sensitivity. It is the lowest power GHz receiver that supports quadrature modulated data. It is also the lowest energy per bit GHz receiver below 1mW that can support quadrature data.

V. CONCLUSION

This work presents a novel receiver architecture and signaling that is able to perform PFE cancellation. This loosens requirements on the receiver performance, which helps to reduce power consumption. The receiver uses a gain boosted mixer to help reduce overall RF domain power consumption. Wide swing amplification is employed to improve the conversion gain of a near-zero power ED, which enables PFE cancellation at lower input powers. A data rate of 1Mbps is achieved helping to reduce time-on-air and hence reduce spectral congestion. It is the lowest power GHz receiver that supports quadrature data. It is also the lowest energy per bit GHz receiver below 1mW that can support quadrature data.

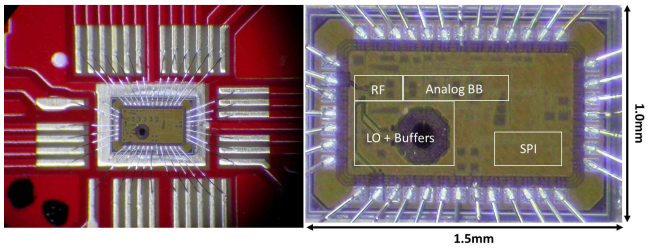

Fig. 5. Die Micrograph

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