Analysis of Substrate Impact on SP3T Switch in Phase-Change Material Technology

L. Nyssens[#], B. Reig[#], J. Lugo[#], V. Puyal[#], C. Héllion[#], M. Allain[#], J. Denizart[#], S. Monfray[$], A. Fleury[$]
[#]CEA-Leti, Université Grenoble Alpes, F-38000 Grenoble, France
[$]STMicroelectronics, Crolles, France
{lucas.nyssens, bruno.reig, jose.lugo}@cea.fr

***Abstract*— This paper investigates the impact of Si substrate characteristics on the performance of phase-change material (PCM) RF switches, specifically focusing on a single-pole, three-throw (SP3T) switch. A SP3T is fabricated on top of a high-resistivity (HR) and a trap-rich (TR) substrate. Moving from a HR to a TR substrate, the switch IL and linearity improves by 0.2 and ~20 dB, respectively, thanks to the higher RF quality substrate. The SP3T switch achieves an IL and isolation of 0.7 and 32 dB at 10 GHz, respectively, handling up to 25.6 dBm of input power, with harmonic levels as low as -71 dBm (at P_{in} = 20 dBm). A thorough analysis identifies the substrate as main contributor to the switch non-linearities on the HR substrate, while the SP3T switch harmonics are dominated by the PCM switch when lying on top of a TR substrate.**

Keywords—PCM, GeTe, phase-change RF switch, SPNT, linearity, SOI, trap-rich substrate, high-resistivity substrate.

I. Introduction

The evolution of communication standards has significantly increased the complexity of front-end modules (FEMs), including RF switches. These switches must now meet stringent requirements, including reduced insertion loss (primarily characterized by the $R_{on}xC_{off}$ metric), improved power handling, enhanced linearity, driving the need for continuous technological advancements. Silicon-on-Insulator (SOI) CMOS technology offers a high-volume, high-performance platform for RF applications, and currently dominates the RF switch market [1]. Nevertheless, phase-change material (PCM) RF switches are gaining attention due to their exceptional $R_{on}xC_{off}$ figure of merit (FoM), advantageous for sub-6 GHz and millimeter-wave applications, and their integration compatibility in a CMOS back-end of line (BEOL). Typically made from germanium telluride (GeTe), these switches rely on a heating mechanism to switch between two stable, non-volatile states: a crystalline (low-resistance) state and an amorphous (high-resistance) state.

Recent developments have demonstrated impressive $R_{on}xC_{off}$ values of around 10 fs [2]-[3] for PCM switches integrated into the BEOL of commercial (Bi)CMOS processes. Single-pole, double-throw (SPDT) [2] and high throw-count switches (SPNT, N > 2) [4] have already exhibited superior insertion loss (IL) performance up to 100 GHz when compared to SOI CMOS and micro-electromechanical system (MEMS) technologies. However, for PCM technology to become a serious contender to SOI CMOS switches, it must overcome two major challenges: limited power handling capability and cycling endurance (reliability) [1]. These issues require further technological development to make PCM a viable alternative.

This paper proposes a novel analysis of how the substrate influences the FoMs of PCM RF switches, specifically applied to the case of a SP3T switch. In (SOI) CMOS technology, it is well-established that the silicon (Si) substrate can significantly impact the performance of overlying circuitry, particularly in RF applications [5]. RF switches are among the most sensitive circuits to substrate characteristics.

High-resistivity (HR) substrates reduce conduction losses compared to standard resistivity substrates, leading to improvements in insertion loss and linearity. However, HR substrates suffer from parasitic surface conduction (PSC), which creates a thin, highly conductive layer near the Si-oxide interface. This layer can partially counteract the IL and linearity improvements. Trap-rich (TR) high-resistivity substrates address this issue by introducing a layer rich in traps that effectively pin the Fermi level in the mid-gap near the Si-oxide interface, resulting in a highly linear and virtually lossless substrate [5]. The deployment of TR substrates in RF SOI CMOS technology has played a crucial role in today's success of RF SOI technology [5].

This paper analyzes a SP3T switch in PCM technology on HR and TR substrates. Section II introduces the technology. Section III details the SP3T model, including PCM switches and EM interconnects simulations. Section IV presents and discusses the measurement results.

II. PCM Technology

The whole fabrication process closely follows the one described in [6], a simplified cross-section of the whole stack is provided in Fig. 1. The fabrication process is based on the integration of GeTe within the BEOL of a CMOS-compatible 200 mm flow. The process starts with a thermal oxidation of a HR Si wafer or an SiO_2 deposition on a TR Si wafer. A first AlCu metallic layer (M1) is deposited, etched and filled with silica. Next, the 100 nm-thick 0.5-0.5 GeTe is deposited and backside contacted to the underlying metal. A 100 nm-thick PVD AlN layer is then deposited over the PCM as a dielectric layer, followed by a silica deposition and planarization. Heaters above the PCM are then formed, using tungsten (W) connected to the first metallic layer. Finally, vias and the 1 µm-thick second metallic layer (M2) are formed.

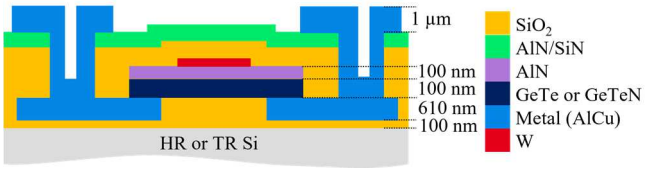

Fig. 1. Simplified cross-section of the fabricated BEOL stack with PCM.

III. SP3T Switch Model

A. SP3T Switch Design

This SP3T design consists of a simplified SP3T series-only topology where two of the throws' ports have been shorted instead of loaded with a 50 Ω impedance. The

simplified SP3T schematic is shown in Fig. 2(a). This simplification eases the design and measurement of the switch by avoiding the need for accurate and high-power on-chip 50 Ω loads or measurements with more than 2 RF ports. However, the simplification applies only when SW1 is ON, SW2 and SW3 are OFF, enabling the meaningful characterization of the SP3T IL FoM up to moderate frequency values. The switch's isolation metric is evaluated in this paper solely based on simulations thanks to the great simulation-measurement agreement achieved as shown below.

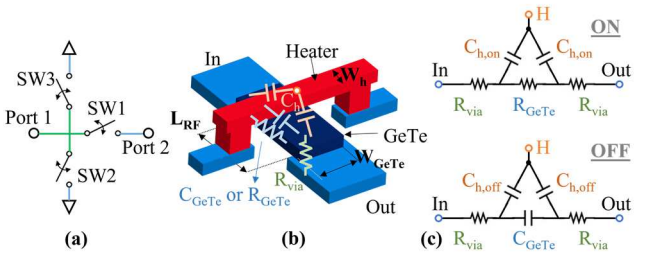

Fig. 2. (a) Designed SP3T switch in simplified configuration. (b) core PCM switch 3D view. (c) lumped-element model of the core PCM switch in ON and OFF states (top and bottom, respectively). Dimensions are: W_h = 1 µm, L_{RF} = 1 µm, W_{GeTe} = 30 µm. Lumped element values are: C_{GeTe} = 2.52 fF, $C_{h,off}$ = 9.3 fF, $C_{h,on}$ = 13.3 fF, R_{GeTe} = 2.83 Ω, R_{via} = 0.21 Ω.

The SP3T switch design consists of 3 identical core PCM switches routed to the 2 RF ports and ground via short pieces of CPW lines in stacked M1-M2 signal and ground tracks. The signal track width is 25.25 µm, spacing to ground: 10.25 µm, total metal thickness: 2.26 µm, lengths: 120 (port 1 – to switches, green in Fig. 2(a)) or 60 µm (all other connections, blue in Fig. 2(a)). The core PCM switch is shown in Fig. 2(b). It is made of 1 µm-long (L_{RF}), 30 µm-wide (W_{GeTe}) GeTe material connected to M1 with vias on each side. They are indirectly commuted from ON (crystalline GeTe) to OFF (amorphous GeTe) states, and vice versa, thanks to a 1 µm-wide (W_h) heater in W. The heaters are connected to dc pads via M1 lines that cross below the RF ground, capacitively coupling the heaters to the RF ground.

B. Core PCM Switch Modeling

The same core PCM switch is also fabricated as standalone structures both in a series and in a shunt configuration. The measurements of these structures enable the extraction of the lumped-element model of the core PCM switch shown in Fig. 2(c), where C_{GeTe}, $C_{h,on}$, $C_{h,off}$, R_{GeTe}, R_{via} expressions are partially given in [6]. Detailed extraction of these values based on the measurements of switches of various geometries is out of scope of this paper. The extracted values are provided in the caption of Fig. 2. The extracted amorphization ratio (δ_{amo}, extracted from power handling measurements in OFF state [7]) -defined as the ratio of amorphous GeTe over L_{RF}- is around 40%.

The measured $R_{on}xC_{off}$ product figure of merit of these switches is around 35 fs, extracting with the method described in [6], from which the resistance accesses have been de-embedded (thus $R_{on} = R_{via} + R_{GeTe}$), but not the capacitance parasitics (thus $C_{off} \gg C_{GeTe}$).

C. SP3T Switch Modeling

The overall SP3T switch model consists of a partitioning between electromagnetic (EM, with Keysight Momentum) simulations of the layout including the RF pads and interconnects, and three instances of the core PCM switch model from Fig. 2(c) in either ON or OFF state. It is interesting to note that the EM simulation includes a port for each heater node from the core switches (see 'H' in Fig. 2(c)), such that the capacitive coupling between the heater and the RF ground pads is accurately taken into account. No additional tuning element has been added to the simulations.

The EM simulation of the TR Si wafer is performed on a substrate stack similar to what is described in Fig. 1, with a single 6 kΩcm-resistive 700 µm-thick Si layer. However, the HR wafer without interface passivation suffers from the PSC effect due to the presence of fixed charges that are trapped in the oxide above the Si interface. These trapped charges induce a thin sheet of highly conductive free carriers in the substrate. Its effect on RF losses and linearity is hardly accurately predicted, because a slight variation in the amount of fixed charges (generated during manufacturing) induces a large variation (with exponential relationship) in the conductivity of the thin sheet.

The EM substrate stack is modified to model this effect, by introducing a 1 µm-thick *low resistivity* Si layer between the oxide and the thick 6 kΩcm Si layer. Coplanar waveguide (CPW) lines of different lengths (and the same cross-section as the SP3T access, cfr. Section III.A and Fig. 3(c)) are measured and their equivalent per-unit-length RLGC parameters are extracted based on the Thru-Reflect-Line (TRL) method. Similarly, EM simulations of the same lines are performed, and the resistivity of the thin Si layer is tuned to fit the measurements. The whole fitting procedure closely follows the method explained in [8]. The RLGC parameters and propagation loss (α) of the measured and simulated lines are shown in Fig. 3.

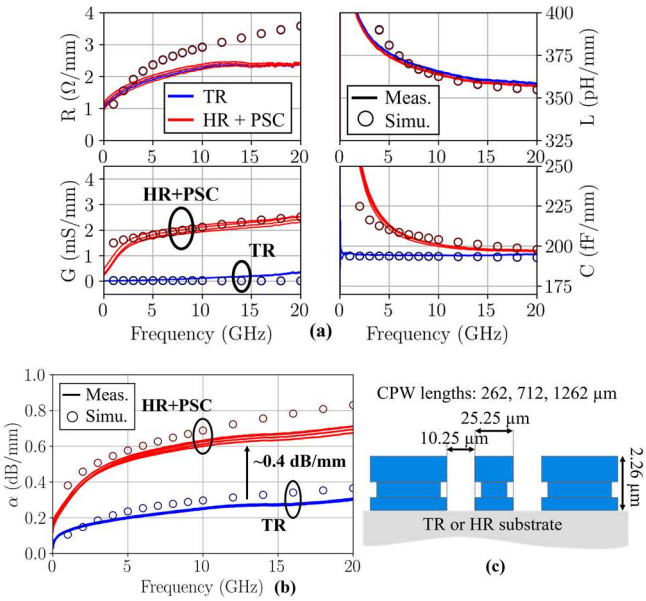

Fig. 3. Per-unit-length RLGC parameters (a) and propagation loss (α, b) of measured (solid lines) and simulated (circles) CPW lines (cross-section in c) for the TR (blue) and the HR substrate with PSC effect (red). The R and L terms are substrate-independent, hence the overlapping and indistinguishable red and blue curves.

Several dies across the wafers are measured. Very little variation is observed for the TR, which could be attributed to probe contact repeatability at first order, whereas significant die-to-die variation is present for the HR substrate, mostly in the substrate-loss term (G) that is also visible in α. Substrate

losses are very small on the TR substrate, so that metallic losses dominate in α. Since the metal lines are the same on both substrates, the ~0.4 dB/mm difference in α from TR to HR entirely comes from additional substrate losses.

A good agreement in EM simulations and measurements is overall achieved. The small discrepancy in α at higher frequencies comes from the approximate fitting of the metallic-loss term (R), which can be improved by tuning the metals' conductivity. The good fitting in C and G (related to the substrate) for the HR wafer is obtained with a 1 µm-thick Si layer of 9 Ωcm resistivity. Although a more complex multi-layer stack modeling might give more accurate results (mostly at lower frequencies), this 2-layer stack is accurate enough for our study as it will be shown in the following.

IV. SP3T Switch Measurements

A. Measurement Setups

Three different setups have been used to perform all the measurements.

i) First, electrical commutation is necessary to turn the switches OFF and ON when appropriate. High speed pulses are applied between the heater electrodes with a 50 Ω-matched HP 8114A pulse generator. The GeTe resistance is measured with a source measurement unit (SMU) by applying 10 mV on the GeTe electrodes. Amorphous GeTe (OFF state) is achieved by applying 800 ns-long pulses (with 10 ns rise and fall times) of 8.6 V. Switches are reset by applying 4.2 V, 2 µs-long pulses. Due to the non-volatility of the PCM switch, the switches are all initially programmed, and hold their state in the following measurements.

ii) S-parameters are measured with a Keysight PNAX, on-wafer with FormFactor Infinity XT67 50 µm-pitch Ground-Signal-Ground (GSG) probes. Line-Reflect-Reflect-Match (LRRM) calibration is performed beforehand on a standard impedance substrate (ISS).

iii) Finally, on-wafer large-signal and power handling measurements are performed with the same setup as the one described in [6]. The input power (P_{in}) is swept from -10 dBm to 37 dBm, with a fundamental frequency (f_0) of 915 MHz, while the fundamental, first and second harmonics (H_1, H_2, H_3, respectively) are measured from the output power (P_{out}). The GeTe dc resistance is monitored in parallel for each power level with a SMU applying 10 mV.

B. RF small-signal performance

As mentioned above, this SP3T design is only meaningful for the state in which SW1 is ON, and SW2 and SW3 are OFF, e.g. for the IL evaluation as shown in Fig. 4(a) and (b). Let us define it as 'State1', illustrated in the inset of Fig. 4(a). For completeness, the other two possible states are also measured, simulated and shown in Fig. 4(c) and (d) and their insets.

Overall, we observe an excellent agreement between measurements and simulations for all the different states. It strengthens the confidence in the isolation metric evaluation via simulations shown in Fig. 4(e).

The switch IL is reduced by ~0.2 dB thanks to the TR substrate with respect to the HR substrate, featuring at best an IL below 0.7 dB up to 10 GHz. The overall increase in losses is well reproduced by simulations and is directly related to additional losses in the CPW accesses dissipated in the substrate. The substrate impact on matching is negligible and the switches are well matched up to 13 GHz on both substrates. Isolation reaches 32 dB at 10 GHz for both substrates, as it depends on the C_{off} capacitance of the core switch and little on the access losses, thus substrate resistivity.

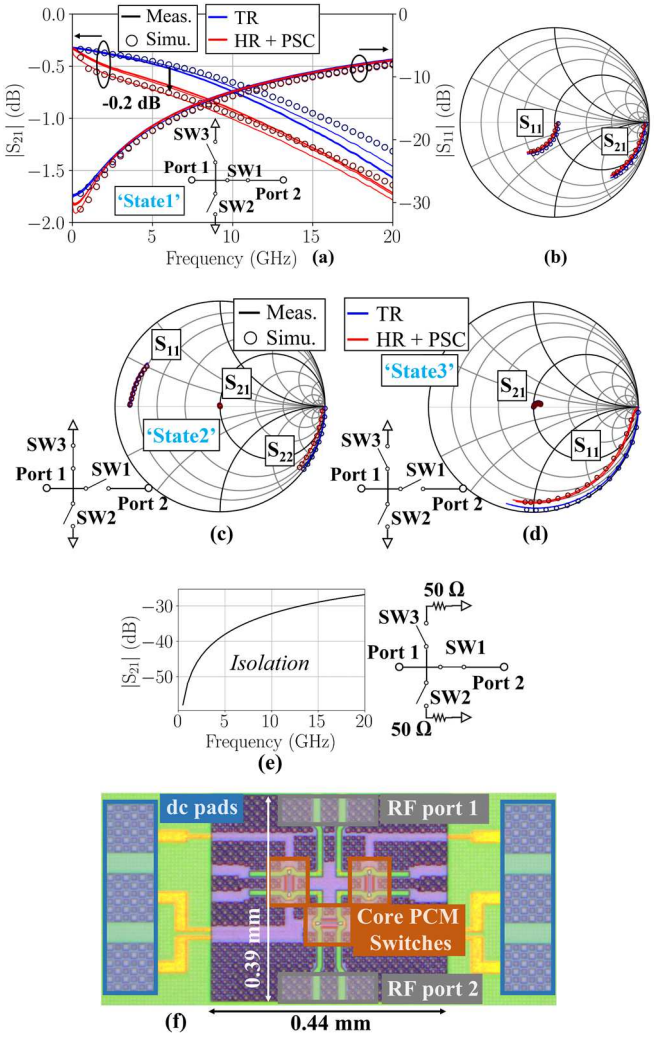

Fig. 4. S-parameters of the SP3T circuit in different configuration states: 'State1' (a, b), 'State2' (c), 'State3' (d), whose schematic is shown in the inset. Measurements (solid lines) and simulations (circles), magnitude versus frequency (a), Smith chart (b-d) of the SP3T on a TR (blue) and a HR (red) substrate. (e) simulated SP3T isolation and circuit used in simulation. (f) microphotography of fabricated SP3T circuit.

It should be noted that the 0.7 dB of IL at 10 GHz can be improved up to 0.5 dB with some matching circuit, e.g. a 250 pH series inductor, without modifying the isolation metric.

C. RF large-signal performance

RF large-signal measurements of the SP3T switch are shown in Fig. 5, only for 'State1', the meaningful state in this SP3T design. The circuit ceases normal operation for P_{in} ~ 18-26 dBm (only one die on each substrate is shown here for readability). At this power level, one or both of the two shunt OFF switches turn ON (crystallization). The port 1-to-port 2 dc resistance (R_{12}) is monitored simultaneously, and a decrease in resistance is observed for the same power level, i.e. the shunt switch R_{on} sees in parallel the R_{on} of the series SW1 in dc. Next, the shunt switches break (open circuit) around 28 dBm inducing an increase in H_1/P_{in} gain and dc resistance, until finally the series switch breaks at ~31 dBm.

These results agree well with standalone core switch measurements provided in Fig. 6.

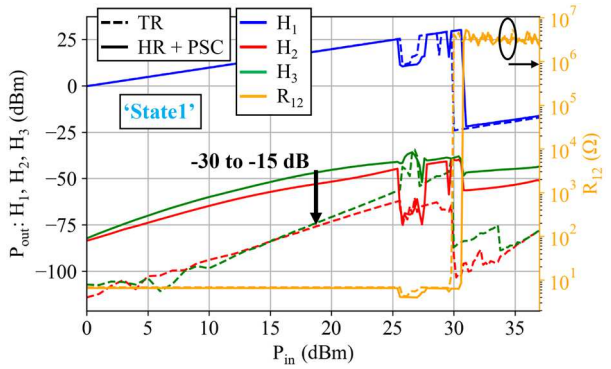

Fig. 5. RF large-signal measurements of SP3T switch on a TR (dashed lines) and a HR (solid lines) substrate, configured in 'State1' (see inset of Fig. 4(a)). P_{out} on the left axis, dc R_{12} on the right axis (orange).

A substantial 15-30 dB reduction (according to P_{in}) in non-linearities (maximum of H_2 and H_3) is observed on the SP3T on top of the TR substrate compared with the HR substrate. A better insight of the origin of non-linearities in the SP3T can be achieved by analyzing the large-signal measurements of the same switch in standalone series and shunt configurations. Fig. 6 shows such measurements as well as Thru structure measurements on both substrates. Shunt switch measurements are repeated in Fig. 6(a) and (b) for better readability.

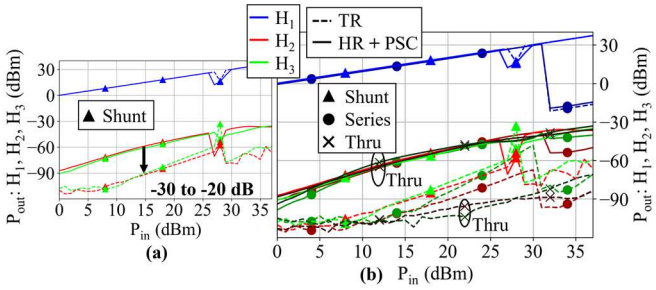

Fig. 6. RF large-signal measurements of standalone core switch. Shunt (a, '^') and series (b, 'o', equivalent to SPST) configurations, on TR (dashed lines) and HR (solid lines) substrates. Measurements of Thru structure ('x') on both substrates are also present in (b). Shunt switch measurements ('^') are repeated in (b) for better readability.

We observe for the HR substrate (solid lines) that the switch non-linearities are dominated by the substrate (similar level as the Thru structure). However, for the TR substrate, the substrate-generated harmonics are much lower, and the switch harmonics are dominated by the PCM device itself in both configurations. Furthermore, on the TR substrate, the non-linearities of the shunt configuration are overall stronger than those of the series configuration. Therefore, the non-linearities from the shunt branches likely dominate the overall SP3T non-linearity behavior (in normal operation, i.e. before breakdown) shown in Fig. 5.

A way to further improve the linearity (and power handling) performance is via compensated stacking, as demonstrated in [9]. However, as in CMOS technology, stacking several devices has the downside of decreasing the operation frequency due to the introduction of additional parasitics (including the compensation capacitances in PCM). Nevertheless, the demonstrated superior performance of PCM switches at higher frequencies compared to CMOS suggests a promising future for highly linear, high-frequency switches based on PCM technology.

V. Conclusion

A SP3T switch in PCM RF switch technology is presented in this paper. Two versions of the switch are fabricated (i) on a HR substrate suffering from PSC effect and (ii) on a TR substrate. Detailed models are given for each switch that agree very well with small-signal measurements. RF S-parameters and large-signal measurements are presented. Moving from a HR to a TR substrate, the switch IL and linearity improves by 0.2 and ~20 dB, respectively. The < 10 GHz SP3T switch achieves an IL and isolation of 0.7 and 32 dB at 10 GHz, respectively, handling up to 25.6 dBm of input power, with harmonic levels as low as -71 dBm (at P_{in} = 20 dBm). A thorough analysis of large-signal behavior identifies the substrate as main contributor to the switch non-linearities on the HR substrate, while the SP3T switch harmonics are dominated by the PCM switch when lying on top of a TR substrate. This is the first analysis of the substrate impact on PCM RF switch performance, to the best of the authors' knowledge.

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