Direct 48-V/1-V 5A Low-Frequency DSD Converter with Bidirectional Recycle Converter for AC-Ripple Cancellation and Transient Enhancement

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***Abstract*— This paper presents a low-frequency double step-down (LF-DSD) converter integrated with a GaN-based high-frequency bidirectional recycle (GHBR) converter, offering a substantial on-time (T_{ON}) of 400 ns. The proposed design effectively suppresses output voltage ripple to 6 mV—an 11× reduction—while leveraging high switching frequency and inductor slew rate to deliver outstanding transient performance. For a load step from 1 A to 5 A, the measured undershoot is 69 mV with a recovery time of 907 ns. Conversely, for a step-down from 5 A to 1 A, the overshoot is 74 mV with a recovery time of 848 ns, achieving a transient performance of 8.2 mV/A. The peak efficiency reaches 96.51%.**

***Keywords*—AC-ripple cancellation, DSD converter, high conversion ratio, recycle converter**

I. Introduction

With the rapid advancement of artificial intelligence and the exponential growth of big data analytics, modern electronic systems are becoming both smarter and more power-hungry. In high power-density applications—such as servers and routers in data centers, as well as ECUs and sensors in automotive systems—the 48V-to-1V converter has emerged as a compelling solution, drawing considerable research interest. However, achieving efficient and responsive 48V-to-1V conversion presents several challenges.

One major challenge lies in the extremely short on-time (T_{ON}) required for such a low voltage conversion ratio, which complicates high-side switch operation. For example, error-based controlled buck converters [1] attempt to improve transient performance by integrating a parallel linear regulator to enable fast current injection or extraction during load transients. While this approach reduces recovery time (T_R), it suffers from two major drawbacks in 48V-to-1V applications: the ultra-short T_{ON} (~10 ns at f_{sw} = 2 MHz), and the inherently low efficiency of linear regulators that rely on high-voltage MOSFETs.

To address voltage stress and extend T_{ON}, hybrid converter topologies have been proposed [2]–[5]. These designs reduce stress on power switches and allow longer conduction times. For instance, the quadruple step-down (QSD) converter [4] and the capacitor-assisted dual-inductor (CADI) converter [5], shown in Fig. 1, extend T_{ON} by factors of 4× and 5×, respectively, and reduce voltage stress on switches by similar margins. However, both converters face the same limitation: a reduced inductor current slew rate (SR) during load transients, resulting in prolonged recovery times—particularly in heavy-to-light transitions. To enhance transient response, increasing the switching frequency (f_{sw}) is a common approach. However, doing so further shortens T_{ON} (e.g., to 40–50 ns at f_{sw} = 2 MHz), which exacerbates switching losses and severely degrades light-load efficiency, as illustrated in Fig. 2. Alternatively, lowering f_{sw} can increase T_{ON} and improve light-load efficiency by giving the high-side switch more conduction time. Yet, this comes at the cost of degraded transient performance, as it leads to higher output voltage ripple (ΔV_{OUT}) and longer T_R.

For example, Fig. 3 demonstrates that in a double step-down (DSD) converter with a 3 µH inductor, C_O = 30 µF, and f_{sw} = 100 kHz, a 4 A load step over 50 ns results in a ΔV_{OUT} of approximately 127 mV and a recovery time of around 100 µs. These results highlight the fundamental trade-off in low-frequency operation: while efficiency improves, the transient response suffers. Addressing this trade-off remains a key focus for next-generation power converter designs.

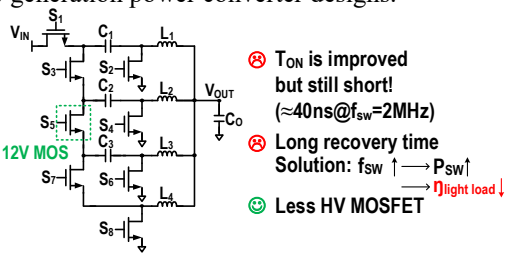

Fig. 1. QSD suffers from short T_{ON} and long recovery time [4].

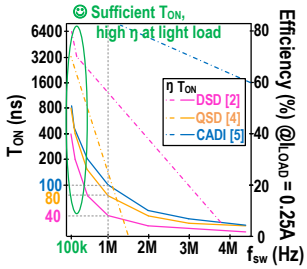

Fig. 2. Comparison of prior arts' T_{ON} and light efficiency.

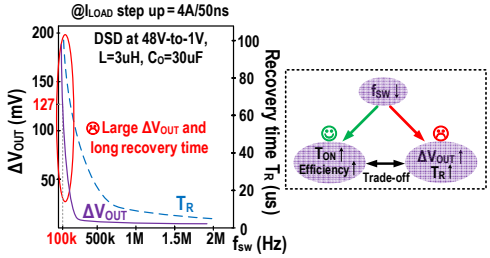

Fig. 3. ΔV_{OUT} & T_R vs. f_{sw} of DSD.

To overcome the aforementioned challenges and simultaneously achieve fast transient response and high efficiency, this paper proposes a hybrid architecture that combines a low-frequency double step-down (LF-DSD) converter with a GHBR converter, as illustrated in Fig. 4. In high-power operating conditions, the LF-DSD converter ensures high efficiency, while the GHBR converter delivers rapid transient response. Additionally, the GHBR converter effectively suppresses the large ΔV_{OUT} typically introduced by

the low switching frequency of the LF-DSD converter. A key advantage of the proposed architecture is that the GHBR converter operates at a low $V_{recycle}$ voltage, allowing the use of low-voltage GaN FETs. This significantly reduces switching losses, thereby further enhancing overall efficiency and response speed. The rest of this paper is organized as follows: Section II presents the proposed LF-DSD and GHBR converter architecture. Section III details the circuit implementation. Section IV provides experimental results that validate the proposed approach. Finally, Section V concludes the paper.

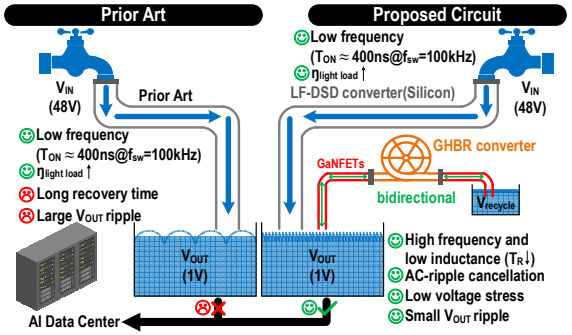

Fig. 4. Comparison of prior art architecture and the proposed architecture.

II. Proposed LF-DSD Converter with GHBR Converter

The architecture shown in Fig. 5 integrates an LF-DSD converter for regulating $V_{recycle}$ and a GHBR converter with a small inductor to achieve high inductor current slew rate, effectively minimizing overshoot, undershoot, and recovery time (T_R) during load transients. The LF-DSD converter delivers the primary current during steady-state operation and regulates a lower intermediate voltage, $V_{recycle}$, rather than V_{OUT}. This allows it to operate at a low switching frequency (f_{sw} = 100 kHz) with a long on-time (~400 ns), optimizing efficiency under light-load conditions.

In contrast, the GHBR converter directly regulates V_{OUT} and responds quickly to transients. It delivers fast source current during load steps and recycles excess energy from V_{OUT}, further improving power efficiency. During high-power conditions, the LF-DSD converter maintains high steady-state efficiency, while the GHBR converter ensures fast transient response and suppresses large ΔV_{OUT} induced by the LF-DSD converter's low switching frequency.

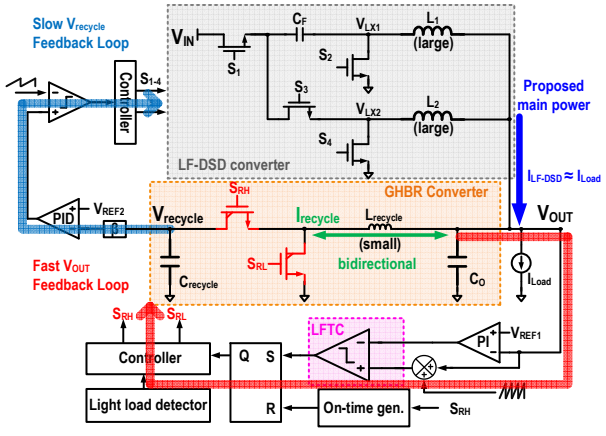

Fig. 5. Architecture of proposed LF-DSD converter with GHBR converter.

The proposed constant on-time control scheme incorporates a low false-trigger comparator (LFTC) to prevent erroneous on-time activation, while a light load detector (LLD) disables the GHBR converter under light-load conditions to enhance efficiency. Fig. 6 illustrates the GHBR converter's steady-state operation. In phase $\Phi 1$, the inductor current ($I_{recycle}$) flows from the output capacitor (C_O) into $C_{recycle}$, and in phase Φ_2, it returns. During phases Φ_3 and Φ_4, $I_{recycle}$ alternates bidirectionally between C_O and $C_{recycle}$. As a result, the average inductor current ($I_{recycle\_DC}$) remains approximately zero.

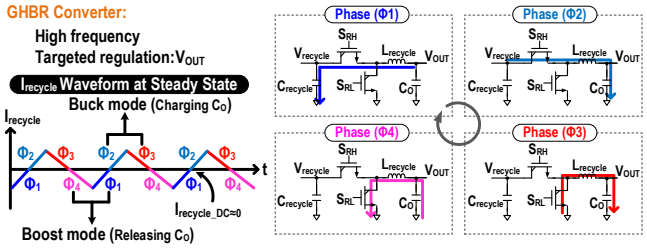

Fig. 6. The operation principle and waveforms of GHBR converter.

Fig. 7 illustrates the AC ripple cancellation mechanism. With the addition of the GHBR converter, its high-frequency operation inherently counteracts the large $\Delta I_{LF\text{-}DSD}$ generated by the LF-DSD stage. The GHBR converter produces compensating charge pulses ($+Q_{re}$ and $-Q_{re}$) that directly oppose the inductor current ripple of the LF-DSD stage ($-Q_{LF\text{-}DSD}$ and $+Q_{LF\text{-}DSD}$), effectively reducing the total ripple current ($\Delta I_{L,total}$). This results in a more stable output voltage with significantly lower ripple, improving both system performance and overall efficiency.

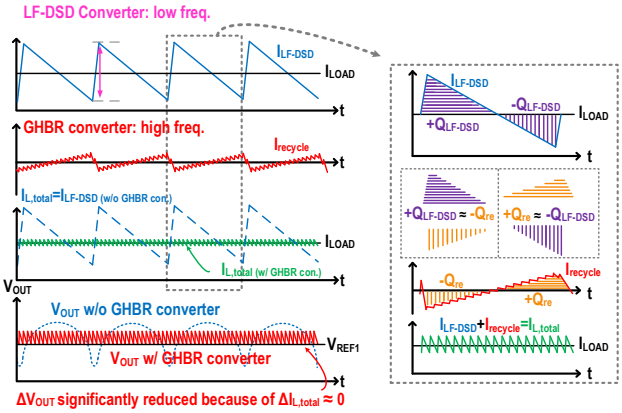

Fig. 7. Operation and principle of AC-ripple cancellation.

III. Circuit Implementations

Fig. 8(a) illustrates an LFTC incorporating a dynamic current generator (DCG) that establishes an instantaneous hysteresis window to prevent false triggering caused by rapid input transitions. As shown in Fig. 8(b), when V_{IP} rapidly approaches V_{IN}, the differential current ($I_P - I_N$) approaches zero, entering a current dead-zone. In this region, device mismatch may lead to incorrect output logic, potentially causing V_{OP} to erroneously switch to a high level. To mitigate this, the DCG dynamically boosts $I_{dynamic}$ as V_{IP} nears V_{IN}, introducing a temporary hysteresis window that stabilizes the output and prevents false switching. Once the signal exits the dead-zone, I_R

equals I_{BR}, and $I_{dynamic}$ returns to zero, ensuring normal operation without affecting the output state.

Fig. 9 presents the timing diagram of the transient response. During a light-to-heavy load transition, the GHBR converter rapidly toggles between phases Φ_2 and Φ_3 to boost $I_{recycle}$, delivering the required ΔI_{Load} to the output. As $I_{LF\text{-}DSD}$ begins to exceed I_{Load}, the converter shifts to phases Φ_1 and Φ_4 to recharge $C_{recycle}$, ultimately reaching steady-state operation where $I_{LF\text{-}DSD}$ closely matches I_{Load}. Conversely, during a heavy-to-light transition, the converter initially operates in phase Φ_4 to quickly drive $I_{recycle}$ negative, extracting the excess current from the output. Once $I_{LF\text{-}DSD}$ drops below I_{Load}, the converter transitions to phases Φ_2 and Φ_3 to discharge $C_{recycle}$, stabilizing again when $I_{LF\text{-}DSD}$ aligns with I_{Load}. Through this dynamic phase management, the GHBR converter effectively mitigates large overshoot/undershoot and long settling time (T_R), enabling fast and stable transient response.

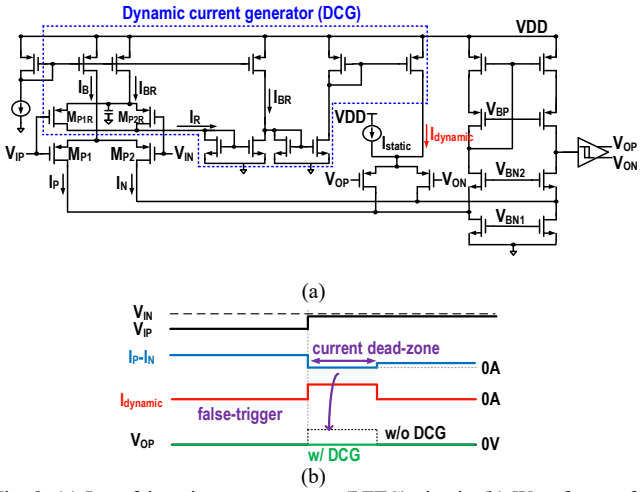

Fig. 8. (a) Low false-trigger comparator (LFTC) circuit. (b) Waveforms of proposed DCG.

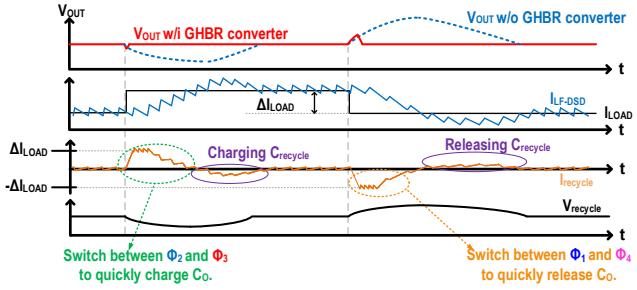

Fig. 9. Timing diagram of transient response.

Fig. 10 compares ΔV_{OUT} and the switching frequency ($f_{sw\_LF\text{-}DSD}$). As the target ΔV_{OUT} decreases, a higher f_{sw} is typically required, which limits the minimum achievable T_{ON}. In contrast, the proposed LF-DSD converter maintains a constant $f_{sw\_LF\text{-}DSD}$ of 100 kHz, regardless of ΔV_{OUT}, thereby ensuring sufficient T_{ON} under all conditions. Fig. 11 illustrates the relationship between V_{OUT} and the SR as a function of $V_{recycle}$. With T_{ON_re} fixed at 15 ns, $L_{recycle}$ = 60 nH, C_O = 30 µF, and ESR = 5 mΩ, the derived equation shows that SR increases with higher $V_{recycle}$, improving transient performance. However, this comes at the cost of increased output voltage ripple (ΔV_{OUT}). Conversely, reducing $V_{recycle}$ suppresses ΔV_{OUT} but degrades SR. This trade-off between transient response and voltage ripple can be optimized by adjusting the resistor divider that sets $V_{recycle}$. Fig. 12 compares the maximum slew rate of the total inductor current ($I_{L,total}$). The proposed topology achieves maximum rising and falling SR values of 74 V/µs and 17.33 V/µs, respectively—representing improvements of 22× and 7.8× compared to [3] and [2].

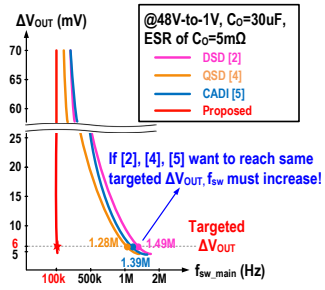

Fig. 10. ΔV_{OUT} and $f_{sw\_LF\text{-}DSD}$ comparison.

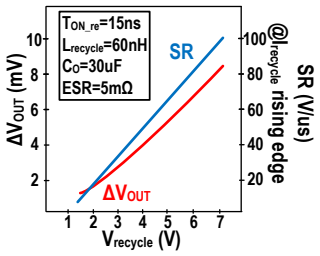

Fig. 11. ΔV_{OUT} & SR vs. $V_{recycle}$.

IV. Experimental Results

The proposed LF-DSD converter integrated with the GHBR converter is fabricated using a 0.18 µm CMOS process, with the chip micrograph and prototype shown in Fig. 13. The silicon area is approximately 2.18 × 4.08 mm², and the PCB area measures 60 × 47 mm². The resulting power density is approximately 2.36 mW/mm³. Although not specifically optimized for maximum density, the design demonstrates competitive performance and validates the effectiveness of the proposed architecture.

Fig. 14 presents the measured steady-state waveforms at I_{Load} = 5 A with the GHBR converter enabled. Activating the GHBR converter effectively suppresses ΔV_{OUT} to just 6.12 mV. Fig. 15 shows the measured load transient response. With the GHBR converter disabled, a load step from 1 A to 5 A within 50 ns results in a voltage undershoot of 360 mV and a recovery time T_R of 86.7 µs. Enabling the GHBR converter reduces the undershoot to 69 mV—a 5.2× improvement—and shortens T_R to 907 ns, a 95.6× reduction. Similarly, for a load step from 5 A to 1 A, the overshoot is 1.24 V and T_R is 42.6 µs when the GHBR converter is off. Turning it on reduces the overshoot to just 74 mV (a 16.7× improvement) and shortens T_R to 848 ns, representing a 50× improvement.

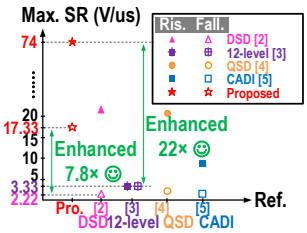

Fig. 12. Comparison of Max. SR of $I_{L,total}$.

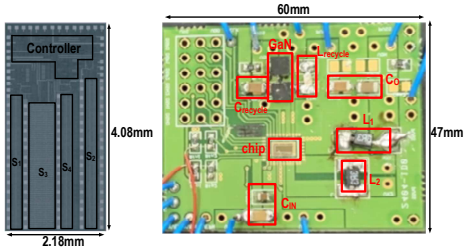

Fig. 13. Chip micrograph and PCB.

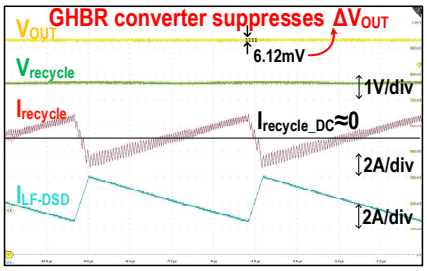

Fig. 14. Measured steady-state waveforms when turning on GHBR converter (V_{IN}=48V, V_{OUT}=1V, I_{Load}=5A, $f_{sw\_LF\text{-}DSD}$=100kHz, $f_{sw\_recycle}$=10MHz).

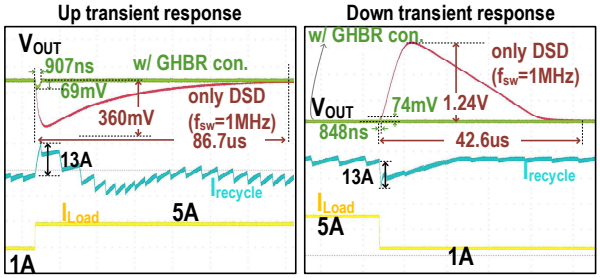

Fig. 15. Measured load transient response waveforms when V_{IN}=48V, V_{OUT}=1V, $V_{recycle}$=5V, $f_{sw\_LF\text{-}DSD}$=100kHz, and $f_{sw\_recycle}$=10MHz.

Fig. 16 presents the measured waveform under light-load conditions. As I_{Load} decreases from 5 A to 0.9 A, the GHBR converter actively stabilizes V_{OUT}. Once the DC component of $I_{LF\text{-}DSD}$ falls below 1 A, the light load detector disables the GHBR converter to enhance efficiency.

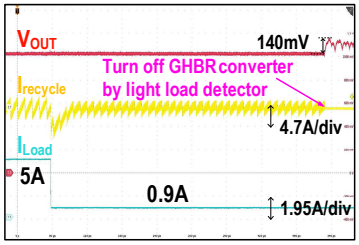

Fig. 16. Measured recycling current operation waveform when V_{IN}=48V, V_{OUT}=1V, $f_{sw\_LF\text{-}DSD}$=100kHz, $f_{sw\_recycle}$=10MHz, I_{Load} changes from 5A to 0.9A.

As shown in Fig. 17, when I_{Load} decreases from 5 A to 0.9 A, the GHBR converter actively stabilizes V_{OUT}. Once the DC component of $I_{LF\text{-}DSD}$ falls below 1 A, the GHBR converter is disabled by the LLD to improve efficiency. The measured efficiency results demonstrate that disabling the GHBR converter under light load conditions (I_{LOAD} < 1 A) increases peak efficiency from 92.84% to 96.51%, yielding a significant improvement of 3.67%.

Table I summarizes the ΔV_{OUT}, undershoot, overshoot, and recovery time of the proposed converter in comparison with state-of-the-art hybrid buck converters. While [2] achieves minimal component count, the proposed design incorporates additional circuitry to deliver superior efficiency and transient performance—making the trade-off highly favorable. At I_{Load} = 5 A, the proposed converter achieves a ΔV_{OUT} of just 6.12 mV, with an undershoot of only 69 mV and a recovery time of 907 ns—outperforming all other referenced designs.

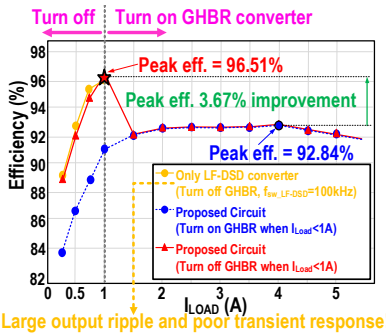

Fig. 17. Measured efficiencies between turning on and off the GHBR converter.

V. Conclusions

In summary, this paper presents a hybrid power converter architecture that integrates a low-frequency double step-down (LF-DSD) converter with a GaN-based high-frequency bidirectional recycle (GHBR) converter to achieve fast transient response and enhanced efficiency. The GHBR converter significantly reduces ΔV_{OUT} and recovery time during load transients, while the LF-DSD converter operates at a low switching frequency to maintain sufficient on-time (T_{ON}) and improve efficiency, particularly under light-load conditions.

Table I: Comparison with state-of-the-art works.

		[2] JSSC 2020	[3] ISSCC 2021	[4] VLSI 2022	[5] ISSCC 2022	This work
Process		0.18μm HV BCD & GaN HEMTs	0.18μm BCD	0.18μm HV BCD	0.18μm HV BCD	0.18μm HV BCD & GaN HEMTs (discrete)
Topology		DSD with AO²T Control	12-level converter	QSD	3:1 Ladder-based CADI	LF-DSD with GHBR converter
Input Voltage		48V	36V-60V	48V	36V-55V	48V
Nominal Output Voltage		1V	1.5V	1V / 1.2V	3.3V	1V
Max I_{load}		1.5A	8A	10A	3A	5A
F_{sw}		2MHz	2.5MHz	0.5MHz/1MHz	2.5MHz-5MHz	100kHz (LF-DSD)/ 10MHz (GHBR)
No. of power switches		4	24	8	7	6
Inductor		2×0.9μH	2×0.1μH	4×1μH	2×0.82μH	2×3μH/60nH
Cap. on power stage		1μF	11×1μF	3×2.2μF	4×0.22μF	10μF
C_O		22μF	188μF	15μF	20μF	15μF ($C_{recycle}$)/30μF
Output ripple @I_{Load}		70mV @0.2A*	13mV @N.A.*	18.4mV @7.3A*	10mV @1A	6.12mV @5A
Peak Efficiency		85.4% (100kHz) 79% (250kHz) 56.8% (2MHz)	90.2% (2.5MHz)	88.5% (500kHz) 74.7% (1MHz)	87% (2.5MHz) 83.7% (5MHz)	turn-off GHBR: 96.51%@1A turn-on GHBR: 92.84%@4A
Load transient	Load step /slew rate	1A	5A/25μs*	6.3A/50ns	N.A.	4A/50ns
	Undershoot	160mV	114.5mV*	80mV		69mV
	Recovery time	8.2μs (10%**)	85μs (2%**)*	1μs (2%**)		907ns (2%**)
	Load step	N.A.	N.A.	N.A.	N.A.	4A/50ns
	Overshoot					74mV
	Recovery time					848ns (2%**)

*Estimated from figure.
**Estimated time when its value is regulated back to a percentage of nominal value

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