A 2.5 GS/s 7.4 ENOB 6.8 mW VD-TD ADC with RC-Based Time-Residue Processing

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***Abstract*—This paper presents a 2.5 GS/s, 9.5-bit voltage-domain (VD) and time-domain (TD) hybrid ADC that addresses the speed and power limitations of traditional VD ADCs while overcoming the resolution constraints of TD ADCs. The proposed ADC minimizes CDAC switching for residue generation to the first VD conversion stage, with subsequent TD stages process residue in time manner. With the aid of a novel TD comparison and residue process scheme, the proposed ADC achieves 46.3 dB SNDR and 6.8 mW power consumption at 2.5 GS/s.**

Keywords—Time to digital converter, High-speed ADC, time-amplifier, RC-based delay generation

I. Introduction

Conventional VD ADCs for high-speed conversion suffer from speed and power bottlenecks caused by the comparator, CDAC switching, and residue amplification. While TD conversion can circumvent CDAC switching owing to its inherent open-loop comparison/ conversion operation and residue-processing [1], the finite time-domain full scale (T_{FS} < T_{sample}) makes T_{LSB} (Time Least Significant Bit) limited. This makes the design highly sensitive to jitter and device mismatch and makes TD residue suffer pulse shrinking. Hybrid VD-TD approaches, such as [2], [3], were introduced to overcome pulse shrinking. In these approaches, while all/some comparison is done in TD, the residue is generated in VD via CDAC switching, the close- loop configuration. Consequently, these approaches still suffer from power/speed limitations mentioned above (Fig. 1).

This work presents a 2.5 GS/s, 9.5-bit VD-TD hybrid ADC that minimizes closed-loop operation to the first-stage VD conversion, followed by two TD ADC stages operate entirely in an open-loop configuration. The TD ADCs are designed with energy-efficient RC-based delay cell. Between the two TD stages, a time residue generation scheme and time amplifier are proposed to mitigate power hungry voltage domain residue processing. The proposed design achieves an SNDR of 46.3 dB with a significantly reduced power consumption of 6.8 mW.

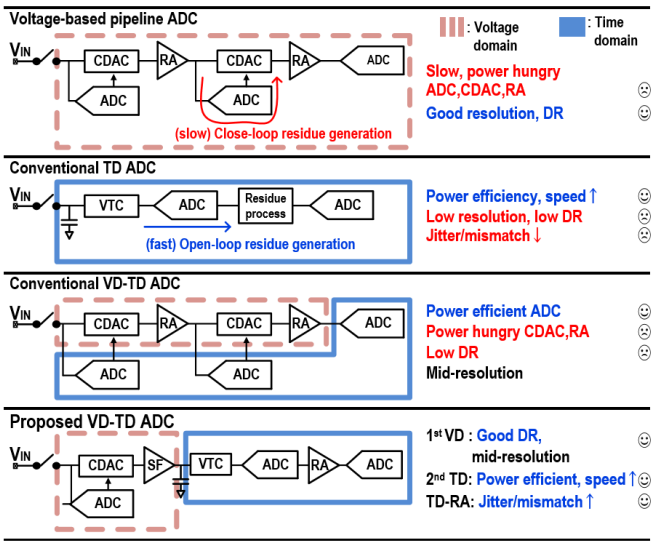


Fig. 1. Proposed VD-TD Hybrid ADC with TD-RA and prior arts

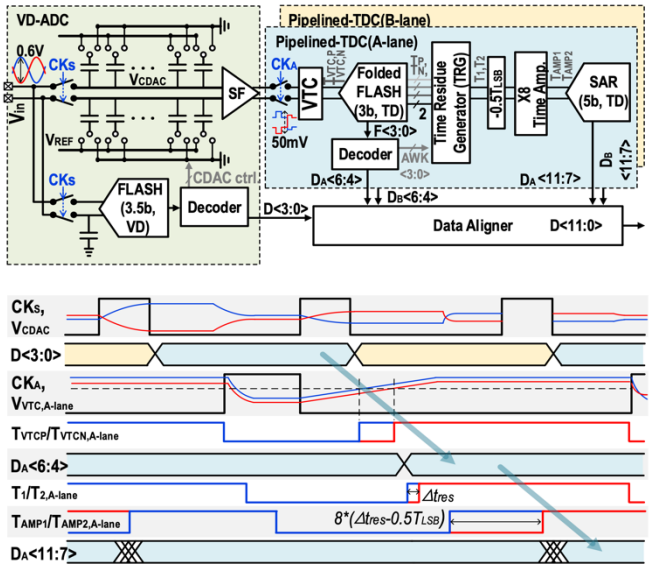


Fig. 2. Block diagram(top) and timing diagram(bottom) of proposed ADC

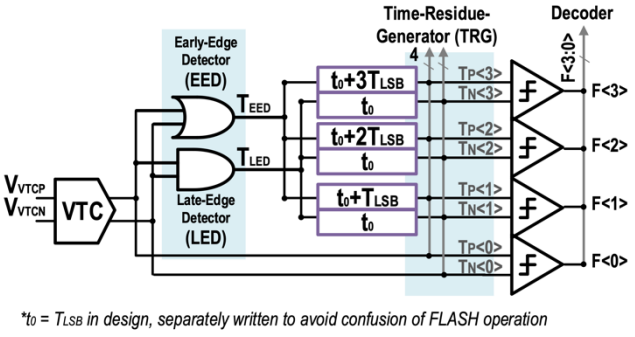
II. Architecture

Fig. 2 illustrates the architecture of the VD-TD Hybrid ADC. To enhance the input dynamic range and alleviate VTC nonlinearity at large voltage input, the first stage operates in the voltage domain (VD). An interpolating Flash ADC divides the 1.2 V_{pp} input signal into 12 distinct levels. The residue is fed into a 2x time-interleaved TDC through a source follower, enabling a wide input time full scale. The Voltage-to-Time Converter (VTC) transforms the residue voltage into two rising edges with a T_{FS} of ±80 ps. The VTC outputs goes into 3-bit Folded Flash TDC. The time-shifted rising edges made for FLASH TDC operation are also sent into the time-register inside the time-residue generator (TRG), stored until comparison ends. After comparison, one of the time-register is activated and outputs a residue. The residue is $0.5T_{LSB}$ time-subtracted and amplified eightfold through a time-residue amplifier. Lastly, the 5-bit SAR TDC quantizes the amplified residue. The quantization data of three stages are finally retimed at the data aligner.

III. Circuit Implementation

At the 1st stage TDC, the Folded Flash TDC scheme is proposed to address the stringent design symmetry requirement of Flash TDC [1], along with a 40 % reduction in power consumption (Fig. 3). The two rising edges generated by the VTC first enter comparator and AND/OR gate pair (LED/EED). The LED and EED identifies the later and the earlier rising edge, respectively. EED output is delay-added, and then compared with the LED output. The comparator that directly receives VTC output (L<0>) will determine which signal is faster, while the rest three comparators (L<1:3>) will quantize the absolute difference between the two rising edges. This folded architecture eliminates one side of the two symmetric pairs, improving the power consumption and comparison accuracy. Note that when input time is less than $1T_{LSB}$, VTC output (TP, TN<0>) is selected for residue processing instead of the LED/EED output, which alleviates delay contamination of LED/EED (Fig. 4). The RC-based delay cell (Fig. 5) is proposed to improve power efficiency over the inverter chain, which is predominantly used for delay generation in prior TDCs. The proposed topology generates delay by relying on the passive RC time constant, ensuring good delay linearity and a large delay in a single switching. Overall, the proposed delay cell saves TDC power by 12% compared to the inverter chain. Compared to cascoded NMOS (CS) delay cell [4] which can be low-power alternative, RC-based delay cell shows better linearity and corner stability while CS delay cell suffers from reduced head room (Fig. 6). The four time-shifted pairs are input to the TRG in parallel to the comparators.

The TRG is shown in Fig. 7, which consists of four time-register pair and time-multiplexer. The time-adder of [5] is used as time-register in this paper. The rising edge time difference is stored as capacitor voltage in time-register, avoiding redundant inverter chains [1],[6],[7] to wait for comparison completion. An encoder triggers one of the time-registers (AWK) according to comparators' output. The selected residue is 0.5 T_{LSB} delay-subtracted and goes into time amplifier.



t0 = TLSB in design, separately written to avoid confusion of FLASH operation

Fig. 3. Folded-FLASH TDC block diagram

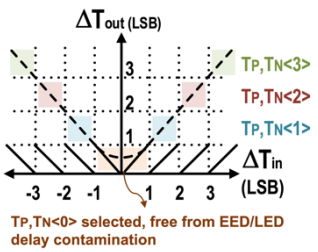


Fig. 4. Folded-FLASH TDC residue transfer plot.

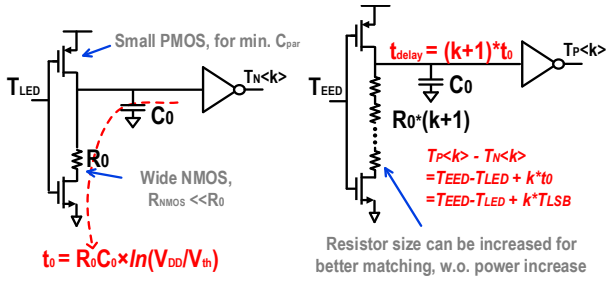


Fig. 5. RC-based delay cell for (left) t_0(=$1T_{LSB}$) delay and (right) t_0+ kT_{LSB} delay generation.

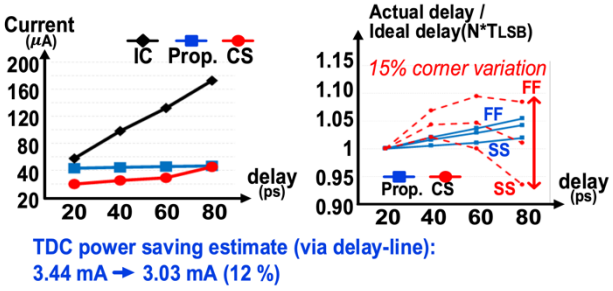


Fig. 6. Comparison versus other topologies: inverter chain (IC), cascoded NMOS (CS).

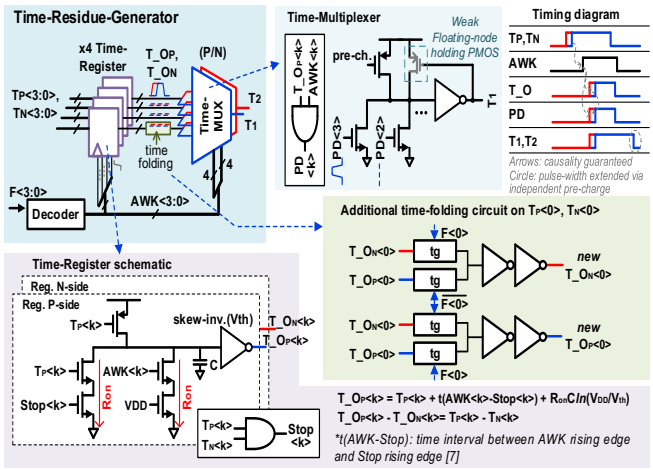


Fig. 7. Time-residue generator (TRG) block diagram implemented with time-register.

The proposed time amplifier, illustrated in Fig. 8, consists of two symmetrical dynamic circuits. The dynamic circuit is implemented with two NMOS cascodes with different W/L ratios: 4*W/L for branch A and W/L for branch B, resulting in 4-times higher resistance in branch B.

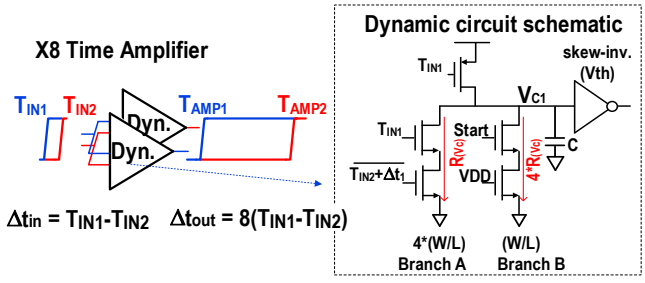


Fig. 8. ×8 time-residue amplifier schematic

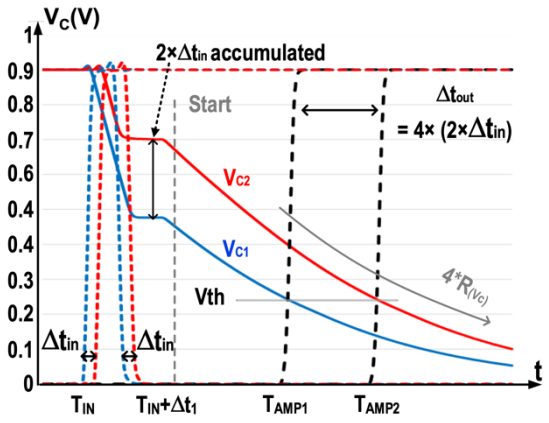


Fig. 9. Time-residue amplifier time waveform

The operation waveform is shown in Fig. 9. The first draining occurs in branch A for a duration of T_1-T_2+Δt_1 and T_2-T_1+Δt_1, respectively. Δt_1 is additional delay to ensure T_2+Δt_1 (or T_1+Δt_1) is later than T_1(or T_2). The two capacitor voltages at discharge cessation represent duration difference, 2(T_1-T_2). Branch B then re-discharges until the capacitor voltage falls below V_{th}. The final output rising edge time difference is 4*2(T_1-T_2), as 4-times higher resistance of branch B amplifies the perceived first-drain duration.

The first advantage of the proposed amplifier is its symmetrical response from dynamic circuit pair. Consistent gain within the input range is maintained, even in the presence of A/B ratio (N) mismatches (N1≠N2, 10 % discrepancy) between the two dynamic circuit. In contrast, single-sided operation in prior designs [8] causes mismatch between two input coefficients and shows gain drift inside input range (Fig. 10). Another advantage comes from the replacement of current-based drain circuitry with resistive drain circuitry, using the on-resistance of NMOS switches. Reduction of transistor sizes and cascode stacks significantly improves speed, power and noise.

Note that not only when assuming R_{on} is constant, but also when R_{on} changes as V_{ds} varies with the capacitor voltage, the time to reach V_{th} remains proportional to the A/B ratio, thereby maintaining consistent gain of the amplifier. To analyze this behavior quantitatively, the voltage at the Vc node of Fig. 8 can be represented as follows:

$$\frac{dQ_C(t)}{dt} = -\frac{V_C(t)}{R(V_C(t))} \quad (1)$$

R(Vc) is on-resistance of branch A or B in the dynamic circuit when drain voltage is Vc. Based on (2) and (3),

$$dQ_C = C \times dV_C(t) \quad (2)$$

$$R(V_C(t)) = \frac{L}{W} \times K(V_C(t)) \quad (3)$$

the time t required for Vc to transition from V_A to V_B is given by:

$$t = -C \times \int_{V_B}^{V_A} \frac{K(V_C(t))}{V_C(t)} dV_C(t) \times \frac{L}{W} \quad (4)$$

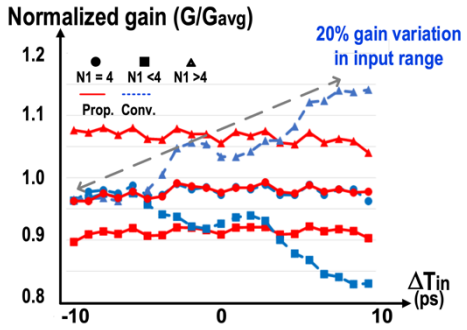


Fig. 10. Gain error simulation when two dynamic circuit have mismatch. (N1 ≠ N2 (10% offset))

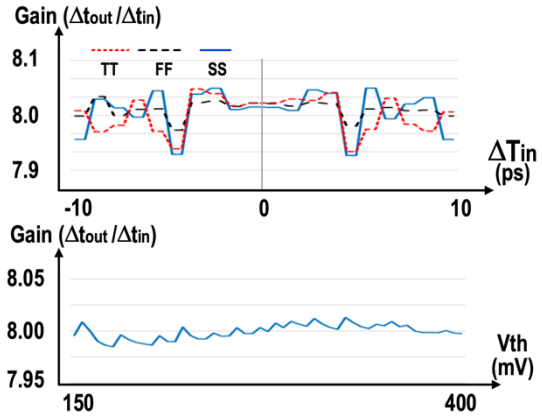


Fig. 11. (top) Simulated gain variation at corner conditions and (bottom) at different skewed inverter Vth. (Simulation interpolation offset is included.)

Thus, when W of branch B is four-times smaller than branch A, the accumulated voltage difference generated during branch A operation will generate 4 times larger rising edge delay at the output after branch B operation. PVT and Vth tolerability of the amplifier are shown in Fig. 10 and Fig. 11, respectively. Overall, this architecture enables precise amplification of picosecond-range signal at multi-GS/s rates, which is an unprecedented capability.

IV. Measurement Results

The proposed ADC is fabricated in 28nm CMOS with an active area of 0.013mm² and consumes 6.8 mW at 2.5 GS/s. Foreground calibration is applied to VD stage reference voltage and VTC current bias-voltage, and background calibration is applied to mitigate gain and offset mismatches between each stage. It achieves SNDR of 46.3 dB and an SFDR of 58.3 dB at Nyquist input frequency, respectively (Fig. 12). Measured SNDR and SFDR according to sampling frequency and input frequency is plotted in Fig. 13. The input dynamic range of 48.5 dB, along with SNDR performance across input amplitudes, is also illustrated in Fig. 14. Fig. 15 shows DNL/ INL of the proposed ADC. Measured DNL and INL are -0.4/+0.7 LSB and -0.5/+0.5 LSB, respectively. Power figures and die photo are shown in Fig. 16 and Fig. 17, respectively. Table I compares proposed architecture to prior arts. Achieving a FoM of 16.2 fJ/ conv-step, it surpasses prior hybrid ADCs in energy efficiency while maintaining competitive speed and resolution performance.

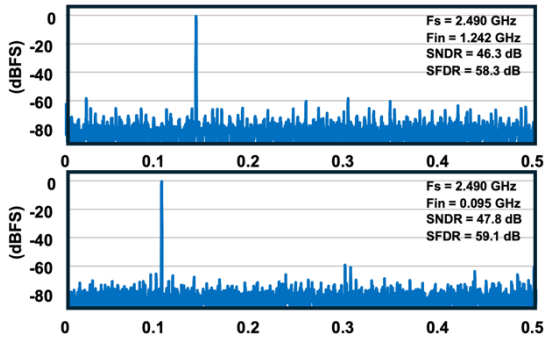


Fig. 12. Measured FFT spectrum, near-Nyquist (top) and near-DC (bottom) Output data decimated by 81.

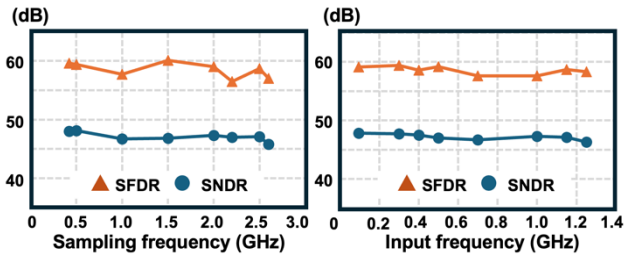


Fig. 13. Measured performance according to sample frequency and input frequency

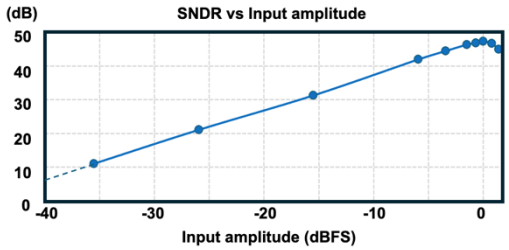


Fig. 14. Measured SNDR versus input signal amplitude

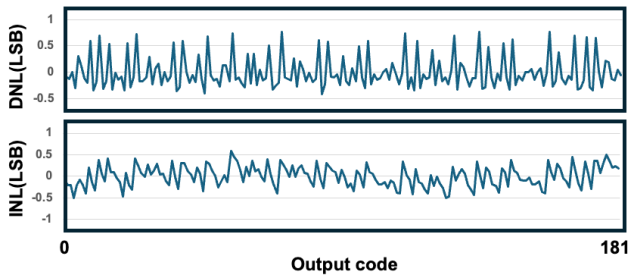


Fig. 15. Measured 7.5 bit level DNL/INL

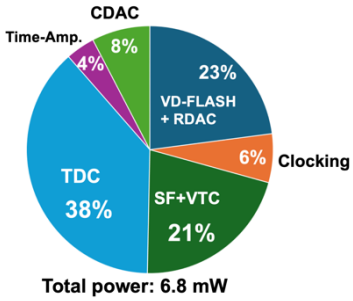


Fig. 16. Power breakdown

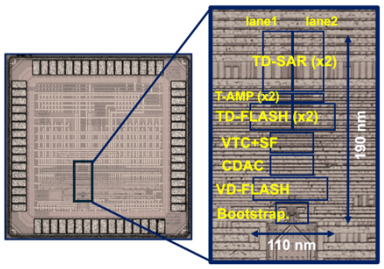


Fig. 17. Die photo

TABLE I. COMPARISON TABLE

	proposed	[1]	[2]	[3]	[4]	Z. Zheng, ISSCC2020
Architecture	Pipeline, VD-TD	Two step TDC	4×TI VD-TD	2×TI, VD-TD	Pipeline, VD-TD	Pipeline, VD
residue gen.	Time, Voltage	Voltage	Voltage	Voltage	VTC	Voltage
time-delay gen.	RC-based	SDT(CS)	IC	IC	CS	-
process	28	14	22, FinFet	28	28	28
resolution (b)	9.5	8	7	9	10	6
Supply (V)	0.9	0.8	0.85/0.9	0.9	0.9	0.9
Fs (GS/s)	2.5	5	3	2.8	2.6	3.3
SNDR @ Nyq. (dB)	46.3	40.8	37.7	51.8	51.7	34.2
SFDR @ Nyq. (dB)	58.3	53.12	47.8	72.4	71	45.5
Power (mW)	6.8	7.4	3.2	18.1	13.9	5.5
FoMw @ Nyq. (fJ/step)	**16.2**	16.6	18.2	20.3	17.6	40
FoMs @ Nyq. (dB)	158.9	156	153.8	160.7	161.1	148.9
Area(mm^2)	0.0133	0.0014	0.0045	0.0097	0.0059	0.0166

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