A 22FDX® Wi-Fi PA Achieving Output Power of 1.1Watts with 41% PAE at 3.8V Supply Voltage

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***Abstract*— This paper presents a Wi-Fi PA for mobile transceivers using an improved LDMOS device in 22FDX®. The two stacked PA design with this improved LDMOS device achieves 30.5dBm of Saturated Power with 41% PAE and 26dB Low Power Gain at 6.75GHz and at a supply voltage of 3.8V. Preliminary modulation measurements for this PA achieve -35dB EVM, -35dBc/-58dBc for ACPR1/2 for MCS7 modulation at 80MHz bandwidth without DPD at 17dBm of output power. Reliability stress test for 72hours and ruggedness test at a VSWR of 10:1 show almost no degradation in Gain, Psat and PAE. The ruggedness test at VSWR of 6:1 was repeated with the supply voltage increased from nominal supply of 3.8V to show the PA with improved LDMOS degrades at higher than 9.5V for a gate length of 190nm, which is one of the highest reported breakdown voltage for a LDMOS device in sub-45nm FDSOI technology.**

***Keywords*— Wi-Fi, FDSOI, VSWR, Improved LDMOS, Power Amplifiers, Pout, Psat, PAE.**

I. INTRODUCTION

The demand for mobile data continues to increase with expanding social media, cloud, and industrial applications. Given the convergence of mobile devices and edge computing, new applications like Internet of Things (IoT), hot spots and Miracast, connectivity to the cloud is enabled. These smart mobile devices now need to operate in long or short range and peer to peer modes and still offer excellent battery life.

Wi-Fi since its inception and introduction in 1997 by the 802.11 committee has become ubiquitous in providing the necessary connectivity at home and work, to meet this demand of mobile data. To meet future growth of this ever-increasing demand for higher data rates newer Wi-Fi standards, like WiFi8 are in the offing. In recent years, highly integrated transceivers and combo radio devices provides ubiquitous wireless connectivity for smart device to the clouds. These transceivers use either standalone Power Amplifiers (PA's) or integrate PA on the same die using the same technology [1] – [3].

High-Power Wi-Fi7/8 PA designs not only face significant challenges due to their stringent linearity and power consumption requirements but also must meet strict linearity and efficiency requirements. The PA's must pass reliability under extreme VSWR conditions. This paper introduces an improved LDMOS device in Globalfoundries 22FDX® for Wi-Fi PA applications. The device has good linearity, efficiency and offers excellent reliability. The following sections provide details on key performance metrics of the improved LDMOS device. A Wi-Fi PA is designed and fabricated with the improved LDMOS device achieves 1.1W of Saturated Power (Psat) at 41% PAE. Rigorous stress and ruggedness measurements were done to show the device can withstand extreme VSWR conditions.

II. DESIGN

A. 22FDX® Technology

The PA was implemented in GlobalFoundries 22nm FD-SOI CMOS technology. The process design kit (PDK) offers a variety of BEOL options for on-chip inductors, baluns and transformers. BEOL Option 11 with 9 Cu levels - 2Mx_5Cx_1JA_1OI, Option 19 with 10 Cu levels - 2Mx_5Cx_1JA_1QA_1QB and Option 24 with 9 Cu levels - 2Mx_3Cx_2JA_1QA_1QB of metal layers. The widely used BEOL configuration is Option 19, containing 10 Copper (Cu) metal layers was used for this PA. The core device offered in 22FDX® is a Super Low Threshold Voltage (Slvt) which has a record Fmax of 371GHz, and Ft of 377GHz. The 22FDX® has a buried oxide (BOX) layer that isolates fully depleted transistors from the low-resistivity substrate, decreasing the capacitive parasitics. The core Slvt device is used as the gm device in this PA design and has a drain-source break-down voltage of 3V at zero gate-source potential, while Hot Carrier Injection (HCI) starts occurring at 1.8V drain-source voltage.

B. Regular versus Improved LDMOS Device in 22FDX®

Globalfoundries 22FDX® process offers a Regular LDMOS for PMIC applications, and an improved LDMOS for Wi-Fi PA designs. A cross-section of Regular LDMOS and Improved LDMOS is shown in Fig. 1 and Fig. 2. Both the Regular and Improved LDMOS are not built on SOI and are Drain engineered Thick Oxide devices. The devices are available in different gate lengths to support different supply voltages- 3.3V, 5V, and 6V for a variety of applications and designs. The LDMOS device is an asymmetric device to tolerate high

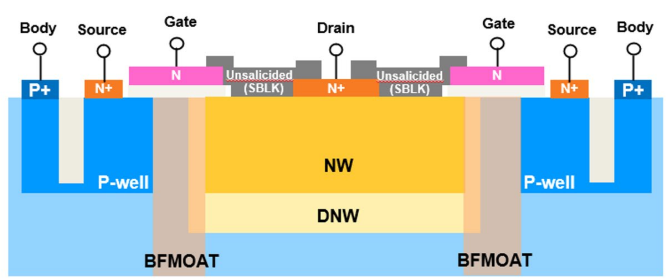

Fig. 1. 22FDX® Regular LDMOS for PMIC applications

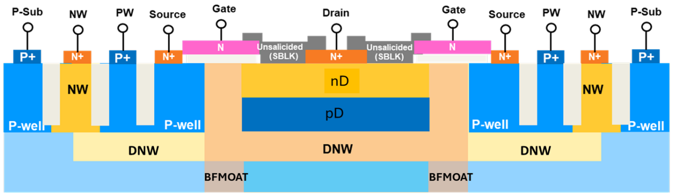

Fig. 2. 22FDX® Improved LDMOS for PMIC applications

voltage swings on the drain, but it is a two-finger device and is symmetrical around the drain.

The Improved LDMOS is derived from Regular LDMOS, using one additional dedicated mask on the drain side. The nDrift and pDrift implants reduce sidewall capacitance and optimize for higher breakdown voltage. Table.1 shows, key performance metrics of Improved LDMOS device. This device construction achieves much better Fmax, lower Cout, and a higher breakdown voltage than regular LDMOS. The lower output capacitance Cout of the new device is less than half of the regular device, and the increased Fmax helps the PA operation at higher end of Wi-Fi frequency bands at significantly improved Power Added Efficiency (PAE).

Table 1. Performance metrics of Improved LDMOS

Parameter	22FDX Regular LDMOS	22FDX Improved LDMOS
Vdd[V]	3.3	3.3
Lg[nm]	250	190
FingerW[um]	5	5
# of Fingers	2	2
Multiplicity	1	1
Total W[um]	10	10
Gm_Max(mS)	5.7	5.3
Cout(fF)	11.5	**4.7**
f_{MAX}[GHz]	90	111
f_T[GHz]	56	47.4
BVdss[V] @1uA/um	9.6	11.3

C. PA Design

The PA design to demonstrate the improved LDMOS device is a straightforward single stage design with Slvt NMOS as Common Source (CS) device and improved LDMOS as Common Gate (CG) device, as shown in Fig. 3. The improved LDMOS device size is 4.8mm with a gate length of 190nm and Slvt device size is 2.64mm with a gate length of 24nm. Custom transformers in BEOL Option 19 have been designed to transform 50ohm reference impedances into optimal impedances for the PA at the input and output. A die photo of the designed PA is shown in Fig.4. The input and output RF Pads – GSG (Ground Signal Ground) are orthogonal to DC Supply and Bias Pads. The PA is biased at an IDDQ of 110mA, the improved LDMOS Gate voltage is at 2.2V and the PA supply is at 3.8V.

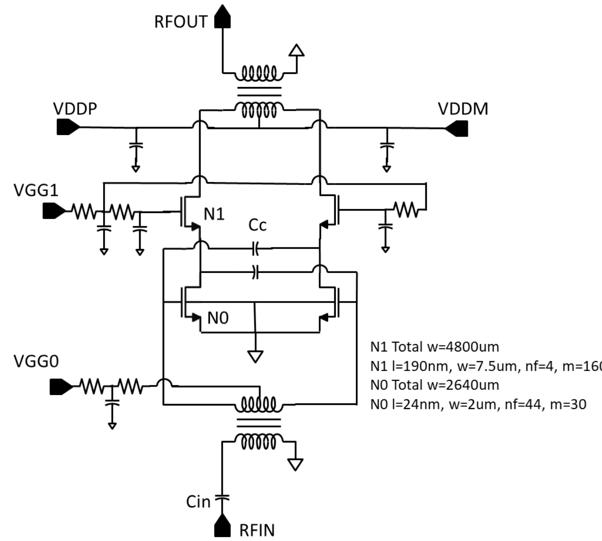

Fig. 3. Wi-Fi PA with Slvt and Improved LDMOS at 3.8V supply

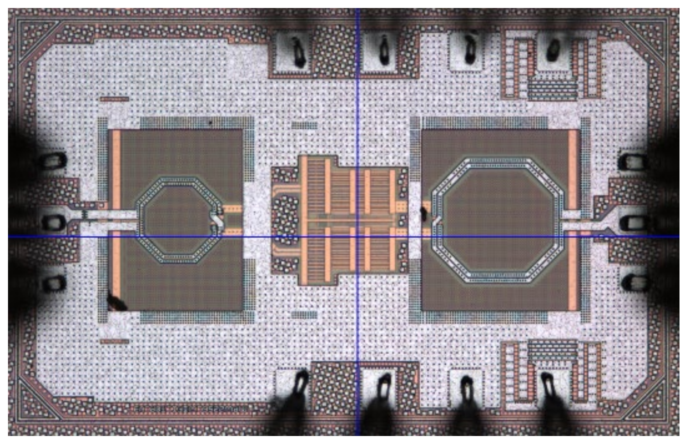

Fig. 4. Die Photo of Wi-Fi PA

III. Measurement

A. S-Param, Load Pull, EVM Measurements

The measured S-parameters are shown in Fig. 5 and large-signal power sweeps, continuous wave (CW) characteristics are shown in Fig. 6. Over the 5 to 7GHz frequency band, the PA has a small-signal gain of 26dB, and input/output return loss around -10/-4dB. The peak measured gain is at 6.75GHz vs 7GHz simulated. This is attributed to continuing model development and pending model to hardware correlation for the Improved LDMOS device. Nevertheless, s-parameter between simulation and measurements are close. Since the measured gain peaks at 6.75GHz, the load pull measurements were done at this frequency.

The measured saturated output power Psat at 5dB compression point is 30.5dBm with a peak PAE of 41%. Fig.6 shows good correlation between simulation vs measurement of gain vs output power. Minor adjustments to the improved LDMOS device model were made for this comparison. Also, the load impedance to PA was tuned to provide a more optimal impedance other than 50 Ohm termination to improve the measured performance.

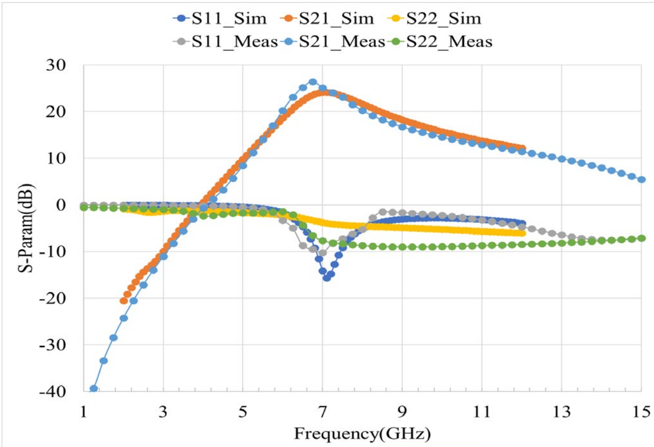

Fig. 5. S-Parameter measurements at IDDQ 110mA and 3.8V supply

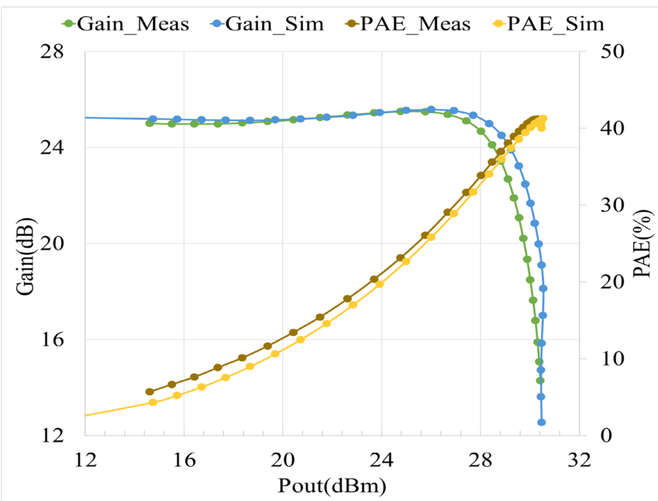

Fig. 6. PA Load Pull power sweep Measured vs Simulated at 3.8V supply

The Wi-Fi PA AM-AM is excellent as seen from Fig. 6 and the AM-PM is also relatively good from the EVM measurements shown in Fig. 7. ACPR and EVM measurements without pre-distortion is shown for MCS7 64-QAM modulation for a BW of 80MHz at 6.75GHz for output power of 17dBm.

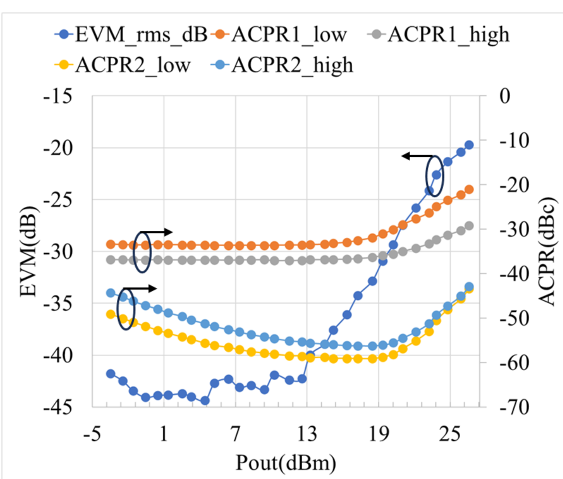

Fig. 7. PA EVM, ACLR for MCS7 80 MHz 64-QAM modulation vs Pout

B. *Stress and Ruggedness Measurements*

The large signal reliability- stress and ruggedness tests were characterized in a Maury load-pull system. The PA, as mentioned has transformer based matching network to provide necessary source and load impedances but additional load pull optimization is performed for optimal performance. Stress and Ruggedness tests are performed around this optimal load impedance.

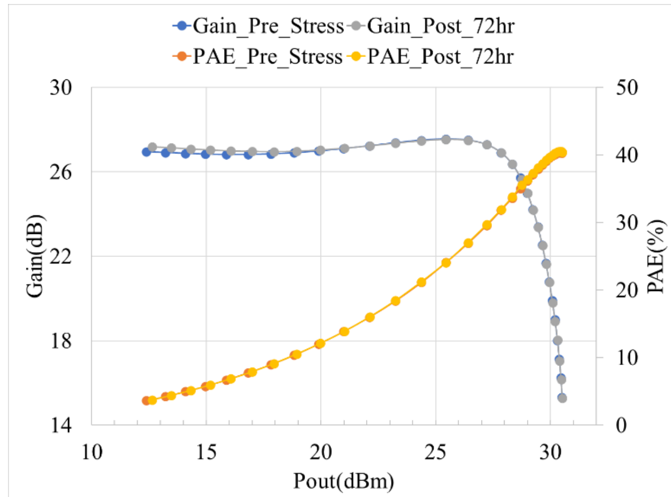

Fig. 8. PA 72hour stress test at Psat 3.8V supply and 6:1 VSWR

Stress test is performed by keeping the PA output at saturated power for 72hours. Gain and PAE measurements are done both pre and post stress. Fig. 8 shows very little degradation pre and post stress test.

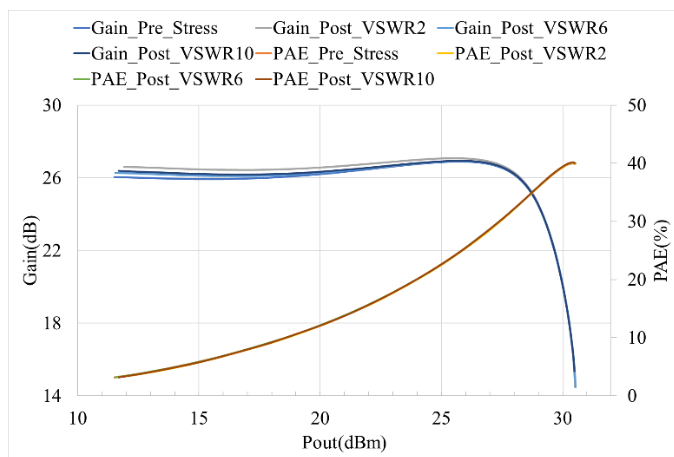

Fig. 9. PA ruggedness test at Psat vs accumulated VSWR (2 to 10)

Ruggedness test is performed at various VSWR. First, pre-test measurements like Gain and PAE versus power are done at VSWR of 1. Second, the PA output power is set to Psat and the VSWR is set to 2. Third, the angle is stepped at 30^0 to complete the full circle. The PA is stressed at each angle for 15 seconds. There is a ten-minute cool down before measuring PA performance post-test. The test is repeated for higher VSWR in steps of 2 until a VSWR of 10. Fig.9 shows PA performance has negligible change pre and post ruggedness test.

C. Breakdown Test

To determine the breakdown voltage of the improved LDMOS, the PA is subjected to both stress and ruggedness tests with increasing supply voltage. First, the PA is stressed at Psat for 72hours. The same device is subjected to ruggedness test at VSWR of 6:1 starting at nominal supply of 3.8V. The Gain and PAE are measured post-test at the nominal supply of 3.8V and VSWR=1. The Ruggedness test is repeated but the PA supply voltage is increased in steps of 200mV, but as mentioned post stress measurement is done at nominal supply and VSWR. The PA Gain, Psat and PAE show very little change until a supply higher than 9.5V. This combined Stress and Ruggedness test was repeated on several parts and the PA consistently shows degradation at a supply higher than 9.5V. Therefore, the improved LDMOS breakdown voltage is 9.5V for a gate length of 190nm.

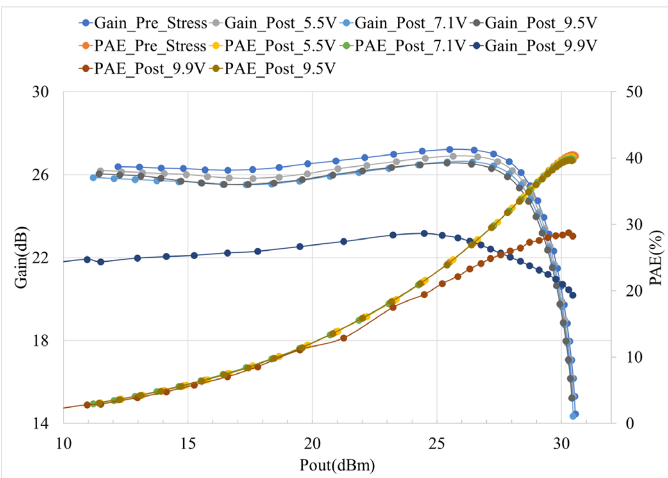

Fig. 10. Improved LDMOS breakdown test vs supply at Psat and 6:1 VSWR

Table 2. Performance summary and comparison

Reference	This Work	[4]	[5]	[6]	[7]
Frequency	**6.75 GHz**	5.5 GHz	5.4 GHz	2.44 GHz	6 GHz
Supply	**3.8V Fixed**	SIMO-APT	3.3V Fixed	3.3V Fixed	5V Fixed
Process	**22nmFDSOI**	28nm CMOS	22nm FDSOI	40nm CMOS	22nmFDSOI
PA Arch	**Linear**	Linear	Linear	Linear	Linear
Device/ Stack	**Core+new LDMOS**	Core+ LDMOS	Core+ 3.3V LDMOS	Core+ 3.3V LDMOS	Core+new 5V LDMOS
Gain	**25 dB**	<25 dB*	15 dB	16 dB	26.5 dB
Psat	**30.5 dBm**	28 dBm*	26 dBm	29 dBm	29.5 dBm
Peak PAE	**41%**	<35%*	22%	not reported	40%
EVM	**-35dB**	-40dB	NA	-48dB	NA
ACPR	**-58dBc**	-47dBc	NA	NA	NA
P_{PBO}	**17.2dBm**	10dBm	NA	18dBm	NA
Modulation	**MCS7-80MHz**	MCS11-40MHz	NA	Wi-Fi6	NA
DPD	**No**	Yes	No	No	No
Breakdown	**9.5V**	<8V*	<5V	<8V*	10V

* estimated/extrapolated

A performance summary comparison is shown in Table 2. The Wi-Fi PA with improved LDMOS introduced in this paper has one of the highest output powers and PAE for a supply voltage of 3.8V. The new device has excellent reliability, passing a VSWR of 10 requirements for Wi-Fi PA and has one of the highest breakdown voltages reported for a Wi-Fi PA in sub-45nm technology.

IV. Conclusion

This paper demonstrated a Wi-Fi PA using the improved LDMOS device in Globalfoundries 22FDX® technology. The two stack PA design using this improved LDMOS device achieved 1.1Watts of Saturated Output Power with 41% PAE at a supply voltage of 3.8V. Without Analog or Digital Pre-Distortion, the PA measures at 6.75GHz an EVM of -35dB, ACPR1/2 of -35/-58dBc for MCS7 modulated signal of 80MHz BW at an output power of 17dBm. Stress and ruggedness tests show the PA is reliable at a VSWR of 10:1. Accumulated stress and ruggedness test with increasing supply at a fixed VSWR of 6:1 shows the PA has no degradation in performance and is functional until a breakdown at 9.5V. The model to hardware correlation is reasonable, and the improved LDMOS device model will be production maturity in year 2025.

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