The Injection Locked Cyclic-Coupled Ring Oscillator for Phase Order Stability

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***Abstract*—The injection-locked Cyclic-Coupled Ring Oscillator time reference is demonstrated for the first time as a highly-scalable method of generating sub-gate delay resolution without any passive devices. It solves the phase order uncertainty issues typically associated with Cyc-CRO. In this work, a 10 ps time reference is fabricated in 65nm which consumes only 1.15 mW and occupies only $0.000275\mathrm{mm}^2$.**

***Index Terms*—TDC, time reference, ring oscillator, Cyc-CRO, Injection Locking**

I. Introduction

Time-domain signal processing is the enabler for a wide variety of key technologies, such as LIDAR [1], time-of-flight spectroscopy to interrogate deep tissue samples [2], [3], and time-domain ADCs most suitable for inclusion on SoCs developed on modern process technologies [4].

The use of high resolution Time to Digital Converters (TDCs) in modern time-domain circuits has demanded circuits with sub-gate delay precision [5]. This is most-commonly achieved using a ring oscillator with resistive interpolation between the phases [6]. The inclusion of resistors between the phases introduces a trade-off between area and power consumption, and limits scalability in highly-scaled CMOS technologies. The Cyclic-Coupled Ring Oscillator (Cyc-CRO) [7], [8] has shown promise as a scaling friendly, passive-free method of achieving sub-gate delay timing precision. The Cyc-CRO's suitability for use as a time reference in TDCs has been limited by its having multiple oscillation modes, any of which can be dominant at startup, resulting in different phase orders. The only TDC implementations making use of Cyc-CROs rely on mode detection circuitry to decode the phase order [9]. This paper presents the injection-locked Cyc-CRO which ensures startup in the most efficient mode, and known phase order, greatly simplifying this circuit's use as a TDC time reference.

II. The Cyc-CRO

The Cyc-CRO is a collection of M individual inverter-based ring oscillators, each capable of achieving a delay τ_G between phases. If the rings' edges are in-phase, there is no resolution improvement over a single ring oscillator, but if the rings could be offset by τ_G/M, sub-gate delays can be achieved. Fig. 1 shows a three-ring Cyc-CRO, which, as illustrated by the simplified timing diagram, can achieve $\tau_G/3$. To ensure the M rings are equally offset, they are weakly coupled together using vertical rings. It is shown in [7], [8] that these weak vertical rings lock the main rings together.

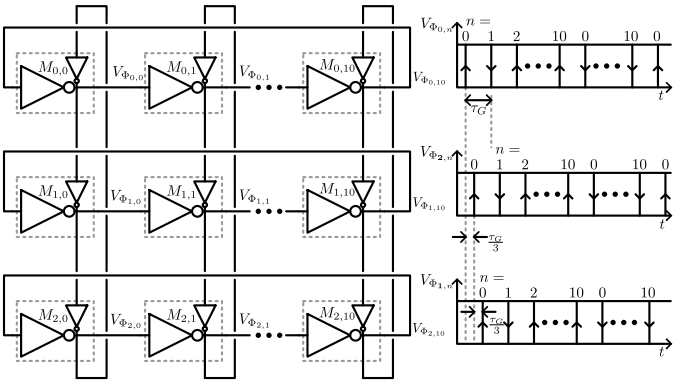


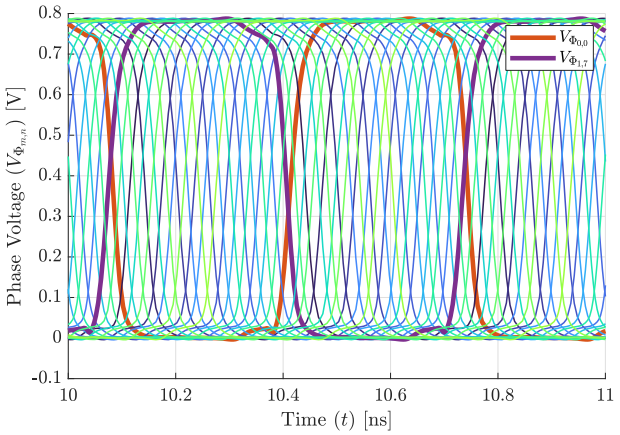
Fig. 1. 3×11 Cyc-CRO showing inter-ring coupling.

A. Oscillation Modes

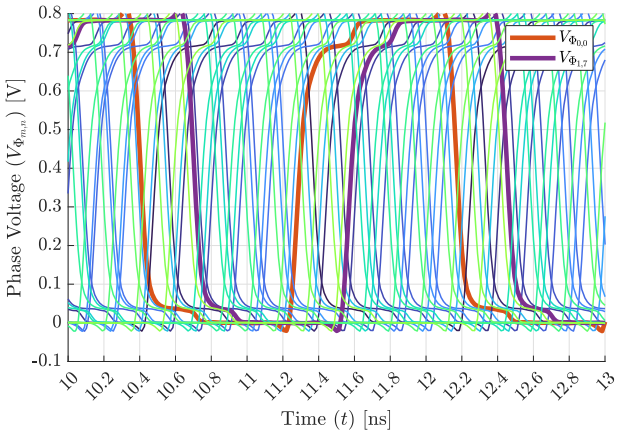
Because the vertical rings themselves form closed rings, periodicity dictates that they can have phase shifts which are multiples of 2π. This results in multiple modes of oscillation [10], as illustrated by the phase shift between the vertical rings, ψ_0:

$$\psi_0 = k\left(\frac{2\pi}{M}\right) \quad 0 < k < M,\ k \in \mathbb{Z}\ . \tag{1}$$

Since $M = 3$ in this case, there are two valid oscillation modes. While larger M will result in more modes, $M = 3$ is the minimum number of rings required to form a Cyc-CRO, thus there are always two or more valid modes. The waveforms, in both modes, for a 3-ring ($M = 3$), 11-element ($N = 11$) Cyc-CRO are shown in Fig. 2. The $k = 1$ mode shown in Fig. 2a is much more power efficient than the $k = 2$ mode due to lower crowbar current in the vertical coupling inverters, and so the $k = 1$ mode should be used. The Cyc-CRO, unfortunately, chooses a mode at random at startup. Previous implementations [9] have relied on high M, so there are many modes, and an increased likelihood a favourable



(a) Desired mode ($k = 1$).



(b) Undesired mode ($k = 2$).

Fig. 2. Cyc-CRO waveforms initialised in (a) the desired mode of operation and (b) the undesired mode of operation.

mode is chosen. This approach still requires mode detection circuitry, however, since the mode cannot be chosen.

III. The Injection Locked Cyc-CRO

Compared with mode detection circuitry [9], a much simpler method of selecting a known, efficient mode is employed in this design. From Fig. 2, note that in the desired $k = 1$ mode, the node $V_{0,0}$ is almost out of phase with $V_{1,7}$, but in the undesired $k = 2$ mode, the two nodes are much closer to being in-phase. This can be exploited by injection locking a differential clock signal into the oscillator at these nodes to promote the nodes being out of phase, and thus promote the desired $k = 1$ mode, as shown in Fig. 3. Not only does injection locking ensure the highest efficiency mode with a fixed phase order, it also provides the benefits traditionally associated with injection locking; improved low-frequency phase noise and jitter performance [11].

A. Startup Mode Selection

The simulated startup waveforms are shown in Fig. 4a. As the supply voltage is ramped, the differential clock signal input to the injection cell, Φ_{CLKIN}, is also ramped since it is in the

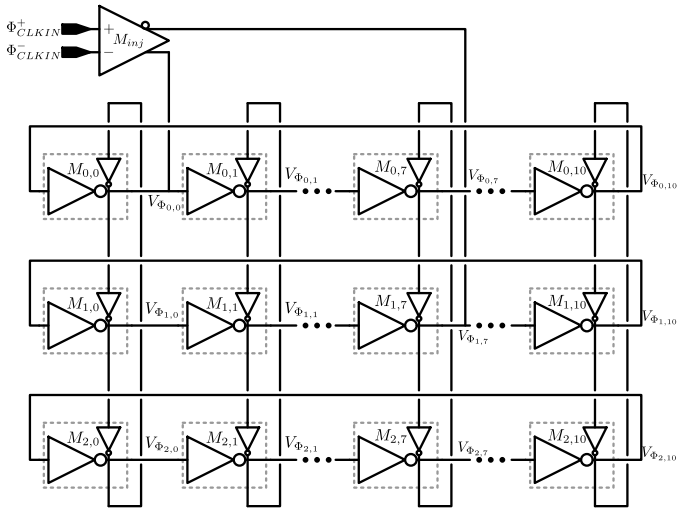


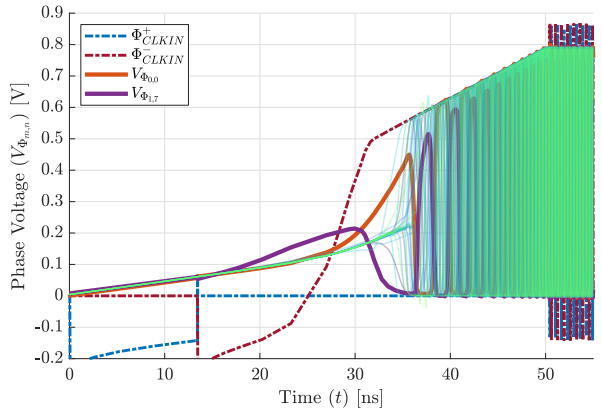
Fig. 3. Schematic of the Injection Locked Cyc-CRO showing clock injection to anti-phase nodes.

same supply domain. During the startup phase, Φ^+_{CLKIN} and Φ^-_{CLKIN} are held apart statically such that $V_{0,0}$ and $V_{1,7}$ are pulled apart as the supply reaches a level for the Cyc-CRO to start. This sets the $k = 1$ mode, which is then stable while the Cyc-CRO is powered. Once the Cyc-CRO is running, the injection clock is passed through Φ_{CLKIN}, and the Cyc-CRO becomes injection locked, as shown in Fig. 4b.

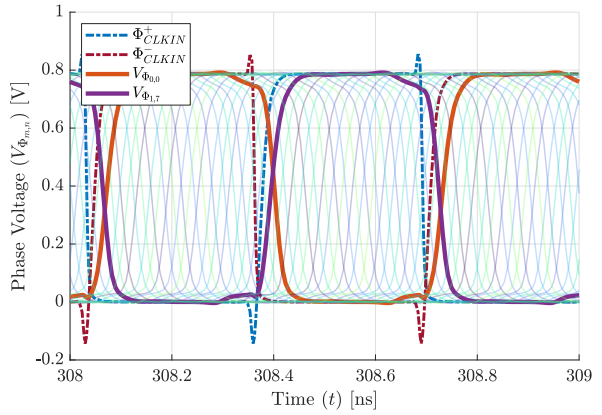
B. Injection Locked Cyc-CRO Design

The injection locked Cyc-CRO was designed in a 65nm test chip as part of a Time-Domain ADC. It is designed to have a resolution of 10 ps, below the 20 ps minimum gate delay of the technology. Three rings were chosen to reduce the possible modes to two. Eleven ring elements were chosen to reduce the injection clock to 1.52 GHz. The Cyc-CRO cells are three-inverter cells, as shown in Fig. 5. The coupling (vertical) inverter is of minimum dimensions with its P/N drive strength matched, and the horizontal main inverter has $5\times$ the drive strength. The output phase is buffered to isolate the Cyc-CRO from loading and sampling kickback of the TDC. The injection cell re-uses the weak coupling inverters to inject current, while minimising load mismatch on $V_{0,0}$ and $V_{1,7}$.

Floorplanning and routing is very important to preserve the resolution and minimise the power consumption of the Cyc-CRO. Typically, ring oscillators are laid out in an out-and-back ring to minimise routing parasitics, but this becomes more complicated for the Cyc-CRO since it is a 2-dimensional topology. One delay cell from each ring is selected to form a macro cell so that the vertical routing could be done within the cell, as shown in Fig. 6a. The macro cells are then routed in the typical out-and-back fashion, with the block of dummies in the top left corner containing the injection clock cell and a mid-point threshold generation cell for the downstream sampling circuits. The physical layout of the cell is shown in Fig. 6b, measuring only $30.8\ \mu\text{m} \times 8.9\ \mu\text{m}$. The extracted capacitance of each internal node in the Cyc-CRO is plotted in Fig. 7,



(a) Startup mode selection.



(b) Steady state locking.

Fig. 4. Cyc-CRO simulations illustrating injection locking-based mode selection and steady-state locking.

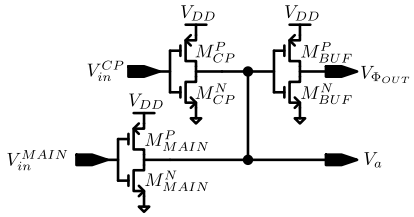
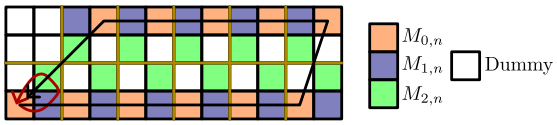
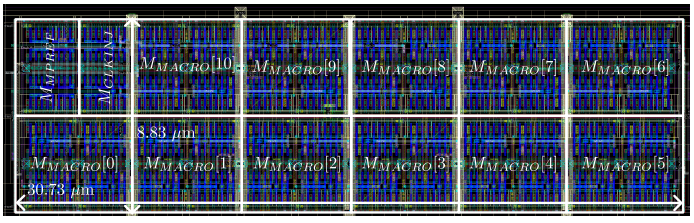


Fig. 5. Schematic of the Cyc-CRO delay cell.



(a) Floorplan: grouped by delay cell for improved parasitics.



(b) Layout of the Cyc-CRO.

Fig. 6. Floorplan and layout of the Cyc-CRO showing macro cell topology.

showing the uniformity of the cell capacitance across the array. A subtle three-node pattern can be observed to repeat; this is due to minute mismatches in the macro cell. The increased parasitics at $V_{0,0}$ and $V_{1,7}$ are due to the injection nodes, but are only $10-20$ %. The increased capacitance at these nodes is, however, compensated by the extra 20 % drive strength of the injection cells. The spikes at $V_{0,5}$, $V_{1,5}$ and $V_{2,5}$ correspond to the connection from the bottom to the top macro cell on the right, and those at $V_{0,10}$, $V_{1,10}$ and $V_{2,10}$ the bottom to top connection on the left. The Cyc-CRO was fabricated in

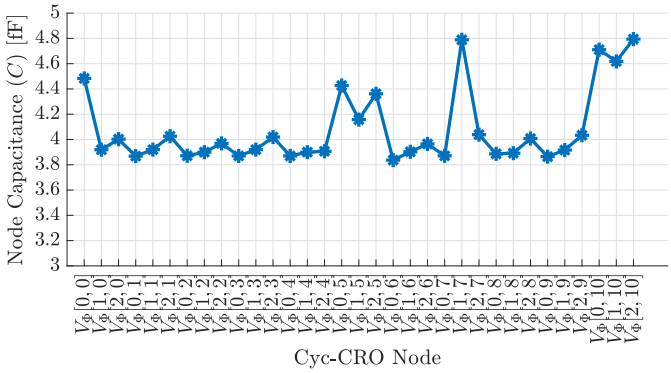


Fig. 7. Plot showing variation in Cyc-CRO capacitance across all cell nodes.

a standard 65nm technology; the die micrograph is shown in Fig. 8.

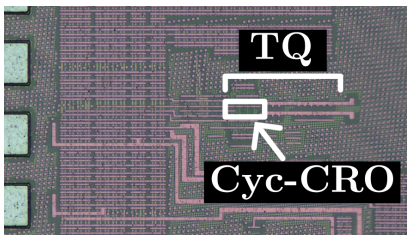


Fig. 8. Die micrograph of the fabricated Cyc-CRO in 65nm.

IV. Measured Results

The fabricated test chip including the Cyc-CRO was tested by sweeping the supply voltage, while providing an injection clock, and observing the divided output frequency ($\div 48$). Since the Cyc-CRO has 33 elements, an injection frequency of $1.5\dot{1}$ GHz is required to achieve 10 ps time resolution. Both the simulated and measured results are plotted in Fig. 9, with schematic, RC extracted and measured results all showing a flat spot at $31.5\dot{6}$ MHz. This indicates that the Cyc-CRO has injection locked with a time resolution of 10 ps.

The frequency stability of the Cyc-CRO over time is plotted in Fig. 10, illustrating the effect of injection locking on the absolute jitter. This absolute jitter refers to that of the $\div 48$ Cyc-CRO frequency. When unlocked, the absolute jitter is 485 ps_{rms}, but when locked, the measured value reduces to 14 ps_{rms}. This jitter, however, is mainly due to the limited resolution of the oscilloscope used to make the measurement,

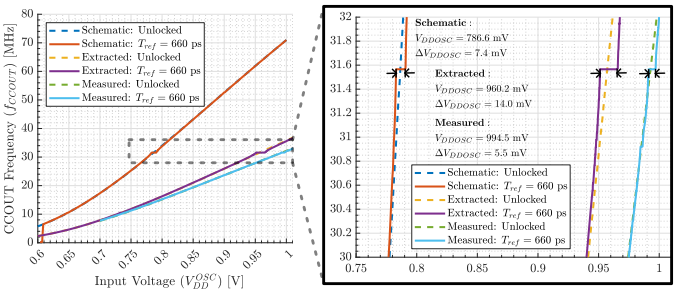


Fig. 9. Cyc-CRO Frequency divided by 48, showing locking ($31.5\dot{6}$ MHz corresponds to 10 ps resolution).

and relative drift between this scope and the injection clock. Extracted simulation with ideal measurement equipment shows an absolute jitter of 0.4 $\mathrm{ps_{rms}}$.

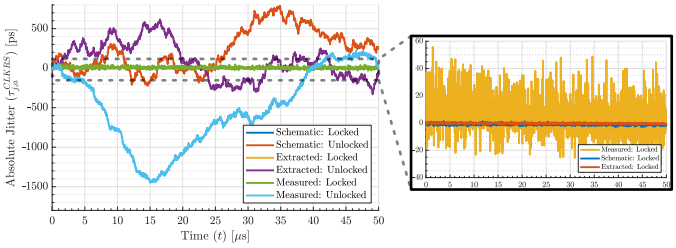


Fig. 10. Cyc-CRO frequency stability over time showing the effect of locking on absolute jitter.

The Cyc-CRO consumed 1.15 mW at its 995 mV locking input voltage to generate 10 ps time resolution.

V. Conclusion

The measured results compare very favourably with the state of the art, as shown in Table I. [12] uses resistive interpolation to generate sub-gate delay resolution, and as a result has a known phase order. The cost of this is in both power and area. The Power-Delay Product (PDP) is a FoM for time references, lower being better, and the PDP of [12] is over $5.7\times$ that of this work. The area of [12] is also much larger than this work due to the large passive devices. Similar performance is seen in the more recent resistively-interpolated work of [4]. The exact area of which is not known. The most energy-efficient Cyc-CRO published to date is the tri-state Cyc-CRO of [13], has a slightly worse PDP than that published in this work, but still suffers from unpredictable phase order.

The injection-locked Cyc-CRO presented shows superior performance to the state of the art Cyc-CRO, while providing the key advantage of predictable phase order, enabling its use in TDCs without the need for mode detection circuitry. This simplifies the generation of sub-gate delay resolution in highly-scaled technologies.

TABLE I
Comparison Table

	Technique	Tech. [nm]	Resolution [ps]	Power [mW]	PDP [fWs]	Area [$\mathrm{mm^2}$]
this work	Inj. Locked Cyc-CRO	65	10	1.15	11.5	0.000275
[12]	Resistive Interpolation	90	4.7	14	65.8	0.02
[13]	Tri-state Cyc-CRO	28	3	4.5	13.5	0.00832
[4]	Resistive Interpolation	65	6	10.3	61.8	< 0.09

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